Speed-Enhanced CMOS Level Shifting Circuits for VLSI Applications

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Abstract: -Speed-enhanced CMOS level shifting circuits are proposed for mixed voltage applications. In circuits embodying this invention, the main advantage as compared to the prior art is one more pair path to charge and discharge the output nodes simultaneously, which leads to a less PMOS to NMOS ratio problem. Therefore, the output low-to-high transition becomes faster due to charging enhancement in the initial phase. The high-to-low transition also becomes faster because of discharging enhancement in the transition period.

Key-Words: - Level shifting, Mixed voltage, Ratio problem, Low power, VLSI, CMOS

1 Introduction

In MOS IC's, MOS devices, such as MOSFET's, are employed which are biased with a high voltage and a low voltage. The low voltage is commonly referred to as VSS and is often 0 volts. The high voltage is commonly referred to as VDD and is often 5 volts. However, in some low voltage MOS IC's, the high voltage may be less than 5 volts, for example 3 volts. In this situation, some MOS IC's must accommodate multiple “high" voltage levels”. For example, the integrated circuit may have some internal circuitry which uses the VCC voltage level for the logic value '1' and other circuitry which uses a larger voltage level VDD for the logic value '1'. Alternatively, the internal circuitry uses VCC and converts to-be-outputted output signals to VDD. This kind of design scheme is suitable for low power IC's which also provide voltage level compatibility with other components of the system.

In other types of digital signal application, it is desired to have a voltage level greater than the common digital signal, which varies between zero and 5 volts. For example, to program an EEPROM memory device, it is desired to have a voltage level varying between zero and 12 volts. Thus, voltage level shifting circuits are required for such design mentioned above. So in this paper, speed-enhanced level shifting circuits are proposed with negligible static power dissipation. In the next section, descriptions of the prior art is given first. And then details of the proposed circuits are described in Section 3, along with simulation results and comparisons with the prior art in Section 4. Conclusions are given in the final section.

2 Prior Art

Voltage level shifting circuits are well-known in the literature [1]-[10] A typical prior art circuit for achieving the level shifting operation is shown in Fig. 1 [5, 6].

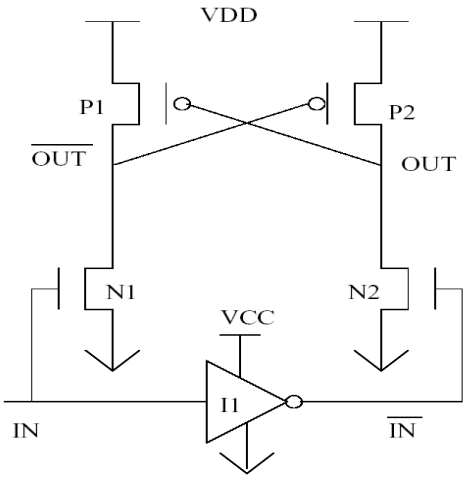

Fig. 1 Prior art 1

The circuit has two inputs for an IN signal and its complement /IN. /IN is the output of the input inverter I1 operated between a first potential of VCC and ground. In the following, detailed operations of the prior art circuit are described. First assume that IN was initially at the ground potential (0 volt), the input signal then goes high to VCC volts. This causes N1 to be turned on and N2 to be turned off. However, outputs OUT and /OUT, which were at ground and VDD, respectively, do not change immediately to VDD and ground, respectively. Because when N1 is turned on, P1 is still turned on and conducting. Therefore, the on-impedance of each P-type transistor has to be made much greater than the on-impedance of the associated N-type transistor under the same bias conditions to guarantee switching of the level shifting inverters. This physical constraint ensures that when transistor N1 (N2) turns on, /OUT (OUT) drops significantly below VDD/2 and correct logic functions are then finally achieved. Therefore, there is a ratio problem associated with the strength of PMOS to NMOS transistors in the circuit. Since the high on-impedance of each P type transistor is required, it slows the rising edge of the output signals. So the rise time of outputs OUT and /OUT are very slow when compared to their fall time. This consequence leads to the second significant problem.

The rise and fall times of the output signals are unequal. The propagation delays from input to output are thus unequal for high-to-low and low-to-high transitions. That is, the rising edge of the level shifted signal will have a relatively slow rise time and long propagation delay. While the fall time is relatively fast and the propagation delay is short. Thus, though the prior art circuit has many desirable features, its speed of operation is relatively slow.

Another prior art adds two NMOS transistors to the prior art circuit, as shown in Fig. 2[7]. NMOS transistors N3 and N4 are connected in a source follower configuration. During steady state operation, both transistors N3 and N4 are off and play no role in the generation of voltage levels at the output nodes. However, during the transient operation, either N3 or N4 will initially turn on to charge the output node. Therefore, the pull-up time of the corresponding output node is decreased. However, note that only one of the transition drivers N3 or N4 operates during each transition; the other transistor is idle. Thus, the transition drivers N3 and N4 are not used to their fullest potential.

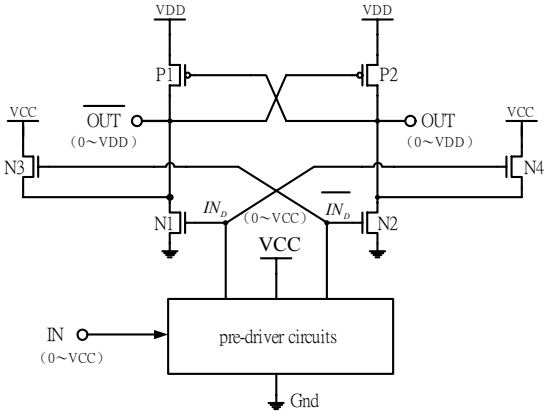

Fig. 2 Prior art 2

3 Proposed Circuits

Three proposed circuits are shown in Fig. 3, Fig. 4 and Fig. 5, respectively.

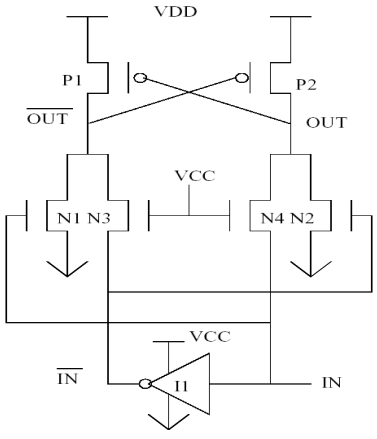

Fig. 3 Proposed circuit 1

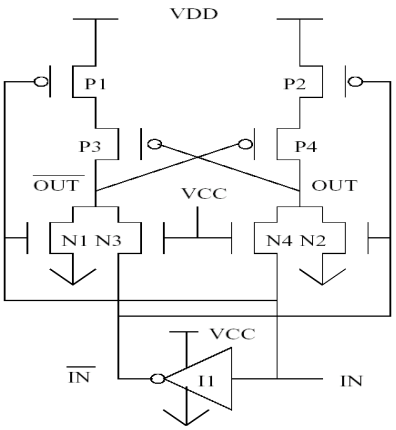

Fig. 4 Proposed circuit 2

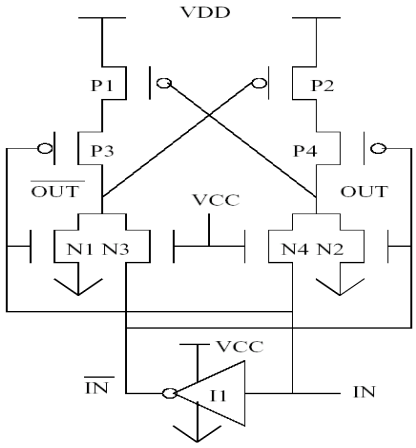

Fig. 5 Proposed circuit 3

However, we only take the first circuit as an example to detail its operation. As compared to the prior art circuit, only N type transistors N3 and N4 are added, which play a role as a pass transistor. The switching response of the circuit is now examined. Assume, initially, that IN is low (ground), and consequently, /IN is high (VCC). Then the input signal IN makes a transition from the low level (ground) to the high level (VCC). Consequently, /IN makes a transition from the high level (VCC) to the low level (ground).

As the IN signal rises from zero volts towards (VCC) volts, it reaches a value equal to the threshold voltage (VT) of transistor N1. Once transistor N1 turns on, the potential at /OUT drops from VDD volts towards ground. At the same time with N1-on, the positive going signal IN is applied to the source of N4 and the negative going signal /IN is applied to the source of N3. Now the roles of N3 and N4 in enhancing the transition speed at nodes OUT and /OUT are described. Initially, N4 is on since its gate is applied to a potential of VCC with its drain and source at the ground potential. Therefore, once the signal IN rises from zero volts N4 conducts current to charge node OUT. It keeps the charging enhancement to node OUT until the input reaches VCC. In this transition period, transistor N4 will finally charge node OUT to (VCC- threshold voltage of N4) volts. This path is an additional charge path while transistor N3 provides another discharge path during this switching operation. The role of N3 is detailed as follows. Initially, N3 is off because potentials at its gate, drain and source are VCC,VDD and VCC volts, respectively. Thus no channel exists in this transistor. After /IN drops its potential below (VCC- threshold voltage of N3) volts, transistor N3 starts to conduct current. From then on, N3 keeps the discharging enhancement to node /OUT until this node is driven to the ground potential. So, this is another discharge path to speed up the transition.

Due to the conduction of N4 the positive rise in potential of node OUT causes a decreased conductivity of P1 because of the decrease of its source-to-gate voltage. Since the impedance of P1 is increased N1 discharges node /OUT to ground faster and more sharply. This, in turn, speeds up the turn-on of P2. The pull-up of node OUT to VDD is accelerated and thus P1 is fully turn-off. As P2 turns on, it couples VDD volts to node OUT. When the potential at this node increases, the impedance of P1 is increased (less conductive). This consequence drives node /OUT more close to ground and thus P2 is turned on harder. Hence, a full positive feedback action begins and node OUT is finally driven to VDD and /OUT to ground with both P1 complete turn-off and P2 full turn-on. For this signal condition transistor N4 conducts first and then is turned off. As for N3, after the output transition is over its gate electrode is at VCC and its drain/source electrode at ground. Since the drain-to-source voltage difference is zero, it is on but non-conducting. Therefore, both transistors N3 and

N4 are non-conducting and do not dissipate any power in the steady state condition.

For the complementary input transient condition to the circuit just discussed, the same operation described above occurs with roles of (N1, N2), (N3, N4) and (P1, P2) interchanged. Therefore, this condition is not described in detail. So far, it has been shown that, in circuits embodying the present invention, the potential at an output node (OUT or /OUT) makes faster high-to-low and low-to-high transitions than in the prior art circuit of Fig. 1. This consequence results from one more pair path to charge and discharge because of the addition of transistors N3 and N4. And thus the ratio problem of the strength of PMOS devices P1, P2 to NMOS devices N1, N2 is less.

In summary, the potential of the falling output drops more sharply and results in a faster turn-on of one of these two load transistors. As the potential of this node increases it applies a faster turn-off signal to the other load device. Therefore, the speed of circuit operation is enhanced.

4 Results and Comparisons

In this section, speed-enhancement of the proposed circuits are demonstrated by Hspice simulations which are based on device parameters of a 0.6 um process. Four cases are considered for comparisons. All transistors use 0.6um as their channel length. The proposed circuit in Fig. 3 with device width P1=P2=2 um , N1=N2=6um and N3=N4=2um is classified as case a. While the prior art 1 circuits with different combinations of device size are denoted as cases b, c and d, respectively. For case b, device width of P1=P2=2 um and N1=N2=6um. For case c, P1=P2=4 um and N1=N2=6 um. For case d, P1=P2=2 um and N1=N2=8 um. In simulations, power VCC is 3 volts and larger power VDD is 5 volts. The propagation delay (tplh and tphl) is defined as the time interval between VCC/2 of the input signal and VDD/2 of the output signal. Simulated propagation delays as a function of the loading capacitance is shown in Fig. 6.

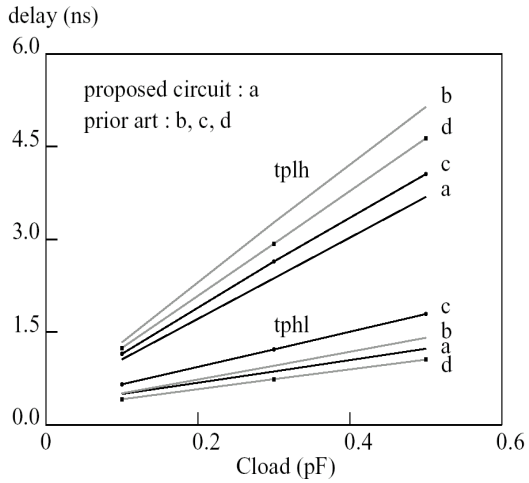

Fig. 6 Propagation delay as a function of C_{load} for four cases

Judging from the results, case a and case d show speed-up for both tplh and tphl. However, in case d the propagation delay tplh is much larger than that in case a. Besides, the propagation delay tplh is in fact the speed bottleneck of the level shifting circuit. Therefore, the proposed circuit is superior to the prior art circuit in terms of speed and area.

Another transient circuit simulations are performed for comparisons for the prior art 1, 2 and the proposed circuit 1. The loading condition is 0.1pF at the output nodes OUT and /OUT. All these three simulation results are shown in Fig. 7, Fig. 8 and Fig. 9, respectively.

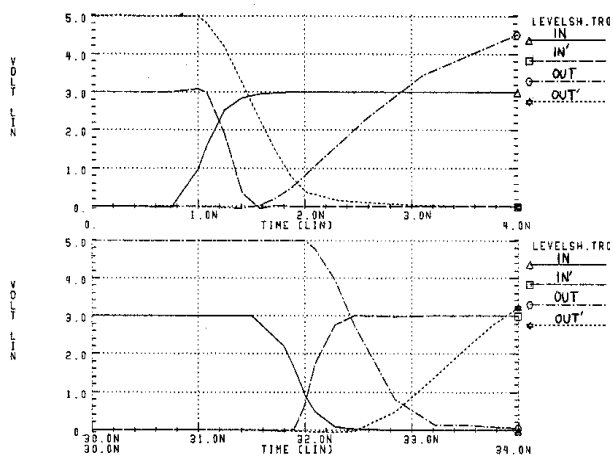

Fig. 7 Transient simulations of prior art 1

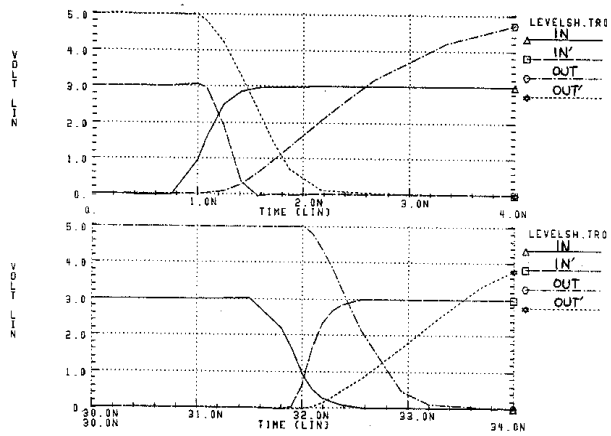

Fig. 8 Transient simulations of prior art 2

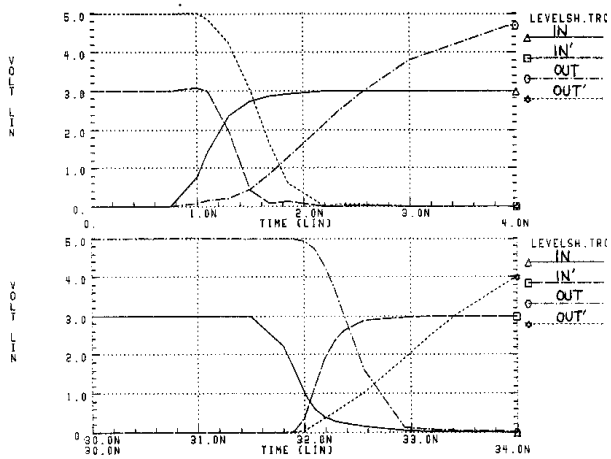

Fig. 9 Transient simulations of proposed ckt 1

Compare the propagation delays of these three cases as shown in the above figures. For the prior art 1 circuit, tplh=1.6084ns and tphl=0.60329ns. For the prior art 2 circuit, tplh=1.2825ns and tphl=0.58532ns while for the proposed circuit, tplh=1.2296ns and tphl=0.52532ns. Thus, both the smallest low-to-high and high-to-low propagation delay times are achieved by the proposed invention.

5 Conclusion

In this paper, speed-enhanced CMOS level shifting circuits have been demonstrated. Due to one more pair path to charge and discharge the output nodes simultaneously, the speed of switching response is increased along with a less PMOS to NMOS ratio problem. Since the proposed circuits offer both speed-up and negligible static power dissipation, they are suitable for mixed voltage applications such as low power VLSI design and nonvolatile memory design.

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