High and Low Speed Output Buffer Design with Reduced Switching Noise for USB Applications

HWANG-CHERNG CHOW, C. HUANG and HSING-CHUNG LIANG
Department of Electronics Engineering, Chang Gung University
Kwei-Shan, Tao-Yuan 333
TAIWAN, REPUBLIC OF CHINA

Abstract: -A novel high and low speed output buffer circuit is proposed for Universal Serial Bus (USB) interface applications. Operation principles of this novel buffer are developed based on slew rate control and delayed turn-on technique. The mechanism for slew rate control is process variation self compensating. So, both precise rise and fall times of the output signal have been obtained for low speed operation. Moreover, the pull-up and pull-down output drivers are divided into several sub-drivers in parallel with the delayed turn-on characteristics. Therefore, the change of rate of di/dt decreases. And the simultaneous switching noise, based on simulations, are reduced from maximum overshoot 3.47V to 3.36V and maximum undershoot from -0.427V to -0.068V, respectively. This proposed output buffer design is low cost due to its easy realization in a digital CMOS process. The disclosed output buffer has been integrated in a complete USB transceiver circuit. Based on measured silicon data, satisfactory functions of the whole USB application IC have been obtained.

Key-Words: - USB, Slew rate, High and low speed, Delayed turn-on, Switching noise

1 Introduction

Output drivers are used to translate an input signal, which is generated in the core of an integrated circuit with a low driving ability, into an output signal with a large driving ability. Since the capacitive load off the chip is heavy, the strength of an output buffer is made strong by merely increasing the transistor size. However, when output drivers switch they generate noise on power supply lines of this chip because they sink or surge a large current in a short time interval. This undesirable power and ground noise is generally referred to as ``ground bounce" (L • di/dt noise) [1], [2]. The ground bounce will be more severe if more output buffers are simultaneously making transitions at a higher operating speed.

For high drive output buffers, this undesirable ground bounce has to be well controlled. In the literature, a lot of work has been made to reduce this noise [3]-[9].

Recently, a protocol for serial data transmission called Universal Serial Bus (USB) was approved for computer equipment peripherals [10]-[11]. In this protocol, the USB transceiver supports two data rates of transmission. For high speed device such as display monitor a full speed data rate of 12 M bits/sec is supported. While for low speed device such as disk drive a low speed data rate of 1.5 M bits/sec is used. Moreover, the
USB standard specifies precise rise and fall rates of output voltage levels of USB compliant devices of about 4--20 nano second for full speed data communication but only 75--300 nano second for low speed communication. This presents a problem for ground bounce suppressing output buffers which are typically designed with slew rates for only a single particular data communication rate.

Therefore, this new demanding output buffer has to be versatile in use since its speed of operation can be controlled by a speed control signal. So, in this paper a novel output buffer for both high and low speed operations is proposed. This proposed circuit is very suitable for implementation in a digital CMOS process with low cost and satisfactory function.

2 Proposed Circuit Design

As shown in Figure 1, a novel output buffer with two operation modes is disclosed, in which realization is based on a standard digital CMOS process. The proposed circuit structure has a small-size driver (P0 and N0), a large-size driver (P1, P2 and N1, N2), delay element DLs, fast turn-off transistors (P10, P11, N10, N11), control inverters (I1--I6), rise/fall time control circuit and speed control signals. It is noted that inverters I1, I3 and I4 are designed to have a logic threshold (switching voltage) in excess of VDD/2 while inverters I2, I5 and I6 are designed to have a logic threshold less than VDD/2. This special arrangement will eliminate the short circuit current during circuit operations.

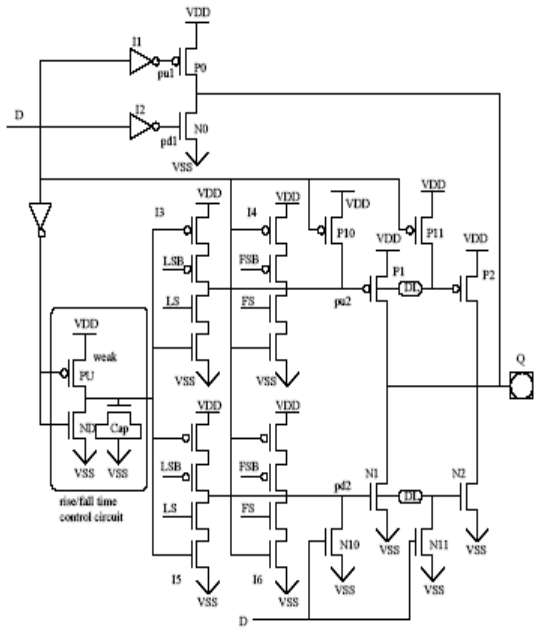
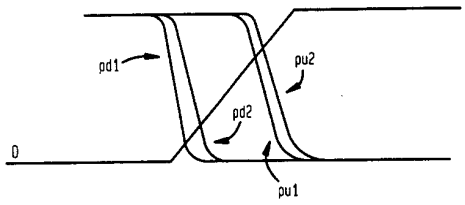
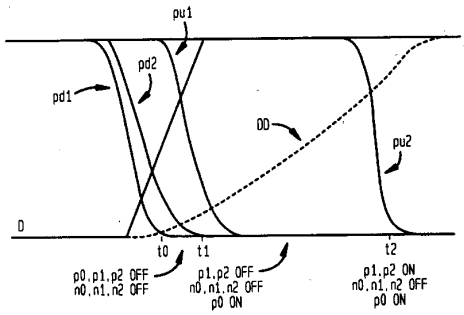


Fig. 1 Proposed high and low speed output buffer.

In the following, brief descriptions are summarized. Consider circuit operations of full speed first. Under this condition, controlled inverters I3 and I5 are tri-stated, that is, are disabled. Consider the input D changes its voltage level from logic 0 to logic 1. N0 is turned off by I2 and N1, N2 are almost at the same time turned off by I6, N10 and N11. Then P0 is turned on and P1 on and then P2 on. The timing diagram can refer to Figure 2(a). Since the pull-down driver transistors are off first then the pull-up driver transistors are activated so the short circuit current is completely eliminated. Besides, the pull-up drivers are specially arranged to turn on one by one with delay elements. Therefore, the change of rate of di/dt decreases and the simultaneous switching noise can be reduced.



(a)



(b)

Fig. 2 Timing diagram for (a) full speed operation and (b) low speed operation

Consider now low speed circuit operations. Under this condition, controlled inverters I4 and I6 are tri-stated, that is, are disabled. Consider the input D changes its voltage level from logic 0 to logic 1. N0 is turned off by I2 and N1, N2 are almost at the same time turned off by N10, N11. Then P0 is turned on first. However, the turn-on of P1 has a large time difference since the rise/fall time control circuit enables an input signal DD at I3 with a prolonged transition

time. Once P1 is on and then P2 on. The respective timing diagram can refer to Figures 2(a) and 2(b). The rise/fall time control circuit plays an important role in generating an output signal with process variation compensated slew rate. This reason is given below. The capacitor Cap is intentionally implemented as a MOS transistor. In fact, this capacitance of Cap is important of fixing the transition prolongation during low speed operation and its value is given by $Cap = \in_{ox} * AREA / t_{ox}$, where t_{ox} and $\in_{ox}$ are the thickness and permittivity of the gate oxide, respectively. Note that t_{ox} is not perfect. If t_{ox} is thinner than originally designed, then the capacitance of Cap will increase. However, the current driving strength of PU and ND will also increase. Likewise, if t_{ox} is thicker, then the capacitance of Cap will decrease but so will the current driving strength of PU and ND. Thus, such a capacitor is somewhat process variation self compensating.

In summary, when the output buffer is operated in low speed mode the small-size driver is enabled first and then the large-size driver is activated at a relative later time such as several tens of nano second according to the design.

The second proposed tri-state output buffer is shown in Figure 3. When the output enable signal EN=0 (ENB=1), then pub=0, pdb=1, pu2=1 and pd2=0. That is, the output Q is in a high impedance state. While EN=1 (ENB=0) OR1 and AND1 are both simplified to non-inverting buffers. While EN=1 (ENB=0) OR1 and AND1 are both simplified to non-inverting buffers. Therefore, the total circuit is equivalent to the first proposed circuit.

3 Simulation Results and Discussions

Figures 4(a) and 4(b) show simulations based on the proposed output buffer according to USB's spec. Simulation conditions are: full speed operation, typical process assumed, VDD = 3.3V, temperature = 25C, and loading = 50pF; and low speed operation, typical process assumed, VDD =

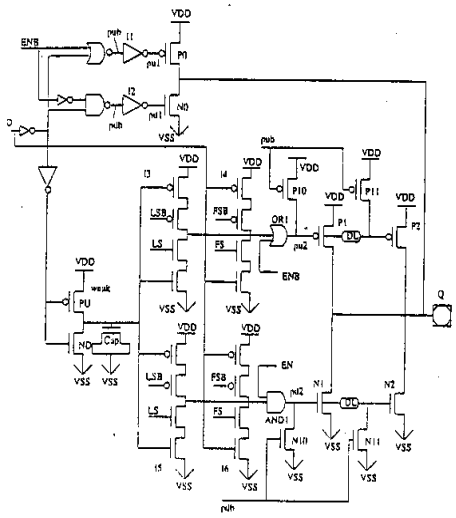
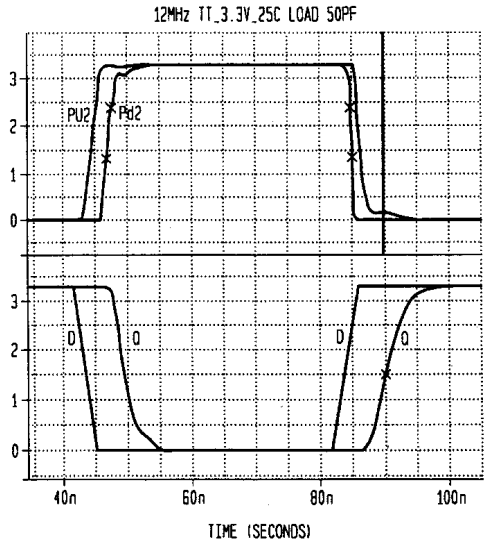


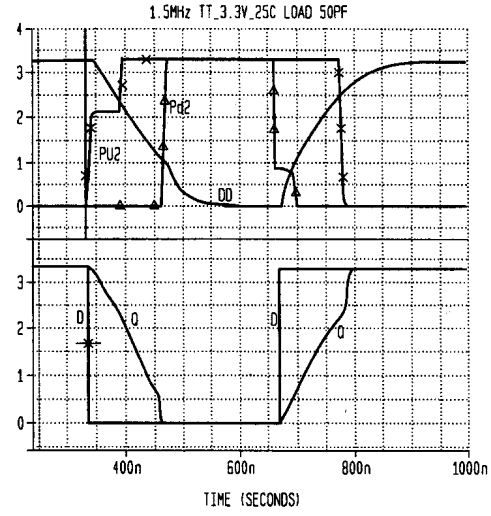
Fig. 3 Proposed tri-state output buffer.

3.3V,temperature = 25C, and loading = 50pF, respectively. In Table 1, summarized results for fast (best), typical and worst cases according to USB's spec are presented. Note that all simulations including process variations, loading conditions, operating voltages and temperatures meet the USB application requirements.

The proposed novel output buffer has been integrated in an USB application IC. The microphotograph of the realized complete USB transceiver is shown in Figure 5 **(upper right corner including two extra large pads in the right)**. The total MOS device width of driver PMOS and NMOS transistors are 1170μm and 500μm, respectively. These two large MOS transistors are actually divided into four sub-driver transistors each. The complete USB transceiver, as shown in Figure 6, needs one differential receiver, two single-ended receivers and two USB output buffers (Figure 3 circuit) with speed control. Figures 7(a) and 7(b) show the measured 3.3V and 1.5 MHz operations for VPO to D+ and VMO to D-, respectively. In Table 2, we summarize respective measured data for low speed operations with operating voltages ranging from 3.6V to 3.0V. For verification of full speed operations it is performed by the whole chip function. All system function is so far satisfactory. Therefore, the validity of the proposed buffer design is confirmed.



(a)



(b)

Fig. 4 Simulation results for (a) full speed operation and (b) low speed operation.

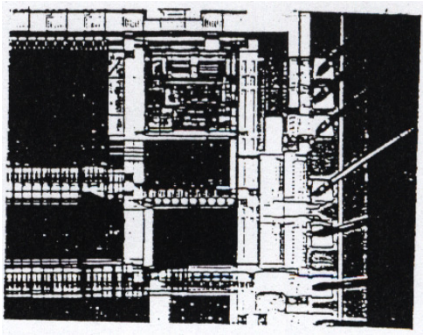


Fig. 5 Microphotograph of integrated complete USB transceiver (upper right corner).

Table 1 Summary for full and low speed operations

Full Speed

Parameter	Best	Typical	Worst
V_{DD}	3.6volts	3.3volts	3.0volts
Temperature	0˚C	25˚C	85˚C
Load	50pF	50pF	50pF
Fall time	4.5nsec	5.5nsec	7.2nsec
Rise time	4.8nsec	6.0nsec	7.9nsec
Delay	4.5nsec	5.9nsec	9.5nsec

Low Speed

Parameter	Best	Typical	Worst
V_{DD}	3.6volts	3.3volts	3.0volts
Temperature	0˚C	25˚C	85˚C
Load	50pF	50pF	350pF
Fall time	75nsec	101.2nsec	122.2nsec
Rise time	75.5nsec	101.2nsec	102.6nsec
Delay	54.8nsec	73.6nsec	206.4nsec

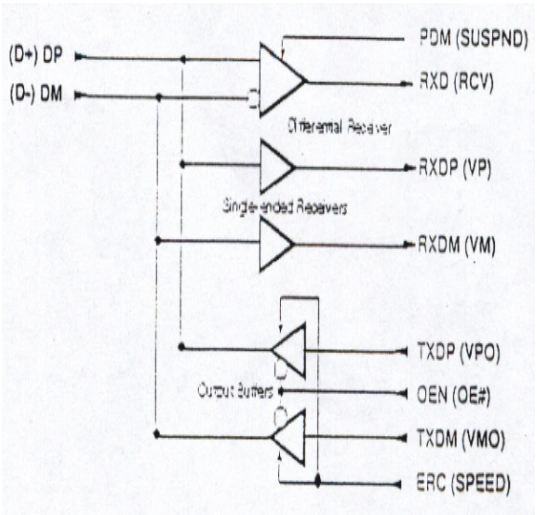


Fig. 6 Complete USB transceiver circuit.

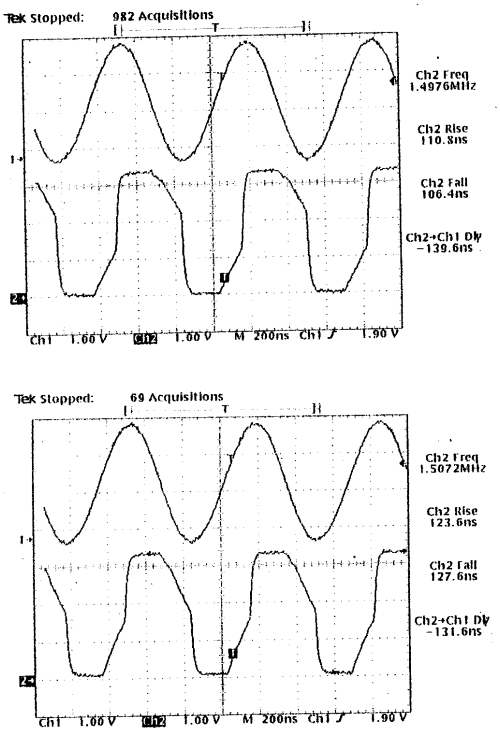
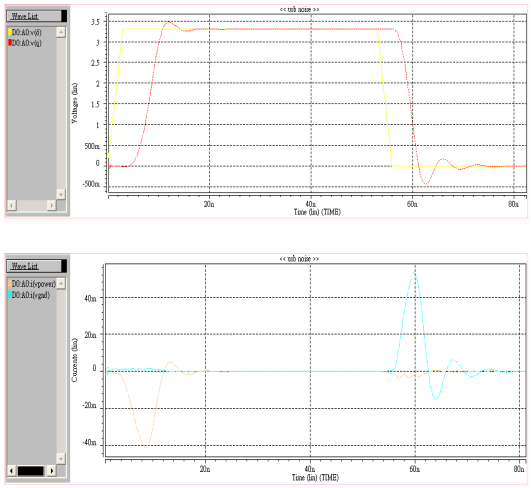


Fig. 7 Measured results for (a) VPO to D+ and (b) VMO to D-, all in low speed operations.

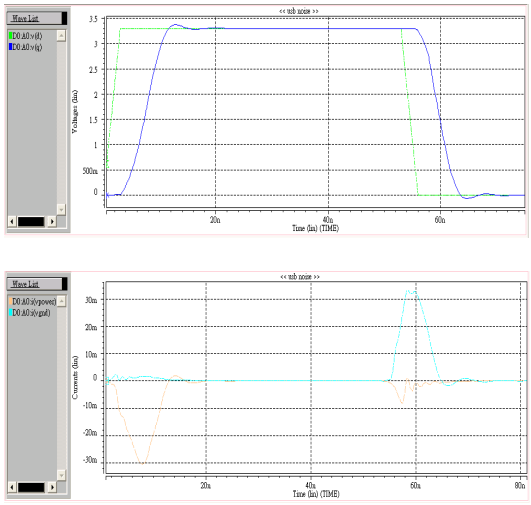
Table 2 Measured performance for low speed operation.

XCVR \ PWR		3V	3.3V	3.6V
VPO->D+	Rise time	118.4ns	110.8ns	104.0ns
	Fall time	117.2ns	106.4ns	103.2ns
	Delay	134.8ns	139.6ns	132ns
VMO->D-	Rise time	136.4ns	123.6ns	115.6ns
	Fall time	145.6ns	127.6ns	124.0ns
	Delay	132.8ns	131.6ns	139.6ns

As for the noise performance, it is shown in Figure 8. For noise simulation purpose, both power VDD and ground GND are connected in series with an inductor of 20 nano Henry, which results from the bonding wire of the package. Two cases are considered. The first one is a single large output driver for pull-up and pull-down operations. Simulation results of input D, output Q, transient power current and ground current are given in Figure 8(a). Note that the maximum overshoot and undershoot of output Q are 3.47V and -0.427V, respectively. The peak currents are over ±40mA. While in Figure 8(b) are simulations of the proposed design. The maximum overshoot and undershoot of output Q are effectively reduced to 3.36V and -0.068V, respectively. And the peak current are well controlled in ±33mA. The noise performance is improved significantly.



(a)



(b)

Fig. 8 Noise performance (a) without noise design (b) with noise design (this work).

4 Conclusion

A novel output buffer circuit with both high and low speed operations for USB applications has been presented. The proposed circuit is low cost in terms of implementation since it can be easily integrated in a standard digital CMOS process. Furthermore, the mechanism for slew rate control is process variation self compensating. So, both precise rise and fall times of the output signal have been obtained for low speed operation. Moreover, the pull-up and pull-down output drivers are divided into several sub-drivers in parallel with the delayed turn-on characteristics. Therefore, the change of rate of di/dt decreases and the simultaneous switching noise are reduced from 3.47V to 3.36V and -0.427V to -0.068V, respectively. Based on both simulation and measured results, the proposed output buffer gives very satisfactory circuit function and therefore this novel design meets the demanding USB application requirements very well.

References:

[1] G. A. Katopis, Delta-I noise specification for a high-performance computing machine, *IEEE Proceedings*, 1985, pp. 1405-1415.

[2] R. Senthinathan, G. Tubbs and M. Schuelein, Negative feedback influence on simultaneously switching CMOS outputs, *Proc. of IEEE Custom Integrated Circuits Conf.*, 1988, pp. 5.4.1-4.

[3] E. Chioffi, F. Maloberti, G. Marchesi and G. Torelli, High-speed, low switching noise CMOS memory data output buffer, *IEEE J. Solid-State Circuits*, Vol. 29, 1994, pp. 1359-1365.

[4] C. S. Choy, C. F. Chan and M. H. Ku, A feedback control circuit design technique to suppress power noise in high speed output buffer, *Proc. of IEEE ISCAS*, 1995, pp. 307-310.

[5] K. Leung, Controlled slew rate output buffer, *Proc. of IEEE Custom Integrated Circuits Conf.*, 1988, pp. 5.5.1-4.

[6] M. Hashimoto and O.-K. Kwon, Low di/dt noise and reflection free CMOS signal driver, *Proc. of IEEE Custom Integrated Circuits Conf.*, 1989, pp. 14.4.1-4.

[7] T. Gabara, W. Fischer, J. Harrington and W. Troutman, Forming damped LRC parasitic circuits in simultaneously switched CMOS output buffers, *Proc. of IEEE Custom Integrated Circuits Conf.*, 1996, pp. 13.5.1-4.

[8] K. Asahina, S. Kato and S. Kayano Output buffer with on-chip compensation circuit, *Proc. of IEEE Custom Integrated Circuits Conf.*, 1993, pp. 29.1.1-4.

[9] S.-J. Jou, W.-C. Cheng and Y.-T. Lin, Simultaneous switching noise and low bouncing buffer design, *Proc. of IEEE Custom Integrated Circuits Conf.*, 1998, pp. 25.5.1-4.

[10] G**.** Ramamurthy and K. Ashenayi, Comparative study of the FireWire/spl trade/ IEEE-1394 protocol with the Universal Serial Bus and Ethernet, *IEEE Midwest Symposium on Circuits and Systems*, 2002, pp. II-509-II-512.

[11] C.-P. Young, M. Devaney, and S.-C. Wang, Universal serial bus enhances virtual instrument-based distributed power monitoring, *IEEE Transactions on Instrumentation and Measurement,* Vol. 50, 2001, pp. 1692-1697.