EFFECTING POWER CONSUMPTION REDUCTION IN DIGITAL CMOS CIRCUITS BY A HYBRID LOGIC SYNTHESIS TECHNIQUE

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Abstract:- Power Dissipation of CMOS circuits can be reduced by 50% - 80% by lowering switching activity. In practice, power reduction by an order of 10% - 50% can be obtained by appropriate design efforts [1]. In this paper, an approach is presented for minimizing the power consumption of static digital circuits, based on a function realization method, which employs hybrid gate logic. This approach aims at minimizing the worst case circuit switching activity, transition activity factor, while simultaneously fostering uniformity in the individual gate switching activity, besides reducing it. The universal logic gates with varying inputs and the inverter used in the non-regenerative circuits, were designed using MOS transistors based on 3.3V, 0.5 μm CMOS technology. A significant number of digital circuits were designed and an average reduction in power consumption of the order of 20% - 25% was achieved by way of the proposed synthesis technique, in comparison with the conventional one. The accuracy of the approach is verified by comparing the values calculated by an extension of the method outlined in [2], with that obtained through SPICE simulation studies and they are found to be in close agreement, thus highlighting the usefulness of the proposed strategy, especially for multilevel digital architectures.

Key-Words:- Total circuit switching activity, Individual gate activity, Transition Activity Factor (TAF), Quality of Silicon (QoS), Total Power Dissipation (TPD)

1. Introduction

Recently, there has been a major focus on the design methodology of digital circuits, which directly addresses the issue of power management. More than ever, circuit designers are recognizing the impact of power consumption on IC performance, as it is directly linked to its reliability [11]. The over-whelming demand for portable and mobile electronics encourages the development of a power optimized structure. Given the increasing complexity of designs, power optimization should be a conscious effort starting from the initial stages of a design, where the opportunity to save power is at a maximum.

There are three components of power dissipation in digital CMOS circuits, which are summarized as,

$$P_{avg.} = P_{switching} + P_{short\ ckt.} + P_{leakage} \quad \ldots. (1)$$

The switching (or) dynamic component of power consumption arises when the capacitive load, C_L of a CMOS circuit is charged through PMOS transistors to make a low to high voltage power consuming transition, which is usually the supply (Vdd). Very high power losses in CMOS circuits are dynamic losses, related to gate output transitions. Since CMOS circuits do not consume much power if they are not switching, a major focus of low power design is to reduce the switching activity (or) transition activity to the minimal level, required to perform the computation. Minimization of power dissipation in CMOS based system designs can take place at four levels: technology, circuit, architecture and algorithm. In this paper, this issue is addressed at the circuit level (or) logic level for digital CMOS circuits. The rest of this paper is organized as follows. In Section 2, we first review the power dissipation model, then introduce basic terminology and state the key assumptions, the proposed logic realization technique and constraints of our work. In Section 3, we present specific example problems that

validate and demonstrate the efficiency of our proposed function realization technique, along with the results obtained. We conclude in Section 4.

2. Preliminaries and Assumptions

2.1. A Power Dissipation Model

With a simplified model for power dissipation and subsequently energy dissipation in CMOS circuits, the average switching component of power dissipation of a CMOS gate is directly related to its transition activity factor, as it is generally given by,

$P_{switching} = \alpha \cdot C_L \cdot Vdd^2 \cdot Fclk$ …. (2)

where C_L is the load capacitance associated with the output node of a gate, Fclk is the clock frequency, if the gate is part of a synchronous digital system controlled by a global clock (or) the rate of arrival of inputs in a static system and α is referred to as the node transition activity factor (or) switching probability (or) transition probability. An input signal 'a' of a logic circuit can be described with two statistical signal attributes, namely the static signal probability p(a) and transition probability α (a).

Definition 2.1.1: The static probability, p(a), associated with the input signal 'a' is the probability that the signal is true (or) in the logic high state. Hence, it follows that, $p(a = 1) = 1 - p(a = 0)$ …. (3)

*Definition 2.*1.2: The transition probability, α of signal 'a' is defined as the probability for the signal to undergo a transition either from logic one to logic zero or vice-versa, during two successive clock cycles. In general, α denotes the average number of times in each clock cycle that the gate output node makes a power consuming transition.

2.2. Assumptions

We make the following simplifying assumptions.

1) The intrinsic and extrinsic capacitances are combined and modeled as a single load capacitance, present at the output node of the gate.
2) Either current is flowing through a path from Vdd to O/P capacitor or from O/P capacitor to ground.
3) Any change in a logic-gate output voltage is a change from Vdd to ground or vice-versa.
4) The inputs are uniformly distributed and uncorrelated. No feedback signal paths exist.

These assumptions are reasonably accurate for well-designed CMOS static gates and when combined, imply that the energy dissipated by a CMOS logic gate each time its output changes, is roughly equal to the change in energy stored in the gate's output capacitance. Hence the dynamic power consumed by the digital circuit can be effectively described by means of the following equation,

$$P_{dyn.} = 0.5 \sum_{i=1}^{N} C_i \cdot Vdd^2 \cdot Fclk \cdot E(i) \quad \text{…. (4)}$$

where E (i) is the expected value of the number of gate output transitions over a global clock period and N is the total number of gates present in the circuit.

2.3. Computation of Switching Activity

Table 1. Transition table for a logic gate

Present state I/P vector Ap(t)	Next state I/P vector, Ap(t+1) A_0 A_1 A_2 A_3 …… A_{n-1}
A_0	0 1 0 1 …… 0
A_1	1 0 1 0 …… 1
A_2	1 1 0 1 …… 1
A_3	0 1 1 0 …… 0
.	.
.	.
.	.
.	.
A_{n-1}	1 0 0 1 ….. …… . 0

In the above table, with n different input signals, logic '1' denotes a change in gate output and logic '0' indicates no change. The total no. of '1's in the table gives the individual gate activity. The worst case circuit switching activity is then a summation of the activities of the individual gates, present in the circuit, computed in the same manner. Hence, the total circuit switching activity is given by,

$$C_T = \sum_{i = 1 \text{ to } N} C_i \quad \text{…… (5)}$$

The worst case transition activity occurs in the circuit, when all possible sequences of input vector patterns are exhausted, such that the sequences do not get repeated.

Let us consider an n input logic circuit, comprised of a number of digital gates. With n inputs, there are totally 2^n possible input patterns. In fact, it is a cumbersome and time-consuming task to estimate the worst case circuit activity via, the tabular method illustrated above, as it amounts to creating an $(n \times n)$

matrix for each gate and the complexity of the procedure increases by an order of $(n \times n)$ as n increases. Hence we resort to an alternate method, which is less time expensive, while at the same time, computationally more efficient.

This method actually entails enumeration of the ON set and OFF set of the gate under consideration and subsequently doubling the product of cardinality of both the sets. This is a simple and straightforward approach to evaluate the total possible transitions at any gate output. By adopting the above procedure, one can estimate the worst case switching activity measure for the entire logic circuit, as its complexity decreases by an O (n), with an increase in the no. of inputs to the gate by an equivalent measure. It can be observed that, the switching activity tends to decrease with an increase in inputs. Obviously, an inverter associated with the primary input of a circuit suffers from the worst case switching activity phenomenon. Hence from the above discussion, it naturally follows that a logic gate with an equi-normal distribution of elements in both its ON and OFF sets tends to have maximum switching activity, while the one with a singleton ON (or) OFF set, usually experiences minimum number of transitions at its output node.

2.4. Proposed Synthesis technique

The SoP (Sum of Products) and PoS (Product of Sums) reduced standard forms of Boolean expressions, extracted after minimization of a multivariable canonical Boolean function, using traditional minimization procedures, such as Karnaugh Map method or Tabulation method are generally referred to as the conventional synthesis techniques. It is well known that the reduced SoP and PoS forms are implemented using universal NAND logic and NOR logic gates respectively, along with inverters, whenever complementary versions of input signals are present. It was stated above that the input inverters tend to exhibit the greatest switching activity and consequently contribute much to the total power dissipation of the circuit. Hence our proposed logic synthesis technique mainly focuses on the need for elimination of inverting buffers associated with the primary inputs of the circuit, apart from designing circuits with the lowest possible activity. In particular, De-Morgan's laws of Boolean algebra [10] are effectively and innovatively employed to achieve such a function realization.

Our method actually consists in realization of reduced forms of Boolean expressions, obtained by usual minimization methods, using mixed universal logic gate types, which is a deviation from the conventional approach. In other words, the reduced and modified Boolean expressions contain both SoP and PoS formats, realized by using both NAND and NOR type logic gates together. Hence the name, hybrid logic synthesis. This synthesis method completely does away with primary input inverters, but may result in inverters cropping up in the intermediate levels of the circuit, whose transition probability is wholly dependent upon its driving gate and as a result, experiences minimal activity at its output node. Even if more inverters tend to appear in the intermediate nodes (or) levels of the circuit, they can be conveniently replaced by a single inverter placed at the output node of the circuit, using the concept of Bubble pushing.

This hybrid logic synthesis technique is best suited for those reduced forms, whose individual sum terms (or) product terms contain more than one literal in its complemented form, leading to power consumption minimization, decrease in area, reduction of propagation delay and consequently a better Quality of Silicon (QoS) design metric. QoS is becoming the new industry standard for evaluating the "goodness" of an IC design. QoS measurements include speed, die area and power. The power portion of QoS measurement consists of both the static and dynamic component. As QoS becomes widely adopted in the industry, the importance of designs with lower power consumption will subsequently become more apparent.

Before attempting to decide on the best version of realization of a circuit for the given functionality, the worst case circuit switching activity of both the reduced expressions have to be studied, based upon which, a particular expression is selected, which gives the minimum and optimum values, as illustrated by the following examples.

The theoretical calculations performed to estimate the average power dissipation bounds of the combinational logic circuits cited below, are based upon the equations, explained in detail, available in references [3], [4], [5] and [6].

3. Example Functions

3.1. A 3 variable Boolean function

$Y_{ON} = \{ 0, 7 \}$

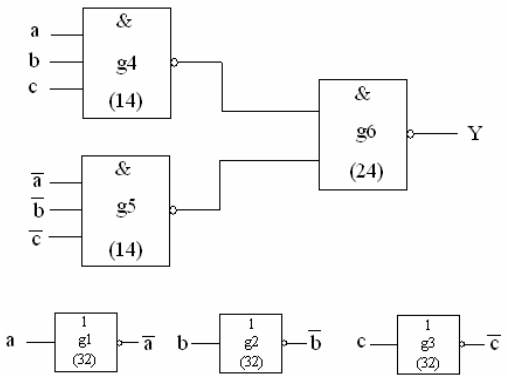

Fig. 1 Conventional Realization

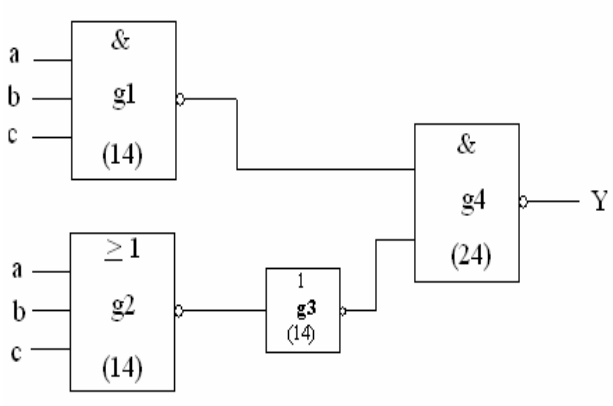

Fig. 2 Reduced switching activity realization

Table 2. Characterization of output node transition probabilities of gates of both circuits

Function type	TAF	g1	g2	g3	g4	g5	g6
Conventional realization	α	0.25	0.25	0.25	0.1094	0.1094	0.1792
Reduced switching activity realization	α	0.1094	0.1094	0.1094	0.1792	-----	-----

Table 3. Comparison of performance at Vdd=3.3V using 0.5µm CMOS technology

Function type	Total circuit switching activity	Device count	%age reduction in TPD by simulation	%age reduction in TPD by calculation
Conventional realization	148	22	-----	-----
Reduced switching activity realization	66	18	27.69	27.9

3.2. A 4 variable Boolean function

Y_{OFF} = { 3, 6, 7, 8 }

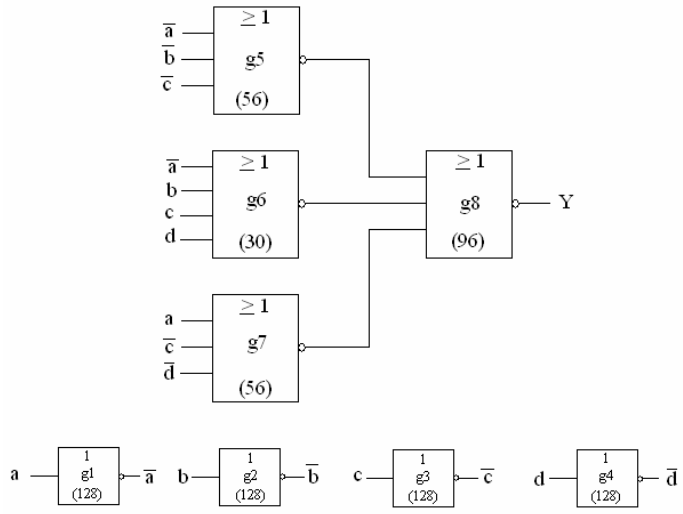

Fig. 3 Conventional Realization

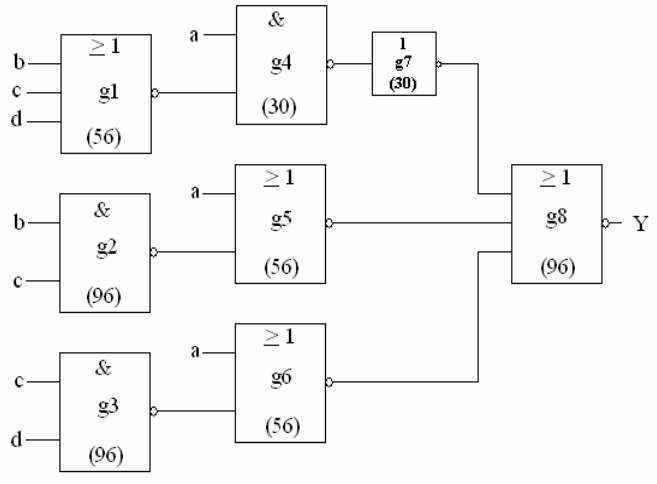

Fig. 4 Reduced switching activity realization

Table 4. Characterization of output node transition probabilities of gates of both circuits

Function type	TAF	g1	g2	g3	g4	g5	g6	g7	g8
Conventional realization	α	0.25	0.25	0.25	0.25	0.1094	0.059	0.1094	0.2025
Reduced switching activity realization	α	0.1094	0.1875	0.1875	0.059	0.1094	0.1094	0.059	0.2025

Table 5. Comparison of performance at Vdd=3.3V using 0.5µm CMOS technology

Function type	Total circuit switching activity	Device count	%age reduction in TPD by simulation	%age reduction in TPD by calculation
Conventional realization	750	34	-----	-----
Reduced switching activity realization	516	34	16.46	15.44

3.3. A 5 variable Boolean function

Y_{ON} = { 8, 12, 14, 16, 18, 22, 24, 28, 30 }

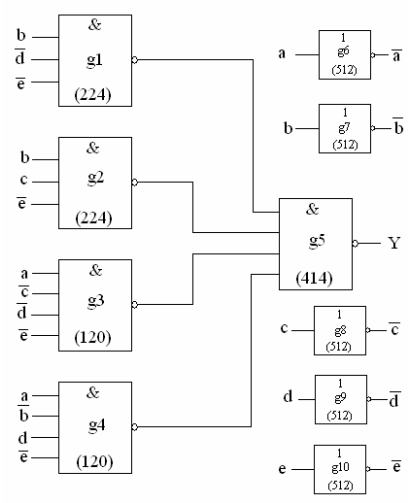

Fig. 5 Conventional Realization

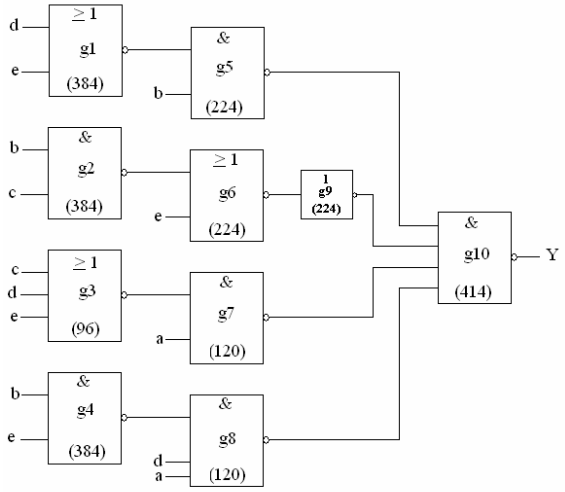

Fig. 6 Reduced switching activity realization

Table 6. Characterization of output node transition probabilities of gates of both circuits

Function type	TAF	g1	g2	g3	g4	g5	g6	g7	g8	g9	g10
Conventional realization	α	0.1094	0.1094	0.0586	0.0586	0.2201	0.25	0.25	0.25	0.25	0.25
Reduced switching activity realization	α	0.1875	0.1094	0.1875	0.1875	0.1875	0.0586	0.1875	0.0586	0.1094	0.2201

Table 7. Comparison of performance at Vdd=3.3V using 0.5µm CMOS technology

Function type	Total circuit switching activity	Device count	%age reduction in TPD by simulation	%age reduction in TPD by calculation
Conventional realization	3662	46	-----	-----
Reduced switching activity realization	2478	46	14.52	15.31

4. Conclusion and Ongoing Work

This paper suggests a method of achieving power consumption reduction in non-regenerative digital logic circuits, based on a hybrid logic synthesis technique. The simulation results obtained so far are encouraging and hence this work is being extended by going in for optimization of higher order multiple ouput complex digital topologies. Also, the possibility of greater benefits that can be derived, by coupling the proposed strategy with other appropriate low-power circuit level design algorithms and methodologies is concurrently explored, so as to achieve optimal QoS critical design metrics for higher levels of abstraction.

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