A Switched Approach for a Voltage Generator

E. VARGAS-CALDERON and F. SANDOVAL-IBARRA
Electronics Design
CINVESTAV-Guadalajara Unit
Prol. López-Mateos Sur 590, 45235 Guadalajara Jalisco
MEXICO
http://www.gdl.cinvestav.mx

Abstract: - In this paper, the design of a voltage generator (VG), realized with the switched-capacitor (SC) approach, is presented. The VG is primarily intended for low-power portable applications, where the proposed circuit is supplied by a single 1.5V battery. This approach allows to obtain a ×2-VG driving an output current of 1mA and can be easily extended to a ×3 design. Simulation results verify the usefulness of the proposed design.

Key-Words: DC-DC power conversion, charge pump, CMOS integrated circuits.

1 Introduction

Nowadays the most important device in modern microelectronics is the MOSFET that is being used in the most demanding applications of low power products operated by a single battery; portable products where the battery lifetime must be as high as possible. In practice a voltage level higher than the battery voltage is preferred to supply analog circuits because of the dynamic range. According that, this paper deals with the design of the voltage-generator block depicted in Fig. 1, where the block diagram represents our portable measuring system (PMS) under design. Description of each block, but the voltage-generator, will not be treated here because it can be found elsewhere [1]-[5].

This paper presents a CMOS voltage generator biased with a battery of 1.5V. In section 2, Basics on VG are presented. The effect of the increment of the switch resistance, as well as its design considerations using a MOS approach, are also presented in this section. A SC analysis of the proposed generator is presented in section 3, where simulation results for a ×2 verify its MOS viability. Finally, some conclusions are given.

2 Basics on VG

The simplest VG is the ×2-design depicted in Fig, 2. Using transistors as ideal switches ($R_{ON}\rightarrow 0\Omega$) and two equal capacitors, C_1 and C_2, a *doubler* is easily designed by connecting C_1 to the battery during Φ_1 through S_2 and S_4. Then, disconnecting it and then stack C_1 on top of the battery in such a way that C_2 is parallel connected with the stack during Φ_2 through S_1 and S_3.

Assuming a zero ON-resistance for each switch, it's easy to demonstrate that the voltage V_{OUT} on the top of C_2 is ideally $2V_{BIAS}$. However in order to analyze the effect of the non-zero ON-resistance on the VG performance the model depicted in Fig. 3 must be used.

2.1 Non-zero ON-resistance approach

When the effect of R_{ON} and discharge current I is taken into account V_{OUT} is not ×2 because losses are function on the charge and discharge time of the capacitors. These times depend on the R_{ON}, $C_{1,2}$ and the operating current (I). Assuming $R_1=R_2=R_3=R_4=R_{ON}$, and $C_1=C_2=C$ the output voltage V_{OUT} is given by

$$V_{OUT}=2V_B-\frac{I}{C}\left(T+T_2\cdot\left(1-e^{-(T_2/RC)}\right)\right)\cdot\left(\frac{3}{4}+\frac{e^{-(T/4RC)}}{2}\right)-\frac{IT_3}{C}\left(1+e^{-(T/4RC)}\right)-IR\left(3+e^{-(T_3/RC)}\right)\cdot\frac{2T_3}{T} \quad (1)$$

Even when (1) is not accurate at all, this result is an approximated method to describe the V_{OUT} behavior. Eq. (1) is accurate when $2RC\leq\frac{1}{2}T$ is satisfied. The magnitude of the undesirable ripple is given by

$$V_{RIPPLE}=\frac{I}{2C}\left(T+T_2\cdot\left(1-e^{-(T_2/RC)}\right)\right) \quad (2)$$

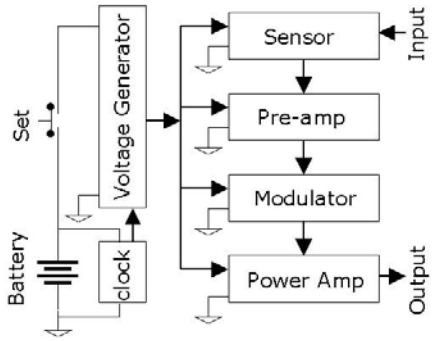

Fig. 1. Block diagram of the PMS under design.

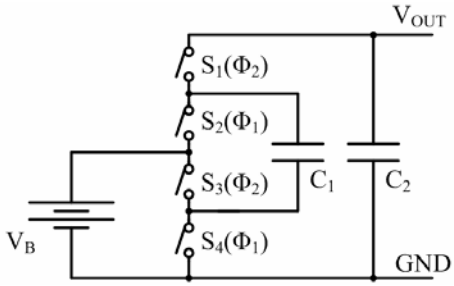

Fig. 2. Conceptual approach of a ×2 voltage generator.

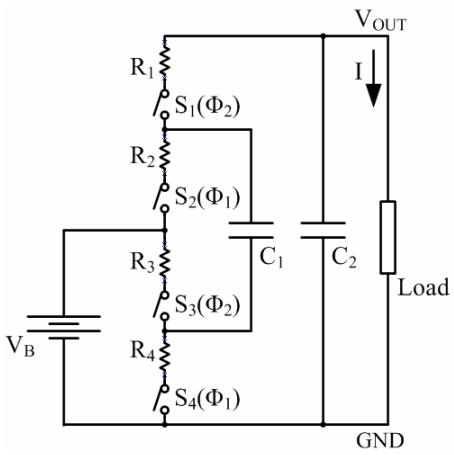

Fig. 3. A ×2 voltage generator including switch's series resistance

where $\mathbf{T_2}$ is the portion of time in which C_2 delivers charge to the load and is given by

$$T_2 = \frac{T}{2} e^{-(10RC/T)} \tag{3}$$

Finally, $\mathbf{T_3}$ is the portion of time in which C_2 gets charge from C_1

$$T_3 = \frac{T}{2}\left(1 - e^{-(10RC/T)}\right) \tag{4}$$

To probe how accurate these equations are, a comparison between simulation results and deduced equations is done. Results are shown in Fig. 4.

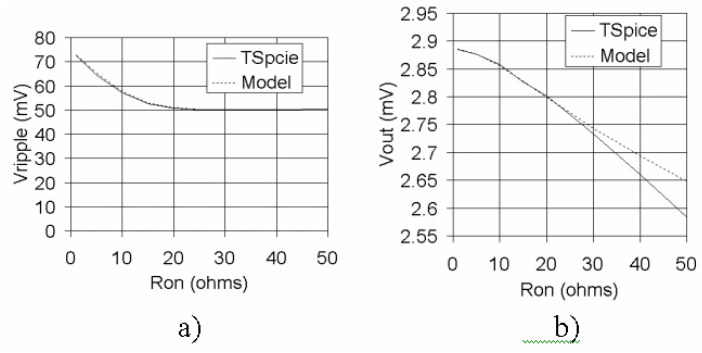

Fig. 4. (a) V_{RIPPLE} ; (b) V_{OUT} with R_{ON} as variable.

2.2 The MOS switch

This device behaves like a resistor in the ON-state and like an open circuit in the OFF-state. The important parameters of the MOS transistor from the standpoint of switched approach are the ON-resistance and its voltage threshold. It is a common practice assuming that transistor can be modeled as a non-zero resistor R_{ON} during the ON-state. However the effect of R_{ON} on the operation of the doubler represents a loss of efficiency because of the voltage drop on it. In other words, the time to charge the capacitors increases with the increment of R_{ON}. For a single MOS transistor, R_{ON} is approximately given by

$$R_{ON} = \frac{L}{\mu_o C_{ox}(V_{GS} - V_T)} \cdot \frac{1}{W} = R'_{ON} \cdot \frac{1}{W} \tag{5}$$

where μ_o, C_{ox} and V_T are technological parameters, while R'_{ON} is the normalized ON-resistance.

2.3 The CMOS doubler

In order to develop a voltage doubler with minimum components we are proposing a design by using complementary transistors, this way, one clock phase (Φ) and a non-overlaping phase (Φ') will be needed. Φ' has the same phase than Φ but it has a short delay in order to avoid high current flow through complementary transistor when they are switched. The doubler is shown in Fig. 5, where just four MOS transistors and two capacitors are needed. Every transistor will substitute each ideal switch with its series resistance, so we expect the same behavior

between the circuit shown in Fig. 5 and that shown in Fig. 3. When Φ=**1**, nMOS transistors will be on while pMOS transistor will be off, this way C_1 will be connected to V_B. When Φ=**0** - nMOS transistors off and pMOS on, so C_1 will be connected in series with V_B and it will deliver charge to C_2.

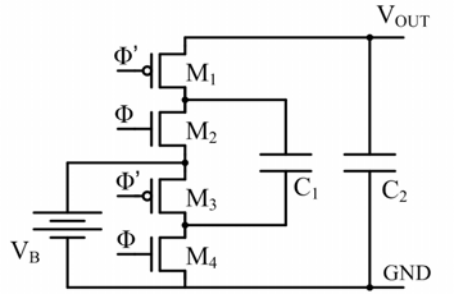

Fig. 5. The proposed CMOS ×2 VG.

The clock phases Φ and Φ' are internally generated by using a VCO-based clock generator (**CKG**). The used topology is that reported by Baker [9]. The CKG , shown in Fig. 6, is directly fed by the battery V_B. The circuit generates a 250 kHz clock phase with amplitude equal to V_B (1.5V), and the control voltage is fixed to V_C =765 mV.

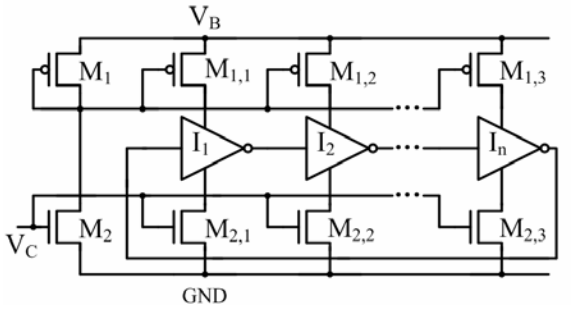

Fig. 6. Block diagram of the Voltage Controlled Oscillator.

According to [9], the oscillation frequency is given by

$$f_{osc} = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}} \quad (6)$$

where C_{tot} is the total capacitance of each single inverter and is given by

$$C_{tot} = \frac{5}{2} C'_{ox} \left(W_p L_p + W_n L_n \right) \quad (7)$$

As was already said, the value of I is given by V_C as well as by geometrical parameter -mainly M_2 -. As can be seen, pMOS transistors form current mirrors so that the charge current can be the same than the discharge current for each inverter.

Once we have a 250 kHz and 1.5 V_{PP} clock phase, it will be necessary to increase the amplitude of this signal in order to feed every gate in the voltage doubler (see Fig. 5). That is true because M_2 won't turn on when we apply 1.5V to its gate. The reason is simple, the gate-to-source voltage will be zero (V_{GSM2} = 0). In order to overcome such difficulty we have designed a circuit called "signal booster" (see Fig. 7).

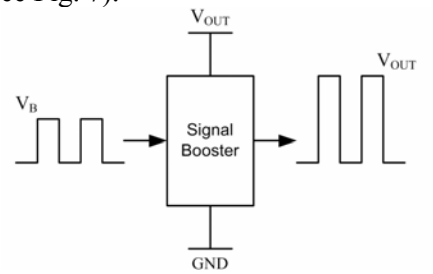

Fig. 7. Block diagram of the signal booster

2.4 Voltage doubler design

Knowing just two designing parameters (V_B=1.5V and I_{output}=1mA), and selecting common values for capacitors (C_1=C_2=100nF), we have used the deduced mathematical model to select an appropriate ON-resistance value for each transistor. It was found that using an R_{ON} = 20 Ω we could get V_{OUT} = 2.85 V and V_{RIPPLE} = 20 mV. Once we have selected the value of R_{ON}, we must determine the size of transistors by using (5). Firstly, it will be necessary to get the V_{GS} values for each transistor (see Fig. 5). Taken into account that we will have an output voltage V_{OUT}=2.85V, the gate to source voltages for each transistors are V_{GSM1} = V_{GSM4} = 2.85 V and V_{GSM2} = V_{GSM3} = 1.35 V. Then using technological parameters we can get the corresponding size which are summarized in Table 1.

	(W/L) (μm)
M_1	(2172/1.8)
M_2	(3380.4/1.8)
M_3	(7555.2/1.8)
M_4	(650.4/1.8)

Table 1. The transistors' size.

3 Simulation Results

Spice results are shown in Fig. 8, where the doubler performance can be seen. The initial voltage is approximately 0.8 V that is the result of the battery voltage minus the voltage drop across the diode in the signal booster.

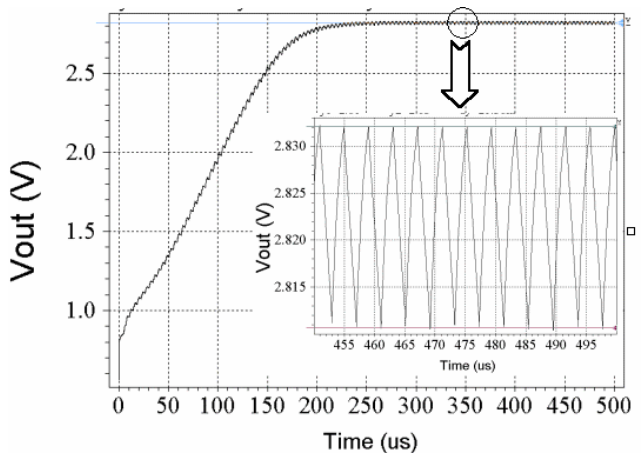

Fig. 8. The time response of the voltage doubler with an output current of 1mA.

The voltage takes several microseconds to reach its stable-state because the output level of the signal booster is always V_{OUT}. Then this voltage level is applied to each transistors' gate, so R_{ON} will be high until V_{OUT} reaches its final value. Zoom of Fig. 8, shows V_{OUT}=2.8216V and V_{RIPPLE}=21.38mV.

4 Conclusions

The design of voltage generator realized with the switched-capacitor approach was presented. The design uses technological parameters of a 1.2µm CMOS process, N-well, two poly levels. This circuit is primarily intended to use it in portable applications. A 1.5V battery supplies the proposed circuit, which allows obtaining a ×2-voltage generator. In order to minimize the effect of parasitic capacitors, external capacitors with high capacitance and low ESR were selected. The difference between deduced equations and TSpice simulation for V_{OUT} was less than 30mV (which is about 1% of difference). This design is easily extender to develop higher voltage generators.

Acknowledgments. One of the authors, E.V.C. thanks the scholarship given by CONACyT-México. The financial support from CONACyT-México (under grant 38951-A) is gratefully appreciated.

References:

[1] P. J. García-Ramírez, F. Sandoval-Ibarra, "Measuring Magnetic Fields at Low Temperature", Proc. of the 4th Electronic Circuits and Systems Conference ECS'03, pp. 143-146,September 11-12, 2003, Bratislava, Slovakia

[2] F. Sandoval-Ibarra, E. J. Vargas, J. A. Herrera and J. M. González, "The Linear Differential Pair: A Case of Study", PROC. OF THE International Conference on Electronic Design, Nov. 17-19, Veracruz, Mexico, 2004

[3] F. Sandoval-Ibarra, R. Rodríguez-Calderón, "Explaining the Unexpected Performance of a Switched-Current ΣΔ Modulator", Proc. of the 4th Electronic Circuits and Systems Conference ECS'03, pp. 127-130, September 11-12, 2003, Bratislava, Slovakia

[4] E. Montoya-Suárez y F. Sandoval-Ibarra, "A Review of VCO's, X Workshop IBERCHIP, March 10-12, Cartagena, Colombia, 2004 (in Spanish)

[5] J.O. Cano-Gómez and F. Sandoval-Ibarra, " The CMOS Class-E Amplifier ", Proc. of the 4th Int. Congress on Electric and Electronics Engineering Research, Nov. 15-19, Aguascalientes, Mexico, 2004

[6] Alexandre Ternes Behr *et al*, "Harmonic Distortion Caused by Capacitors Implemented with MOSFET Gates", IEEE. Solid-State Circuits, vol. 27, no. 10, pp. 1470-1475, 1992

[7] Louis S. Y. Wong *et al*, "A Very Low-power CMOS Mixed-Signal IC for Implantable Pacemaker Applications", IEEE J. of Solid-State Circuits, vol. 39, No. 12, pp. 2446-2455, 2004

[8] Robert W. Brodersen, Paul R. Gray, and David A. Hodges, "MOS Switched-Capacitor Filters", Proc. IEEE, vol. 67, pp. 61-75, 1979

[9] Baker R. Jacob, "CMOS circuit design, layout, and simulation", IEEE PRESS, pp. 384-386, Psicataway, NJ USA, 1998.

[10] J. Silva-Martínez, "A Switched capacitor Double Voltage Generator", Proc. of the IEEE Midwest Symposium on Circuits and Systems, pp. 177-180, Laffayette USA, 1994