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Performance Evaluation of Manchester Carry Chain Adder for VLSI Designer Library

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Abstract: - Adder is the most extensively used component in any VLSI designer library. Thus it is necessary to design a fast and have a constant rise, fall and delay time. The Manchester carry chain adder is chosen because it is fast and give a constant rise, fall and delay time for all the sum and carry output signals compare to other adders, regardless the number of bits. The simulations were done for all types of Manchester adder to determine the Manchester carry chain adder circuitry that provides the best performances. Tanner Tools Pro is used to analyse the Manchester carry chain adder with 2-micron technology and the channel length, L=2µm. T-spice and W-edit are used for circuit analysis. The exhaustive test for the 2-bit Manchester adder proves that the dynamic stage of the Manchester carry chain adder gives constant rise, fall and delay time for the carry and sum outputs with maximum frequency of 125MHz.

Key-Words: - Manchester carry chain adder, VLSI design, VLSI designer library, MOS

1 Introduction

An adder is a LSI circuit, which forms the sum of two binary numbers. Two output variables are required to specify the addition output, the sum and carry. Addition forms the basic for many processing, from counting to multiplication to filtering. As a result, adder circuits that add two binary numbers are the great interest to the digital system designers.

A wide variety of adder implementations are available to serve different speed/density requirements. Various adders have been investigated by many researchers [1], [2], [3], [4], [5] and assumed all adder cells were implemented with static (restoring) logic. Therefore, the ripple-carry propagation delay was linearly proportional to the size of a block. This is in contrast to a more popular adder implementation in VLSI: the Manchester adder using precharge logic [6], [7], [8] in which the ripple-carry propagation delay is proportional to the *square* of the size of a block.

Computers and calculators perform the addition operation on two binary numbers at a time, where each binary number can have several binary digits. The addition process starts by adding the least significant bit (LSB) of the augend and addend. The carry output must be added to the next position along with the augend and addend in that position. The same process is repeated until all the positions are added. Three bits, the augend bit, the addend bit and a carry bit from previous position will be added at each addition process.

The sum and the carry outputs of a full adder are represented by the equations below.

$$Sum,\ S = A \oplus B \oplus C$$

$$Carry,\ C = AB + C(A + B)$$

The gate level schematic for the direct implementation of Sum and Carry is shown in Fig 1.

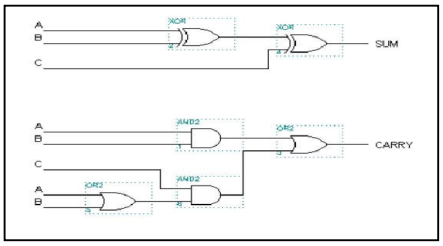

Fig 1: Full adder for Sum and Carry

The Manchester adder stage improves on the carry lookahead implementation by using a single C_3 gate. Three circuits are selected as the model for the Manchester carry chain adder. Two dynamic stage Manchester carry chain adder and a static stage Manchester carry chain adder, as shown in the Fig 2, 3 and 4. Generate, G, propagate signal, P and Sum output, S for the 2nd and 3rd circuits is shown in Fig 5. The A and B are the input signals and C_{i-1} is the carry input

The output node is pre-charged by the p pull-up transistor when the CLK is low for dynamic stage Manchester carry chain adder. The n pull-down transistor turns on when the CLK goes high. If generate (A.B) is true, then the output node is discharged. If propagate (A+B) is true, then a previous carry may be coupled to the output node, conditionally discharging it. Note that the CARRY is actually propagated.

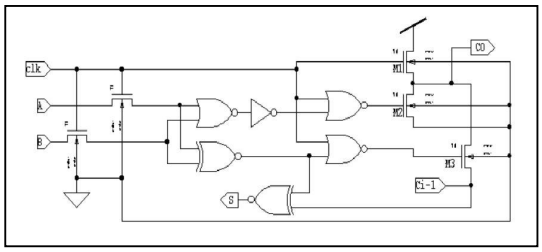

Fig 2: 1st Dynamic stage Manchester adder

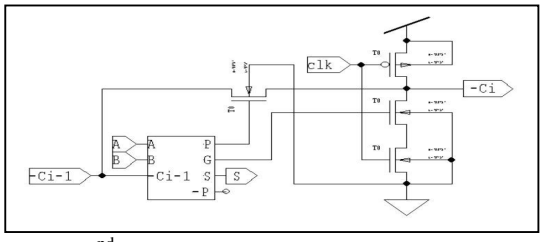

Fig 3: 2nd Dynamic sage Manchester carry chain adder

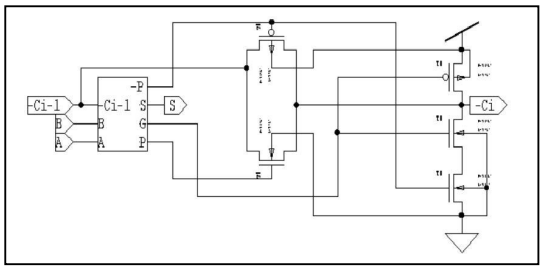

Fig 4: 3rd Static stage Manchester carry chain adder

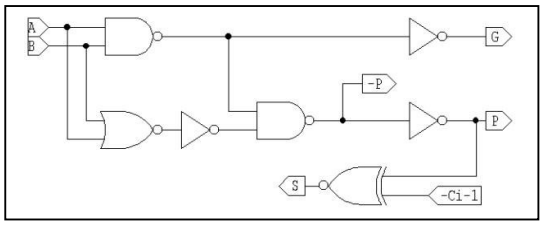

Fig 5: Generate, G, Propagate, P and Sum output, S

Tanner Tools Pro is used for simulation analyse. The circuits are constructed by S-edit using CMOS (Complementary MOS) technology. The standard CMOS (SCMOS) gates with 2-micron technology which means the length of the CMOS, L=2µm, is used for the simulation. The schematics are converted to text by using T-spice to add the parameters and command for transient analysis. The output waveform is shown by using W-edit for performance analysis between the Manchester adders.

2 Performance Analysis

The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance, C_L. An input transition results in the output transition that either charges C_L toward V_{DD} or discharges toward V_{SS}. The performance analysis is mainly focused on rise time, fall time and delay. Rise time is the time for a waveform to rise from 10% to 0% of its steady state value. Fall time is the time for a waveform to fall from 90% to 10% of its steady state value. Delay is the time difference between the input transition (50%) and the 50% of the output level.

Simulation was done concentrating on a single bit Manchester carry chain adders. All the three Manchester adders are tested for the functional and performance analysis. The tests are concentrated on delay, rise and fall time for the Manchester carry chain adder outputs, Sum, S and carry output, C_i. A capacitive load like inverter or buffer is added to test the charging and pre-charging time. The 50MHz clock pulse with 1ns for the rise and fall time is used for the dynamic stage Manchester adder. The truth table for the single-bit of 1st Manchester adder is shown in Fig 6 and the simulation output is shown in Fig 7.

The simulation results are shown in Fig 8. The simulation results show that the 1st dynamic stage Manchester carry chain adder gives better performance compared to the other Manchester adder. The 1st dynamic stage Manchester carry chain adder is used to develop the adder for VLSI designer library.

	clk	C_{i-1}	A	B	-G	-P	C_i	S
Propagate C_{i-1}	0	0	0	0	0	1	0	0
	0	0	0	1	1	0	0	1
	0	0	1	0	1	0	0	1
Generate C_i	0	0	1	1	1	1	1	0
Kill C_{i-1}	0	1	0	0	0	1	0	1
Propagate C_{i-1}	0	1	0	1	1	0	1	0
	0	1	1	0	1	0	1	0
	0	1	1	1	1	1	1	1
Pre-charging	1	0	0	0	0	1	1	0
	1	0	0	1	1	0	1	1
	1	0	1	0	1	0	1	1
	1	0	1	1	1	1	1	0
	1	1	0	0	0	1	1	1
	1	1	0	1	1	0	1	0
	1	1	1	0	1	0	1	0
	1	1	1	1	1	1	1	1

Fig 6: Truth table for Dynamic stage Manchester adder

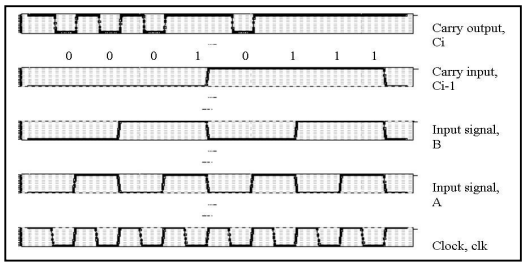

Fig 7: Simulation outputs for Dynamic stage Manchester adder.

The 1st dynamic stage Manchester carry chain adder is cascaded to form a 2-bit Manchester adder as shown in Fig 9. Exhaustive test is implemented for the simulation of 2-bit Manchester adder with 3 sets of input data, A_1A_0, B_1B_0 and C_0. The adding operation for LSB input signals is shown in equation below; with S_1 is the sum output and C_1 is the carry output of the LSB signals.

$$A_0 + B_0 + C_0 = C_1S_1$$

C_1 is added to MSB signals as carry input for MSB and with sum output, S_2 and carry output, C_2.

$$A_1 + B_1 + C_1 = C_2S_2$$

	Average (ns)	1st Dynamic Manchester adder	2nd Dynamic Manchester adder	3rd Static Manchester adder
Carry output, C_i	Rise time	0.9250	1.5333	0.8800
	Rise time delay	0.4075	1.2867	1.0500
	Fall time	0.4450	0.7467	0.9800
	Fall time delay	0.7475	0.7067	1.5650
Sum output, S	Rise time	1.2900	2.0900	1.9800
	Rise time delay	2.0433	2.3333	2.3167
	Fall time	0.9600	0.8933	0.8867
	Fall time delay	1.7233	1.3300	1.4033

Fig 8: The simulation results of the three-type single bit Manchester carry chain adders

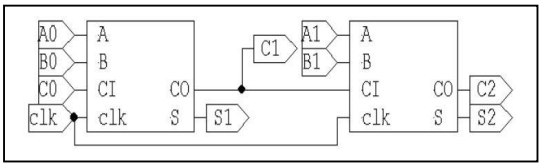

Fig 9: 2-bit dynamic stage Manchester adder

Clock pulse with frequency 50MHz is used for the simulation analysis. The 2-bit Manchester carry chain adder performs the correct functional operation. The simulation output is shown in Fig 10. The maximum time difference of rise time, fall time and delay between carry outputs C_1, C_2 and sum output, S_1, S_2 is not more than 0.5ns. The 2-bit Manchester adder gives constant rise time, fall time and the delay for the carry output signals C_1 and C_2. The worst case for rise time delay average is 2.0375ns and fall time delay is 1.8558ns. Total delay is 2.0375ns+1.8558ns equal to 3.8933ns. The clock signal with period is 8ns (f=125MHz), which is 2 times of the delay, can be used as input clock signal for the dynamic stage Manchester carry chain adder.

The 4-bit dynamic stage Manchester carry chain adder with bypass circuit is constructed as shown in Fig 11. Few sets of data as shown in Fig 12 are used for the simulation analysis. The simulation results are summarized as shown in Fig 13. The clock with frequency of 50MHz is used for the simulation analysis.

The simulations are continued with a 4-bit Manchester carry chain adder without the bypass circuit to compare the performance of the adder. It performs the correct functions as a Manchester adder but with one difference, which is the output of the carry output signal, CO as shown in Fig 14. The performance of the circuit is shown in Fig 15. The overall performance of the 4-bit Manchester adder without bypass circuit is better than the Manchester adder with bypass circuit. The bypass circuit is used to bypass the worst-case propagation time of the four stages if all carry-propagate signals are true.

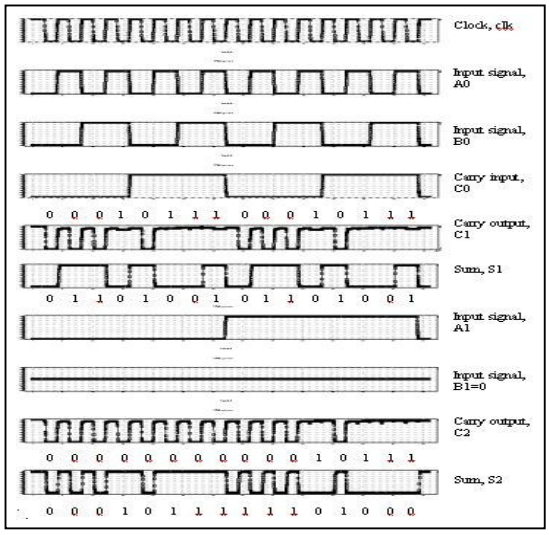

Fig 10: Simulation output of 2-bit Manchester adder

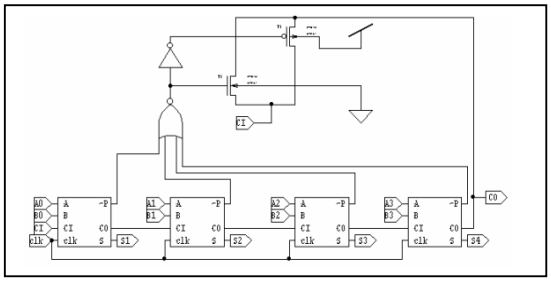

Fig 11: 4-bit dynamic stage Manchester adder with bypass circuit

Carry input, CI	A	$A_3A_2A_1A_0$	B	$B_3B_2B_1B_0$	Output	$C_oS_4S_3S_2S_1$
1	0	0000	0	0000	1	00001
1	15	1111	0	0000	16	10000
1	1	0001	15	1111	17	10001
0	14	1110	0	0000	14	01110
0	9	1001	12	1100	21	10101
1	6	0110	3	0011	10	01010
1	5	0101	10	1010	16	10000

Fig 12: Data used for 4-bit Manchester adder simulation analysis

Average time	Rise time, t_R(ns)	Rise time delay, t_{RD}(ns)	Fall time, t_F(ns)	Fall time delay, t_{FD}(ns)
C1	1.5147	0.7140	0.6969	1.0331
C2	1.0910	0.4805	0.4650	0.9095
|C1-C2|	0.4237	0.2335	0.2319	0.1236
S1	0.9167	2.0375	0.8000	1.8558
S2	1.0522	1.9339	0.8128	1.3844
|S1-S2|	0.1355	0.1036	0.0178	0.4714

Fig 13: Rise, fall and delay time differences between C_1, C_2 and S_1, S_2.

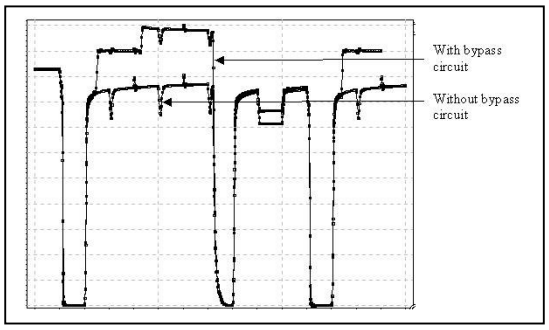

Fig 14: The output difference of CO for Manchester adder with and without bypass circuit

Output signal	Rise time, t_R(ns)	Rise time delay, t_{RD}(ns)	Fall time, t_F(ns)	Fall time delay, t_{FD}(ns)
Sum, S1	0.49	2.67	0.75	2.07
	1.77	2.52	0.75	0.71
	0.58	3.21	0.62	0.20
Sum, S2	1.93	2.05	0.71	1.57
	0.68	1.52	0.71	0.68
			1.26	1.94
Sum, S3	2.04	2.79	0.70	1.57
	1.80	1.96	0.72	0.67
	0.60	3.21	0.71	0.67
Sum, S4	1.90	3.16	0.71	1.58
	0.47	1.20	0.74	0.65
Carry output, CO	0.58	0.32	0.43	0.69
	0.65	0.29	1.45	1.94
	0.62	0.33	0.39	0.65

Fig 15: The performance of 4-bit Manchester adder without bypass circuit.

3 Discussion

Three types of Manchester carry chain adder are selected for the VLSI designer library. The adders are simulated using 2-micron technology. Exhaustive test is performed for 2-bit addition operation using clock with 50MHz. The performance analysis is mainly targeted on the rise time, fall time and the delay of the output carry and sum signals. The 1st dynamic stage Manchester adder gives best performance compare to the other adders as shown in Fig 8. The 1st dynamic stage Manchester adder is selected for the VLSI designer library. The simulation is carry on by 4-bit Manchester carry chain adder using the 1st Manchester adder.

4 Conclusion

Two approaches are targeted in this simulation. The 1st approach is with the bypass circuitry for the MSB carry output signal and the second approach is without the bypass circuitry. The 2nd approach gives better performance compare to the 1st approach. The 1st approach is recommended for addition operation that is more than 4-bits. The 2nd approach is used for 4-bits addition operations.

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