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Modeling of Conduction and Switching Losses in Three-Phase Asymmetric Multi-Level Cascaded Inverter

M. G. Hosseini Aghdam, S. H. Fathi

***Abstract*--The designer of power converters must model the losses of converter switches to optimize the performance of system. This paper is focused on a model of a three-phase asymmetric multi-level cascaded inverter losses using switching function concept. The suggested model is based on the semiconductor characteristics. Simulation results are shown the simplicity, convergence, and reliability of the suggested model.**

***Index Terms*--**Three-Phase Asymmetric Multi-level Cascaded Inverter, Switching Function, Conduction Losses Switching Losses.

I. INTRODUCTION

SINCE SEVERAL YEARS, there is a growing demand for high voltage conversion systems capable of providing high output voltage signals and having good spectral performance and easy control. Examples of such as systems are FACTS devices, HVDC light transmission, AC drives, and active filters [1, 2].

In all the well-known multi-level inverter topologies, the number of power devices required depends on the output voltage level needed. However, increasing the number of power semiconductor switches also increase inverter circuit, control complexity and cost. To provide a large number of output levels without increasing the number of inverters, asymmetric multi-level inverters can be used [2].

The basic elements used in asymmetric multi-level inverter are IGBTs and diodes. Because of economical and technical importance of power dissipation, the designers must consider and minimize the losses of these devices. The losses of a switching device can be classified in three groups: off-state, conduction, and switching losses. The leakage current during the off-state is negligibly small therefore the power losses during this state can be neglected. As a result, only conduction and switching losses must be exactly modeled [1, 3, 4, 5].

There are several methods to model these losses. In the case of modeling with Pspice and Saber, the inverter circuits can be schematically expressed by using actual power semiconductor device models and passive elements [1, 6]. These models have shown a number of problems, such as complexity, slow execution times, large amount of generated data, and convergence [1, 6]. To overcome the mentioned limitations, switching function concept has been developed [6].

In this paper, for a three-phase asymmetric multi-level cascaded inverter system the modeling methods of conduction and switching losses based on switching function concept are presented.

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II. ASYMMETRICAL MULTI-LEVEL INVERTER

Asymmetric multi-level inverters have exactly the same circuit topology as *symmetric* multi-level inverters. They differ only in the used *capacitor voltages*. The properties of asymmetric multi-level inverters are however quite different from those of their symmetric versions. Especially the number of output-voltage levels can be dramatically increased [2].

Figure 1 shows a phase circuit diagram of an asymmetric nine-level cascaded inverter.

A number of modulation strategies are used in multi-level power conversion applications. They can generally be classified into three categorize: Multi-step, Space Vector PWM (SVPWM), and Carrier-Based PWM (CBPWM) [1].

This paper focuses on carrier-based PWM (CBPWM) techniques which have been extended for use in multi-level topologies by using multiple carriers.

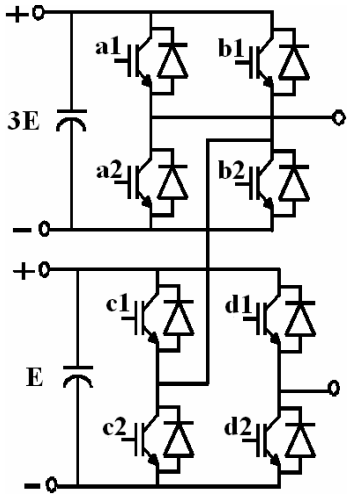


Fig. 1. Phase circuit diagram of an asymmetric nine-level cascaded inverter.

The phase disposition (PD) PWM method as one of the CBPWM methods is based on a comparison of a sinusoidal reference waveform, with vertically shifted carrier waveforms. The PD PWM method uses *N-1* carrier signals to generate the *N*-level inverter output voltage. As it can be seen in figure 2, the carrier signals have the same amplitude A_c and the same frequency f_c and are in phase. The sinusoidal reference wave has a frequency f_r and an amplitude A_r. At each instant, the result of the comparison is decoded in order to generate the correct switching function corresponding to a given output voltage level.

Since there are no redundant output states in a two-cell asymmetric nine-level inverter, the relation between the output and the cell states is unique. As an example, the main- and sub-inverter output voltages are shown in figure 3, for the same PD PWM signals as in four-cell symmetric nine-level inverter.

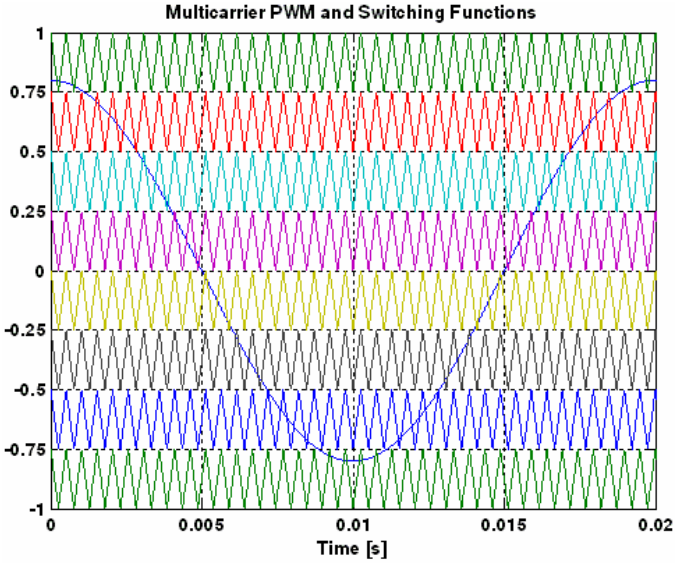


Fig. 2. Reference signal and triangular carriers of an asymmetric nine-level cascaded inverter with the PD PWM control strategy.

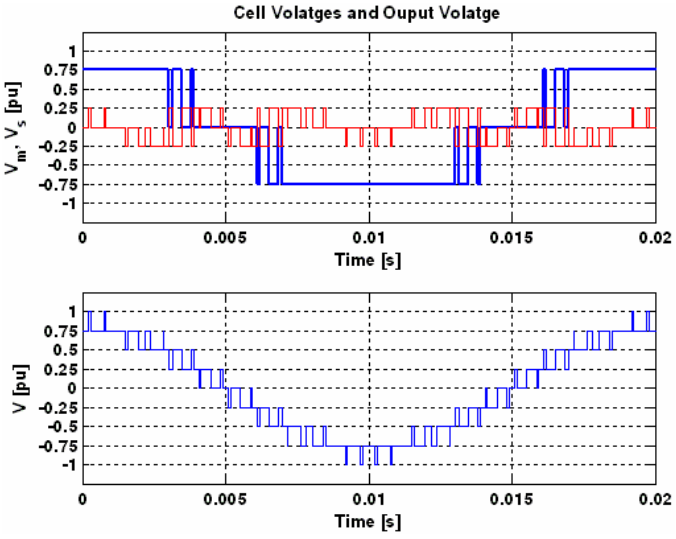


Fig. 3. Cell voltages V_m, V_s and output voltage V of an asymmetric nine-level cascaded inverter.

III. Functional Model

In order to define switching functions, a switching control strategy must be selected. In this paper, the PD PWM control strategy is selected as a control strategy (figure 2). Based on the PD PWM control strategy figure 4 shows the four switching functions (SF_{a1}, SF_{b2}, SF_{c1}, SF_{d2}).

Figure 5 shows the functional model of three-phase asymmetric multi-level cascaded inverter. This model consists of five functional blocks based on the switching functions SF_{a1}, SF_{b2}, SF_{c1}, and SF_{d2}.

As it can be seen in figure 5, the phase and line-to-line voltages are obtained from block 1. Assuming a balanced R-L load, the load currents (I_a, I_b, I_c) are derived as ratio of the phase voltages and respective impedance as

$$I_{an} = \frac{V_{an}}{Z_a} = \frac{V_{an}}{R + j\omega L}$$
$$I_{bn} = \frac{V_{bn}}{Z_b} = \frac{V_{bn}}{R + j\omega L} \quad (1)$$
$$I_{cn} = \frac{V_{cn}}{Z_c} = \frac{V_{cn}}{R + j\omega L}$$

Then, the switch currents (I_{a1}, I_{b2}, I_{c1}, I_{d2}) for each phase can be calculated of the load current with the corresponding switching functions SF_{a1}, SF_{b2}, SF_{c1}, and SF_{d2}, that is,

$$I_{a1} = I_a.SF_{a1}$$
$$I_{b2} = I_a.SF_{b2} \quad (2)$$
$$I_{c1} = I_a.SF_{c1}$$
$$I_{d2} = I_a.SF_{d2}$$

In order to calculate the current rating of the power semiconductor switch (I_{a1}), one needs the information for the pure switch current and the pure diode current. The switch current (I_{a1}) can be determined as follows

$$I_{a1} = I_{a1-S} - I_{a1-D} \quad (3)$$

where $I_{a1\text{-}S}$ and $I_{a1\text{-}D}$ are the pure switch current and the pure diode current of the switch *a1*, respectively.

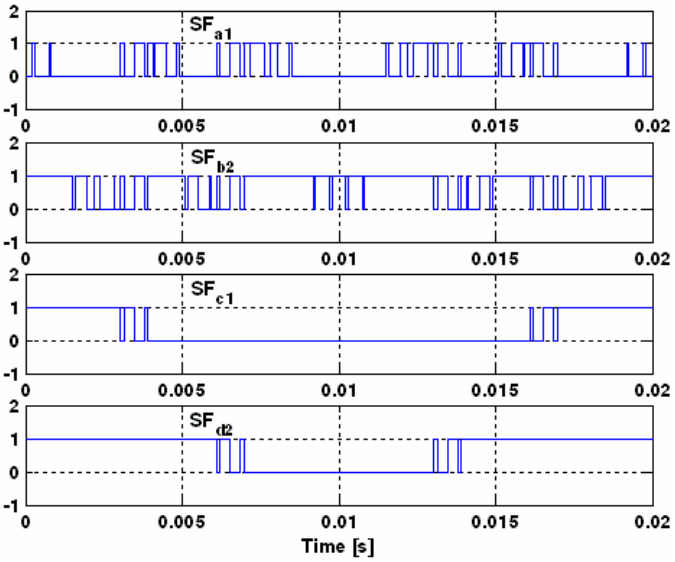


Fig. 4. Switching functions with the PD PWM control strategy for phase *A*.

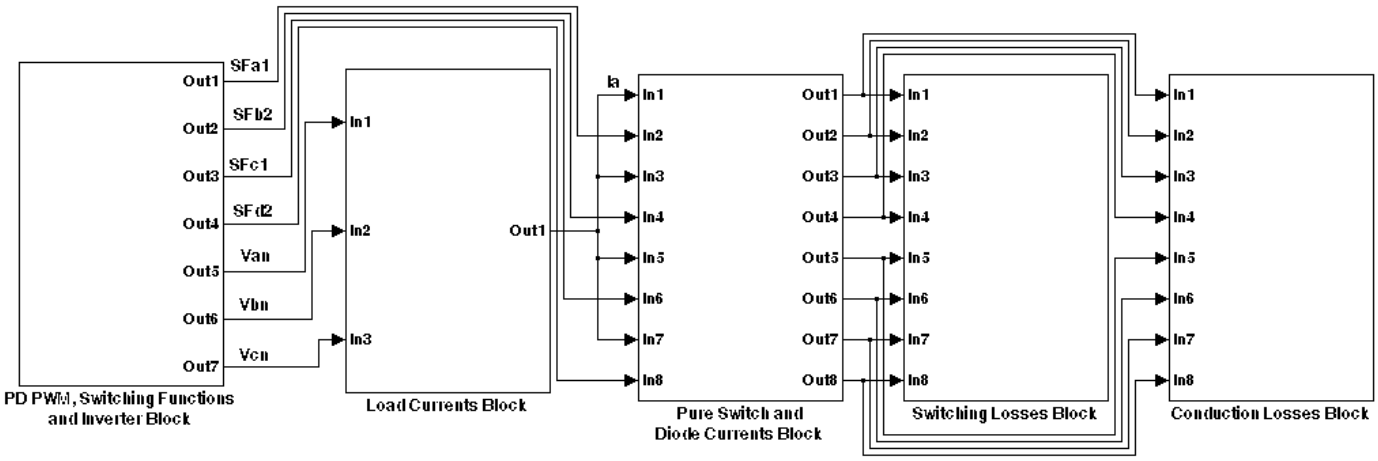


Fig. 5. The model of three-phase asymmetric multi-level cascaded inverter.

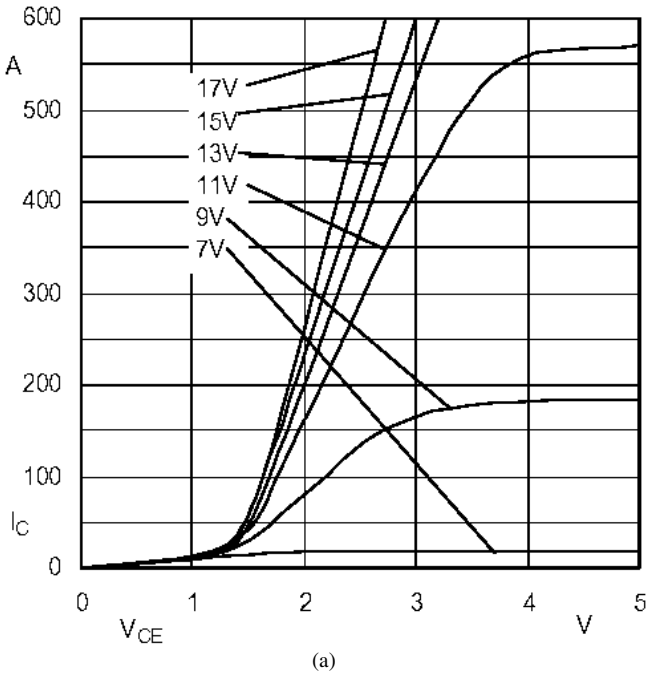
IV. Conduction and Switching Losses

The conduction losses are computed by multiplying the on-state voltage by the on-state current. The on-state voltage is a function of switch current, gate voltage of IGBT, and etc.

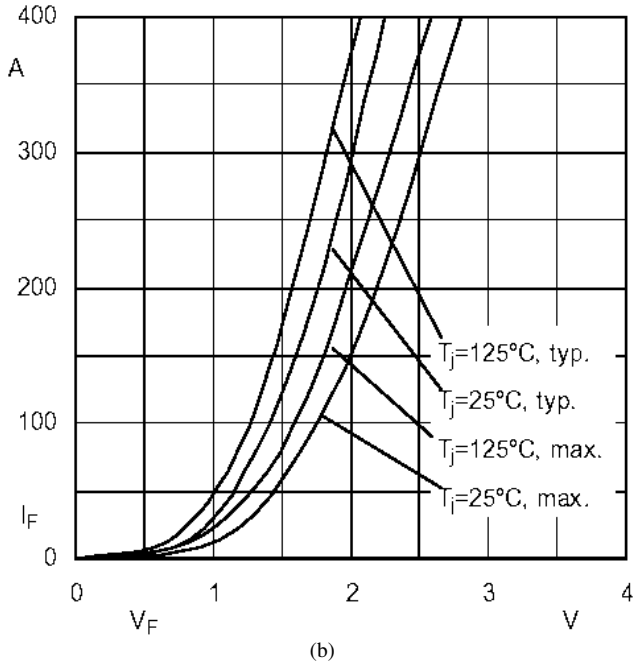
Figure 6 (a) shows the collector current versus collector-emitter voltage of IGBT (SKM 400 GB 124D [7]). Figure 6 (b) shows the *V-I* characteristic of the diode. These curves can be approximated by the following equations

$$V_{CE} = \begin{cases} 0.06I_C & I_C < 20\,A \\ 0.01I_C + 1 & 20\,A < I_C < 50\,A \\ 0.0027I_C + 1.365 & I_C > 50\,A \end{cases} \quad (4)$$

$$V_D = \begin{cases} 0.1I_D & I_D < 7\,A \\ 0.0066I_D + 0.6537 & 7\,A < I_C < 75\,A \\ 0.0029I_D + 0.94 & I_C > 75\,A \end{cases} \quad (5)$$



(a)



(b)

Fig. 6. (a) V_{CE}-I_C characteristic of IGBT. (b) *V-I* characteristic of diode.

The most accurate method of switching losses calculation is the current and voltage waveforms determination during transitions. The point by point multiplication of these curves results in the accurate data [3]. The area under the power waveform is the switching energy at turn-on or turn-off transitions. Figure 7 (a) and (b) show the switching energy versus switch current for IGBT and diode, respectively (SKM 400 GB 124D [7]). These curves are approximate by

$$E_{on-switch} = 0.00021I_S^2 + 0.497I_S + 6.4364 \quad (6)$$

$$E_{off-switch} = 0.1309I_S^2 + 3.8182 \quad (7)$$

$$E_{rec-diode} = 0.0001I_D^2 + 0.073I_D + 0.2111 \quad (8)$$

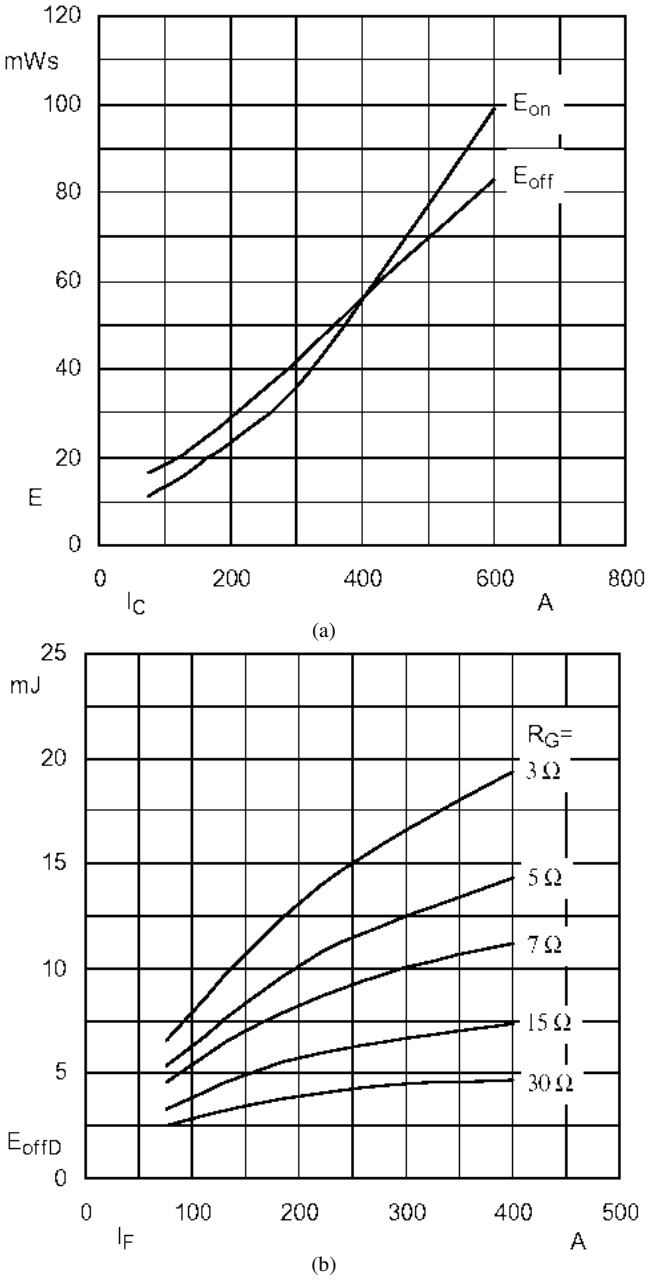


Fig. 7. (a) IGBT turn-on/turn-off energy. (b) Diode turn-off energy.

V. Simulation Results

The proposed model for asymmetric nine-level cascaded inverter is simulated using MATLAB Simulink. The simulation parameters are as follows:

Supplying voltages: V_{d1}=50*V and* V_{d2}=150*V*,

Load: R=5 Ω and L=20 *mH*,

Reference signal frequency (f_r): 50 *Hz*,

Carrier signals frequency (f_c): 1.95 *kHz*

Modulation index (M_a=A_r/A_c) =0.8 and

IGBT type: SKM 400 GB 124D [7].

Figure 8 shows voltage and current waveforms. Figures (8) a, b, and (c) are phase voltage (V_{an}), line-to-line voltage (V_{ab}), and balanced load currents (I_a, I_b, I_c), respectively.

Based on the switching function signals SF_{a1}, SF_{b2}, SF_{c1}, and SF_{d2}, the switch currents I_{a1}, I_{b2}, I_{c1}, and I_{d2} can be successfully derived from pure current generator block as shown in figure 9.

Then using the equation of (3), the switch currents are divided into the pure switch currents ($I_{a1\text{-}S}$, $I_{b2\text{-}S}$, $I_{c1\text{-}S}$, $I_{d2\text{-}S}$) and the pure diode currents ($I_{a1\text{-}D}$, $I_{b2\text{-}D}$, $I_{c1\text{-}D}$, $I_{d2\text{-}D}$) as shown in figures 10 and 11 for switches of *b2*, and *d2*.

Figures 12-15 present the asymmetric nine-level cascaded inverter losses based on equations (4)-(8). Figures (12) and (14) (a), (b) show the IGBT and diode conduction losses, respectively. Figures (13) and (15) (a), (b), (c) show the IGBT turn-on switching losses, IGBT turn-off switching losses, and diode turn-off switching losses, respectively.

The suggested model for conduction and switching losses is very accurate. Therefore, in order to select the proper power semiconductor devices for asymmetric multi-level inverter, the suggested model is very reliable and safe. Also, the simulation run-time measured of the suggested model is 100 times faster than the ordinary method or Pspice simulation model. Also, this developed model solves the problems such as convergence and complexity of circuit and control.

VI. Conclusion

Based on switching function concept, the losses of three-phase asymmetric nine-level cascaded inverter have been modeled with the using of MATLAB Simulink.

The suggested model is based on IGBT and diode characteristics modeling. Therefore, the calculation of conduction and switching losses by using this model is very accurate. Also, In order to select the proper power semiconductor devices for asymmetric multi-level inverter, the suggested model is very reliable and safe. Also, this model is simple and has a short run-time of simulation, too.

VII. References

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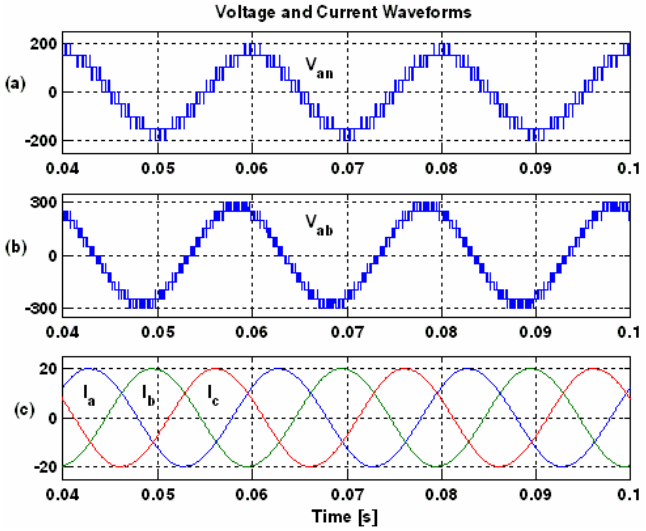

Fig. 8. Voltage and current waveforms of asymmetric nine-level cascaded inverter with the PD PWM control strategy. (a) Phase voltage (V_{an}). (b) Line-to-Line voltage (V_{ab}). (c) Load currents (I_a, I_b, I_c).

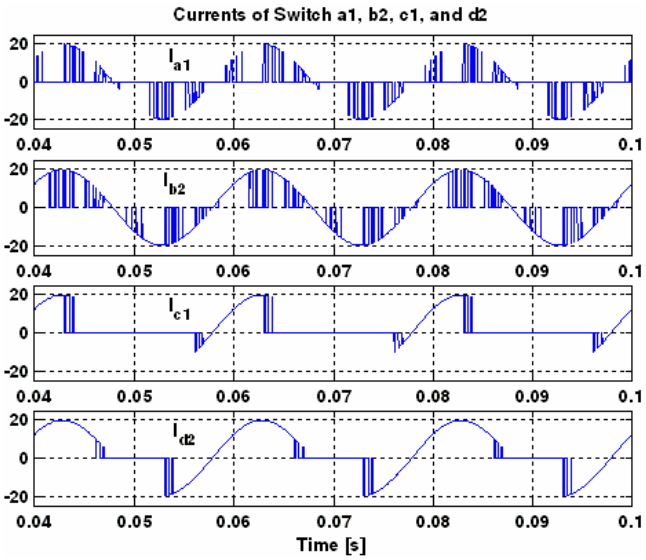

Fig. 9. Current waveforms of switches *a1*, *b2*, *c1*, and *d2*.

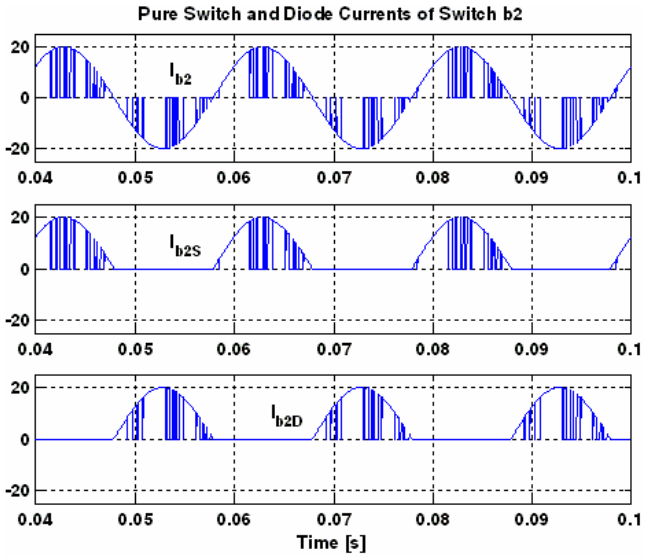

Fig. 10. Current of switch *b2* (I_{b2}), pure switch current of switch *b2* (I_{b2S}), and pure diode current of switch *b2* (I_{b2D}).

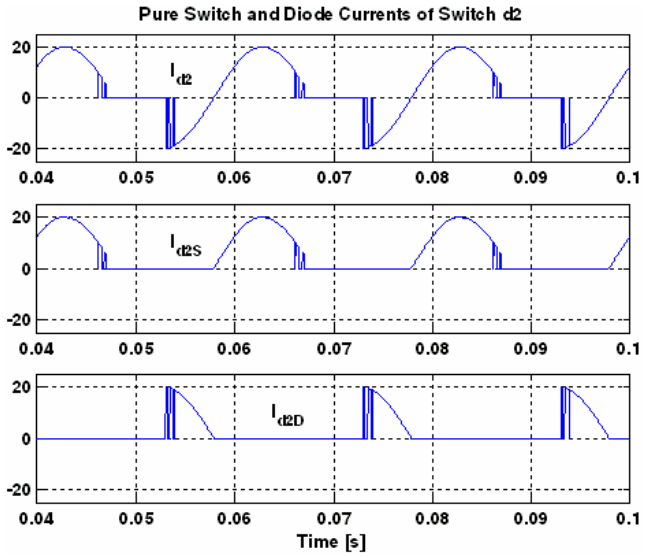

Fig. 11. Current of switch *d2* (I_{d2}), pure switch current of switch *d2* (I_{d2S}), and pure diode current of switch *b2* (I_{d2D}).

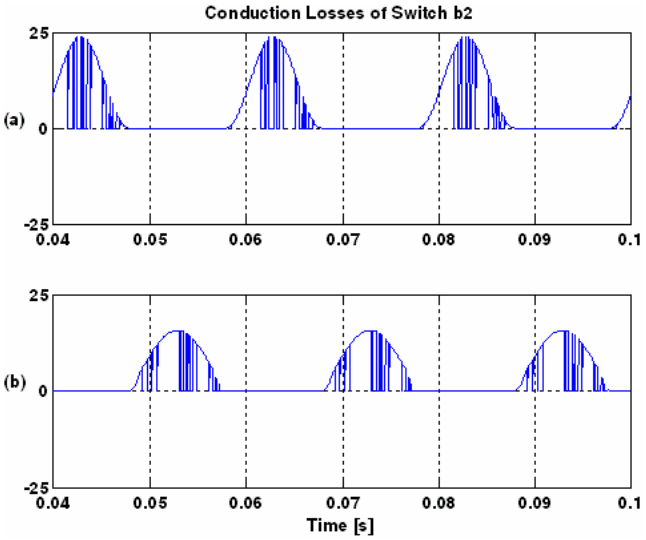

Fig. 12. Conduction losses of switch *b2*. (a) IGBT conduction losses [*mJ*]. (b) Diode conduction losses [*mJ*].

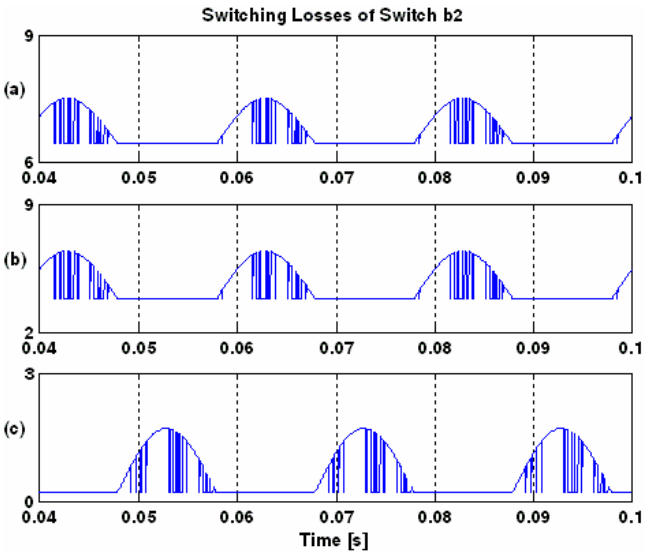

Fig. 13. Switching losses of switch *b2*. (a) IGBT turn-on switching losses [*mJ*]. (b) IGBT turn-off switching losses [*mJ*]. (c) Diode turn-off switching losses [*mJ*].

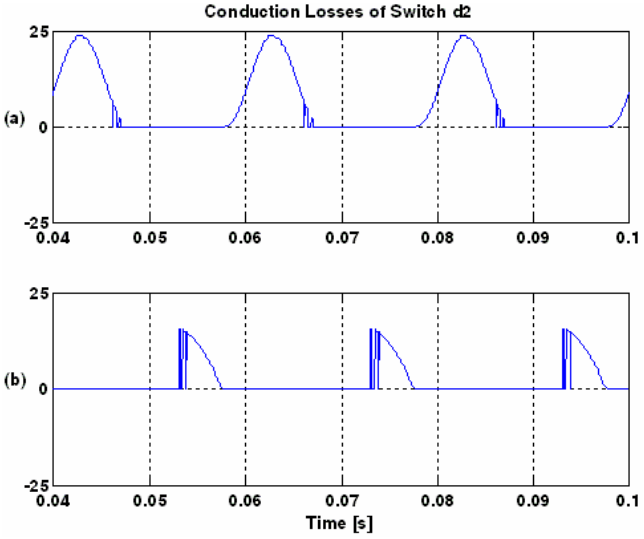

Fig. 14. Conduction losses of switch *d2*. (a) IGBT conduction losses [*mJ*]. (b) Diode conduction losses [*mJ*].

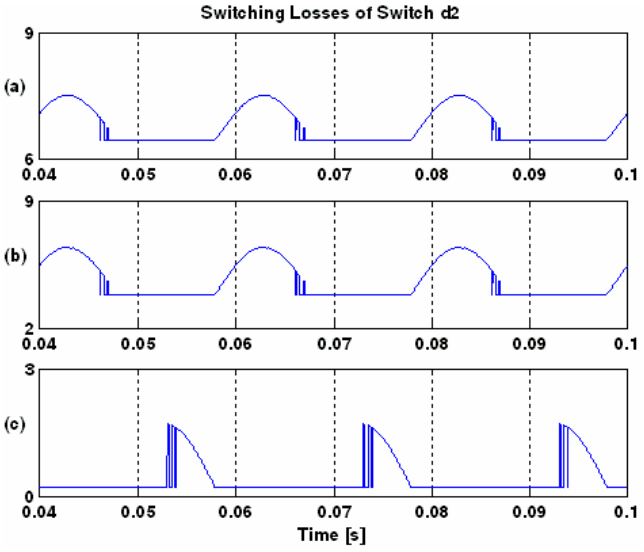

Fig. 15. Switching losses of switch *d2*. (a) IGBT turn-on switching losses [*mJ*]. (b) IGBT turn-off switching losses [*mJ*]. (c) Diode turn-off switching losses [*mJ*].