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EXPERIMENTAL VERIFICATION OF A SPACE VECTOR MODULATION TECHNIQUE FOR NPC INVERTERS

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Abstract: - The paper analyses and experimentally verifies two different modulation strategies based on a Space Vector Modulation (SVM) technique, specifically designed for three-phase Neutral Point Clamped (NPC) inverters. Proposed technique was designed to maintain, also in NPC inverters, all the advantages of SVM used in traditional two-level inverters. The employment of two different modulation strategies, when different operating conditions occurs, allows the improvement of the harmonic content of the output currents produced by NPC inverters. After a detailed description of the Space Vector Modulation technique, the two modulation strategies are compared by the means of some significant experimental results.

Key-Words: - NPC Inverter, Modulation technique, High power converters, Traction locomotives.

1 Introduction

Neutral Point Clamped (NPC) inverters are quite popular for high power electronics applications because they halve the maximum voltage drop on their power devices and furnish a three-level output voltage, improving the current tracking accuracy in current control loops. Moreover, they produce a better harmonic content of the output current than traditional two-level Voltage Source Inverter (VSI), allowing a torque ripple reduction. The main drawbacks of NPC inverters consist on doubling the number of switching devices, respect to two-level VSI, and on employing an opportune strategy to maintain balanced the neutral point voltage, when a single DC supply voltage is used.

Generally, the most used control techniques for NPC inverters are Hysteresis, Sinusoidal PWM (SPWM) and Space Vector (SVM) modulation. The first one was widely investigated in [3-5] by authors that made a comparison between different hysteresis modulation techniques for NPC inverters, and presented a suitable experimental system [5], based on a microcontroller and a Programmable Logic Device. Hysteresis control techniques, which require a closed-loop control of the inverter phases current, give fast response, good accuracy and, in many cases, do not require any knowledge of the load parameters. However, the current waveform is not only determined by the hysteresis characteristics, but depending on the operating conditions, the current slope may widely vary and the current peaks may appreciably exceed the limits of the hysteresis band.

SPWM modulation techniques [6, 12], widely used in industrial application, are based on the comparison, separately for each inverter phase, between suitable carrier signals, generally triangular waveforms, and sinusoidal signals, representing the desired output voltages. Therefore, the commutation instants of the inverter power devices are determined by the comparators outputs, e.g. from the intersections of the signals applied to the comparators. Moreover, if a linear voltage regulation is required, the amplitude of the modulating signal cannot exceed the amplitude of the carrier. This limitation restricts the voltage regulation range. SVM techniques [7-12], instead, determine the modulated waveforms taking into account simultaneously the desired voltage for all the inverter phases. Such techniques, generally more suitable for microcontroller implementation, permit to extend significantly the voltage regulation range respect to that obtained by SPWM.

In recent papers [11, 12], the authors presented an interesting SVM technique based on a six hexagons subdivision of the three-phase plane. The proposed technique preserves the advantages of the traditional SVM; to this aim, all the commutations happen only between adjacent states, so that, during each modulation interval, only three commutations occur.

After a brief overview on NPC inverters behaviour, present paper describes the previously developed

SVM technique designed for NPC inverters and proposes a suitable modification of the modulation procedure to improve the harmonic content of the output currents. Finally, experimental results, obtained by a laboratory prototype, are presented.

2 NPC INVERTERS

NPC inverters, as shown in Fig. 1, are built-up of twelve switches, each one with its freewheeling diode, and six power diodes, allowing the connection of the phases outputs to the middle voltage ($V_{dc}/2$). If only one voltage supply line V_{dc} is used, the drop voltages on the two capacitors can assume different values. As consequence, if an incorrect voltage balance between the capacitors occurs, an average value different from $V_{dc}/2$ is produced on the phase outputs.

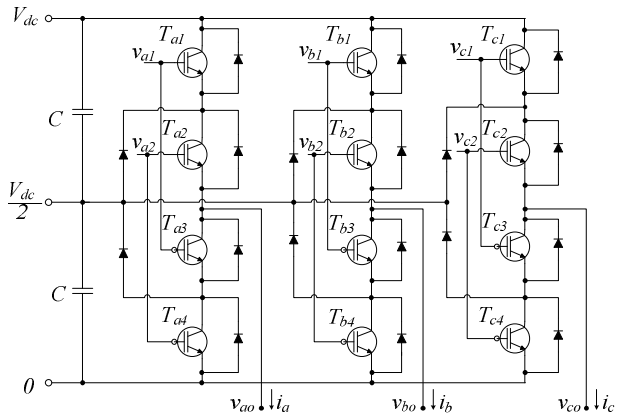

Fig. 1 - NPC inverter circuit.

T_{p1}	T_{p2}	T_{p3}	T_{p4}	v_{po}
0	0	1	1	0
0	1	1	0	$V_{dc}/2$
1	1	0	0	V_{dc}

Table 1 - Driving Logic Signals.

The problem of middle voltage balance, widely discussed in literature [2], can be solved applying suitable modifications to the modulation strategy, as shown also in [9]; for traction drives it is also possible, as considered in this paper, to use two series-connected AC/DC converters, whose independent control loops assure the balanced subdivision of the supply voltage [1]. NPC inverters operate, as highlighted in Fig.1, so that, at every time instant, two switches of each phase are closed whilst the other two are opened. The allowed logic configurations of NPC switches that are able to connect the load to a supply voltage are listed in Table 1, where letter *p* denotes one of the three phases *a*, *b* or *c*, and v_{po} the corresponding output voltage.

From Table 1, it can be pointed out that driving logic signals for IGBTs T_{p3} and T_{p4} can be obtained by inverting driving signals v_{p1} and v_{p2}, used for T_{p1} and T_{p2}. Moreover, each NPC inverter phase can make use of only three different switches configurations; in fact, configuration $v_{p1} = 1$ and $v_{p2} = 0$ cannot be used as it supplies an output voltage dependent on the sign of the phase current. As consequence, the NPC inverter is characterized by 27 switches configurations.

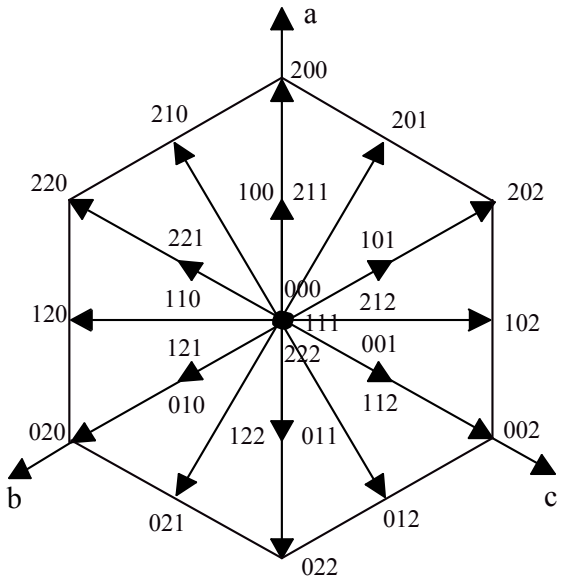

Fig.2 - NPC inverter output voltage vectors.

Switches configurations produce 19 different voltage space vectors, as shown in Fig. 2, in which the switches configurations are coded by symbols 0, 1 and 2, identifying the three voltage levels 0, $V_{dc}/2$ and V_{dc} on each inverter phase. As in two-level VSI, some configurations (000, 111 and 222) supply a null voltage vector and they are denoted as inactive; the others provide a non-zero voltage vector and are denoted as active. There are three different kinds of active vectors:

- six large vectors, whose module V_{max} is equal to $\sqrt{2/3}\ V_{dc}$;
- six medium vectors, whose module V_{med} is equal to $\sqrt{3}\,V_{max}/2$;
- six small vectors, whose module is equal to $V_{max}/2$.

Moreover, two different switches configurations (for example 100 and 211, 221 and 110) produce the same small vector.

3 SPACE VECTOR TECHNIQUE

In two-level inverters, employing a SVM technique, the approximation of the desired voltage vector is achieved by applying, at every sampling period, two active and two inactive voltage vectors. To this aim, the sampling period, T_c, is subdivided in four time intervals t_0, t_1, t_2 and t_3: in the first and in the last interval an inactive vector is employed to obtain always adjacent commutations while, during the others, the two active voltage vectors nearest to the desired one are applied. The durations of time intervals t_1 and t_2 are chosen in such way that the average value of the applied voltage vectors coincides to the desired one; time interval t_0 is chosen equal to t_3.

In two-level inverters, the choice of the active voltage vectors is always unique. On the contrary, in NPC inverters the choice of the active voltage vectors is generally non-unique because there are more than one terns of voltage vectors that can provide the same average voltage vector; moreover, inactive vectors cannot be used in the same manner as in two-level inverters.

The proposed modulation technique aims to save the advantages of the SVM used in traditional two-level inverters, i.e.:

- all the commutations must happen only between adjacent states;
- during each modulation interval, only three commutations are effected.

Several SVM techniques for NPC inverters are presented in literature [6-9]. Generally, these techniques only partially consider the switching frequency minimization problem; in fact, some methods do not impose adjacent commutations, while others guarantee adjacent commutations only when the voltage vector moves inside the same geometrical figure.

To achieve the previously mentioned goals, the paper suggests subdividing the output voltage three-phase plane, shown in Fig. 3, in six partially overlapped hexagons and imposing that, during each sampling interval, the modulation uses only the voltage vectors contained in a hexagon. Fig. 5 illustrates only two hexagons, highlighting their overlapped part with crossed lines.

The same subdivision in six hexagons was suggested also in [8]; however, its utilization is rather different from that presented in [10]. In fact, in the proposed approach, the subdivision of the voltage plane aims to achieve the following two goals:

- the application, inside each hexagon, of the standard SVM used in two-level inverters;
- make, as easy as possible, the transition from a hexagon to the subsequent one.

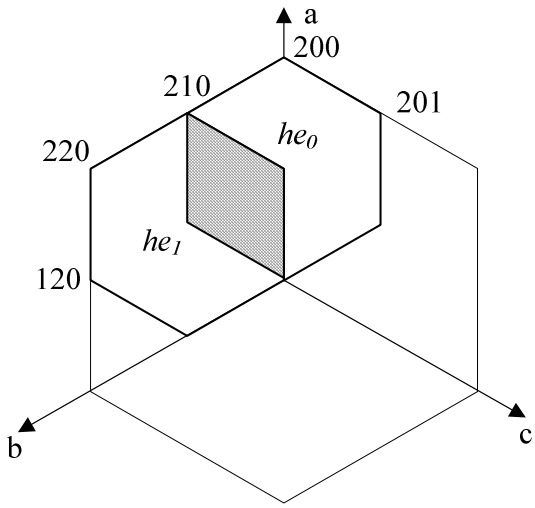

Fig. 3 – Three-phase plane subdivision.

Finally, to simplify the implementation of the modulation procedure on a microcontroller, the voltage space vector is identified by two integer variables i and n; variable i (in range 0 ÷ 5) specifies the actual hexagon he_i, while variable n (in range 0 ÷ 7) indicates the voltage vector v_n inside the hexagon, considering the definitions normally used in two-level SVM.

The techniques used to define the sequence of the voltage vectors are different, depending on the operating conditions: if the desired voltage vector v_d does not overcome a fixed angular threshold, the modulation continues inside the same hexagon; on the contrary, a suitable procedure must be applied to move the modulation to an adjacent hexagon.

When the modulation remains inside the same hexagon, the determination of the voltage vectors follows the usual rules employed in two-level inverters, subtracting from all the voltage vectors the central voltage vector of the hexagon. To describe the proposed technique, at first a desired voltage vector inside hexagon he_0 will be taken into consideration. Fig. 4 shows the correspondence between NPC inverter vectors configurations belonging to hexagon he_0 and the homologous two-level inverter vectors, denoted as $v_1,..,v_6$; configurations 100 and 211 respectively correspond to inactive configurations v_0 and v_7. Therefore intervals durations can be calculated by the same expression used in two-level inverters so to realize voltage vector v_d'.

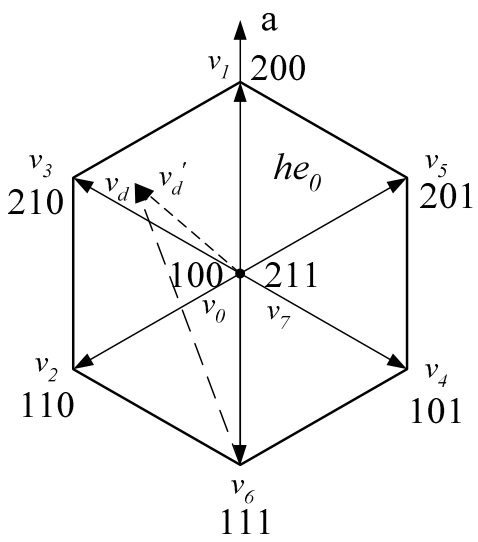

Fig. 4 - Modulation in hexagon he_0.

When the desired voltage vector is in a hexagon he_i, different from he_0, the voltage vectors sequence can be determined in the same manner as in hexagon he_0, applying to the voltage vectors a reference system transformation. To this aim, a rotation equal to $60°\cdot i$ must be effected to refer the actual situation to hexagon he_0. Such approach permits to calculate vector sequence always in the same situation reducing the overall algorithm complexity.

3.1 Transition to an adjacent hexagon

Referring to a generic hexagon he_i and supposing a counter-clockwise rotation of v_d, when the rotating reference voltage overcomes a fixed angular threshold, equal to $60°\cdot(i+0.5)$, the transition to an adjacent hexagon must be predisposed by using the overlapped zones of the hexagons. To this aim, the vectors sequence must be modified so that the final vector of the sequence coincides to the center of the adjacent hexagon. In closed-loop control system, when fast variations either of the load torque or the speed reference occur, the voltage vectors reference can move from a hexagon to another one without transit in the overlapped zones; in this operating condition, to maintain adjacent commutations, the full desired voltage vector cannot be produced during one or more sampling periods. Fortunately, if the sampling period is chosen adequately, this condition is only exceptionally verified.

4 Small Vectors based SVM

The previously described technique, denoted as SVM3L always employs three voltage levels; moreover, as initial and final vectors of each modulation interval, it always uses small vectors whose amplitude is different from zero. Desired voltage vector v_d can be realized in every direction only if its module V_d assumes a value lesser or equal to V_{med}. So modulation index m, defined as the ratio V_d/V_{med}, can be varied from 0 to 1. When m becomes smaller than 0.5 a different strategy, which employs only small and inactive vectors, can be applied. This latter solution, in the following indicated as SVM2L, uses only two voltage levels and employs, as initial and final vectors of each modulation interval, inactive vectors. It is possible to notice that SVM2L produces the same results as SVM technique used in traditional two-level inverters.
Fig. 5 shows the waveforms of a performance index, proportional to the RMS value of the current harmonics losses, produced by both the strategies for different values of modulation index m.

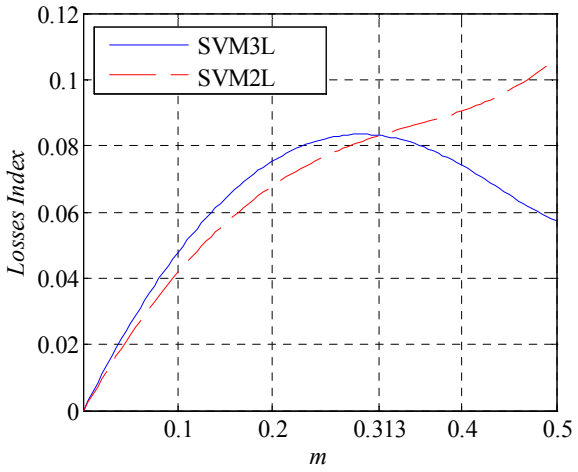

Fig. 5 – Indexes shapes of harmonics losses.

As it can be noticed from Fig. 5, when the modulation index remains below a value equal to about 0.313, the harmonics losses produced by SVM2L are lower than that obtained by SVM3L. Similar waveforms of the harmonics losses were pointed out also in [13].
SVM2L employs, alternatively in each modulation interval, either redundant switches configuration producing a small vector. By this way, the voltage across every supply-line capacitor is maintained more balanced.

5 Experimental Results

The proposed modulation techniques have been verified at first by different simulation tests. In order to provide an experimental validation of the obtained results, a suitable procedure, employing both SVM3L and SVM2L, were implemented on a control board, based on Texas Instruments TMS320F2407A microcontroller. The control

device is equipped with two PWM devices, each one able to provide control signals for a standard two-level inverter. An efficient implementation [11] was necessary both to allow the microcontroller providing the 12 control signals for a NPC inverter and to reduce the computation time of the modulation procedure.

The power circuit employed for the tests was composed by a NPC inverter prototype, built-up by power MOSFET, and passive three-phase RL load, composed by a 10Ω resistance and a 3mH inductance.

Figs. 6 and 7 show the phase current waveforms, characterized by a frequency of about 50 Hz and amplitude of about 6A, obtained using respectively SVM2L and SVM3L. Both the shapes were achieved using a modulation index *m* equal to 0.288 and a sampling period of 250 μs, which produces an average switching frequency per MOSFET of 1 kHz.

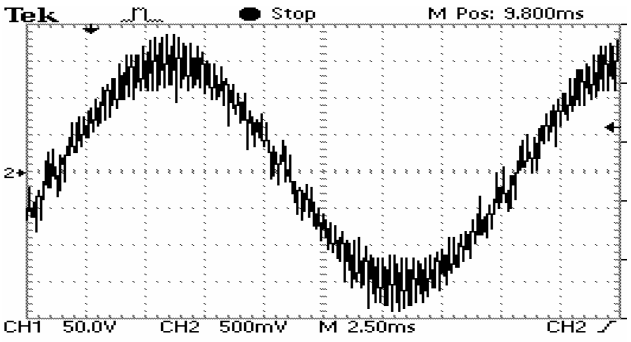

Fig. 6 - Phase current produced by SVM2L.

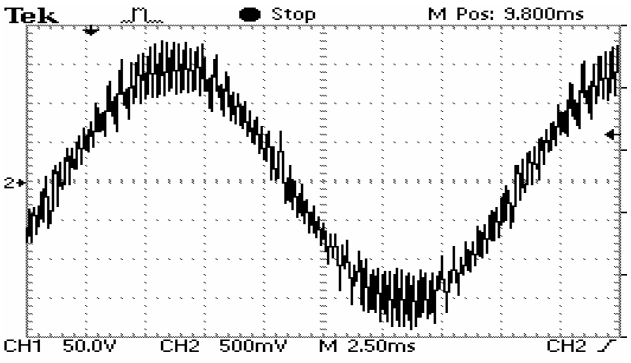

Fig. 7 - Phase current produced by SVM3L.

A quite low commutation frequency was chosen to represent adequately the operating condition of switching devices employed on high power application as locomotives traction inverters.

Figs. 8 and 9 illustrate harmonics spectrum generated, respectively, by the phase currents obtained using SVM2L and SVM3L techniques. The calculation of the Total Harmonic Distortion furnishes, respectively, values of 14.94% and 15.79%, which confirm the better harmonic content produced by SVM2L.

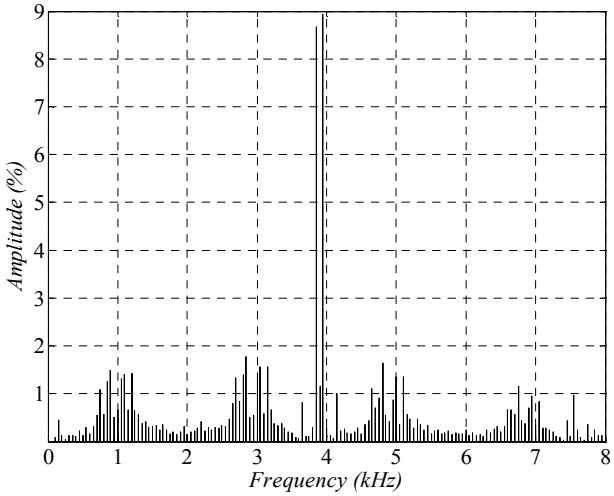

Fig. 8 - Current harmonics produced by SVM2L.

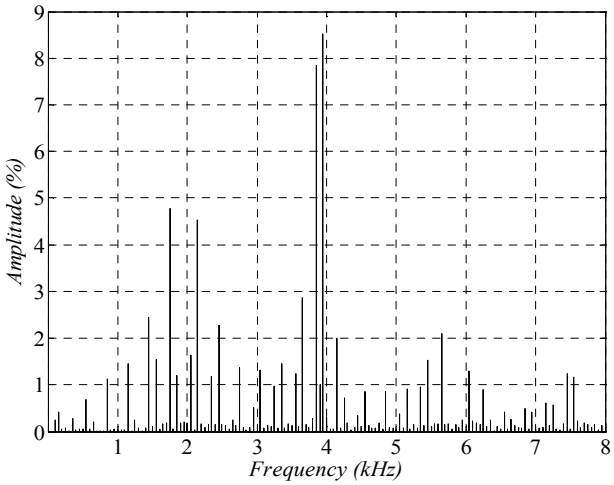

Fig. 9 - Current harmonics produced by SVM3L.

The different behaviour between the two solutions can be justified analyzing the voltage waveforms of the load star centre illustrated in Figs. 10 and 11, respectively for SVM2L and SVM3L modulation techniques. The waveforms were achieved in the previously mentioned operating conditions. Fig. 10 points out that SVM2L produces, on the star centre voltage, only oscillations at frequency equal to 1 kHz, which is the switching frequency of power devices. On the other hand, from Fig. 11, it can be noticed that the star centre voltage produced by SVM3L is characterized by a high frequency oscillation and an overlapped low frequency signal, located at 3 times the output current frequency. The low frequency oscillation can generate, when a single supply voltage is used, a voltage unbalance between the supply-line capacitor.

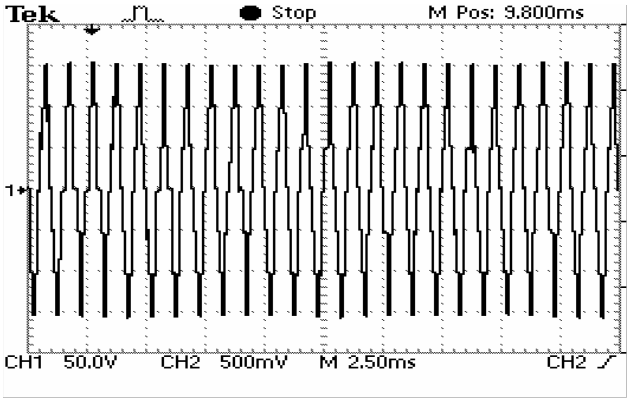

Fig. 10 – Star centre voltage produced by SVM2L.

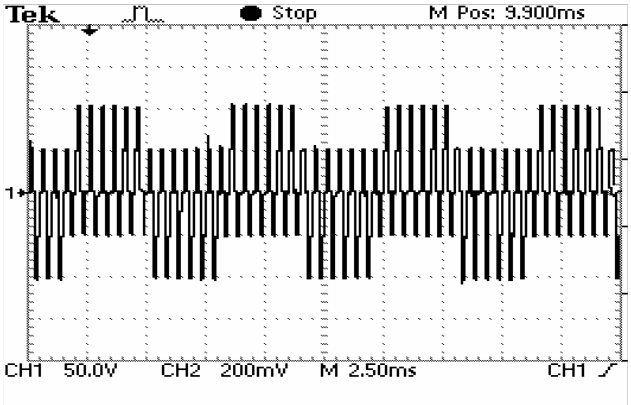

Fig. 11 - Star centre voltage produced by SVM3L.

5 Conclusions

The paper presents two different modulation strategies based on a Space Vector Modulation (SVM) technique, specifically designed for three-phase Neutral Point Clamped (NPC) inverters. SVM technique is able to maintain, also in NPC inverters, all the advantages of SVM used in traditional two-level inverters. The paper proposes to use a different modulation strategy (SVM2L), which employs only small and inactive vectors, when the module of the desired voltage vector assumes values lesser than 22% of the DC supply voltage. An experimental comparison between the two solutions has shown that the utilization of SVM2L improves the harmonic content of the phase currents produced by NPC inverters.

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