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A Resistance Emulation Technique to Improve Efficiency of a PWM Adjustable Speed Drive with Passive Power Factor Correction

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Abstract: - An approach recently introduced to correct the power factor of single-phase and three-phase diode rectifiers is extended to high-power PWM adjustable speed drives (ASDs). The proposed AC/DC stage of the drive is based on a new three-phase diode rectifier, obtained by properly connecting three single-phase diode rectifiers. The power factor of each single-phase rectifier is corrected by using a passive correction technique based on a resistive-capacitive branch connected at the DC-terminals of the rectifier. To improve efficiency of the whole circuit, a resistance emulation technique is introduced, analyzed and discussed. The designing procedure of the passive correcting branches and of the introduced "resistance emulator" circuit, for the power factor correction, is investigated. Analyses of performances of the new PWM ASD scheme are developed with the help of several PSPICE simulations, on a case-study PWM ASD for an asynchronous motor of about 1.5 MW of active power and under different working conditions.

Key-Words: - Adjustable Speed Drives, Power Factor, Total Harmonic Distortion Factor, Efficiency, Three-phase Rectifiers, Passive Power Factor Correctors.

1 Introduction

Traditionally, conversion of electrical power from AC to DC, for medium to high power PWM ASD for asynchronous motors, is done by using a three-phase diode bridge rectifier with inductive/capacitive DC output filter, as shown in Fig.1.

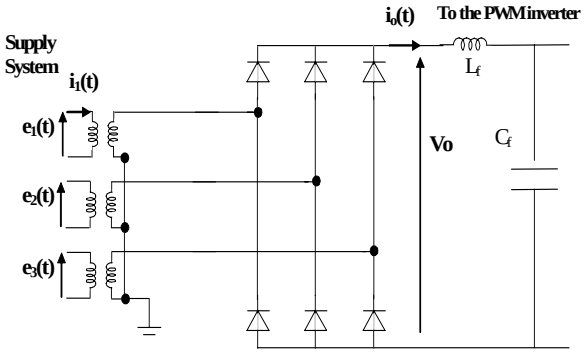

Fig.1. Conventional three-phase diode rectifier

Three-phase bridge rectifiers are characterized by a non-linear behavior because of the time-variant characteristic of their switching devices (diodes) and, thus, they have the disadvantage of absorbing highly distorted AC line current, $\mathbf{i}_1(t)$, with large fifth and seventh harmonic components. The increased use of this kind of power electronic equipments has put attention to quality aspects of electrical power; in order to achieve power quality at acceptable levels, recommended practices specify harmonic limits of power converters and the use of power factor correctors (PFCs) is strongly encouraged.

At present many PFCs are available for three-phase rectifiers. They are essentially based on the use of additional circuit components with different kind of complexity [1-7].

Recently, a simple passive PFC has been introduced for three-phase rectifiers [5-7].
It is essentially based both on the rearrangement of the conventional rectifier circuit topology and on the use of R-C passive branches to be properly inserted on the DC-side of the circuit.
The AC-line currents are effectively improved without introducing high frequency harmonics and low cost and high performances are also expected, especially with respect to other passive PFCs [6].
In [7] it was evidenced that this passive circuit can be effectively used also to correct PF of high power PWM ASD for asynchronous motors.
In [6, 7] it was evidenced that the main drawback of this passive PFC is efficiency, that is low

because of the additional power losses on the circuit resistors, requested for power factor correction.

In the paper, the aforementioned passive PFC is recalled and briefly described, with reference to high power PWM ASD for asynchronous motors.
Then, with the aim to avoid power losses on the resistors of the passive PFC and to improve circuit efficiency, a resistance emulation technique is introduced, analyzed and discussed.
Several PSPICE numerical simulations, of a high power PWM ASD case-study circuit, are performed; the results are critically analyzed in order to give evidence of the effectiveness of the proposed resistance emulation technique.

2 A passive PFC for three-phase diode rectifiers

In [4] a simple passive PFC was introduced and discussed with reference to single phase diode rectifiers.

In order to make possible the extension of the aforementioned passive power factor correction technique also to three-phase diode rectifiers, in [5] the conventional three-phase rectifier bridge topology has been rearranged by using three single-phase rectifiers connected in series at their DC-side terminals. Then each single phase rectifier is corrected by using the same passive correction technique; the PFC passive components are designed by using a procedure able to account for the new circuit topology.
Figure 2 shows the rearranged three phase rectifier circuit.

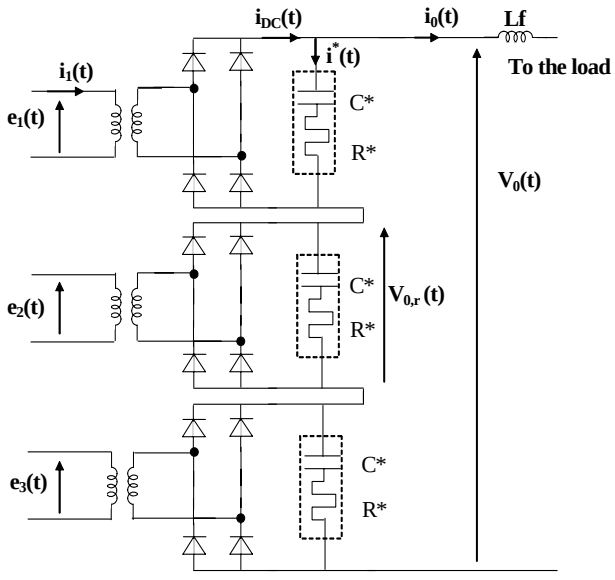

Fig.2. The rearranged three-phase rectifier, with passive PF correction branches.

From figure 2, it is evident that the passive correction technique essentially consists of adding, at the DC-side terminals of each single-phase rectifier, a branch with passive elements (R*, C*). Extra and properly settled currents, $\mathbf{i}^*(t)$, absorbed by these additional branches, are added to the rectifier output current, $\mathbf{i}_0(t)$, so making possible the correction of the rectifier AC line absorbed currents, $\mathbf{i}_1(t)$.

In order to make sinusoidal the AC line currents absorbed by the rearranged three-phase rectifier, the R* and C* parameter values have to be selected so that the equivalent impedance as seen from the DC-side terminals of each single-phase rectifier results resistive and equal to:

$$Ro = \frac{Vo}{Io},$$

where Vo and Io are the mean values of the rectifier output voltage and output current, respectively.
In [5] it was demonstrated that, in order to achieve this goal, it must be:

$$R^* = \frac{Ro}{3},$$

while C* is suggested to be selected as greater as possible, taking into account its cost and also the expected circuit performances.
Fortunately, in [5] it has been shown that circuit performances do not rapidly worsen when C* value rapidly decreases. For the sake of brevity, some more details on the recalled PF correction technique are postponed to [5-7].

In [7], the rearranged three-phase diode rectifier has been used as AC/DC conversion stage of a three-phase PWM ASD for high power asynchronous motors.
It has been shown that this rearranged rectifier with passive PF correction is able to significantly improve the circuit PF, both under nominal and low load power working conditions.

In the next section, the performances of the aforementioned circuit are briefly recalled for the sake of readability.

3 Performances of a rearranged PWM ASD with passive power factor correction

3.1 The case-study

It consists of a three-phase PWM ASD for an asynchronous motor of about 1.5 MW of active power.

The diode rectifier operates with a supplying line to line voltage amplitude of *Vrms*= 6 kV, at the line frequency of *fac*=50 Hz.

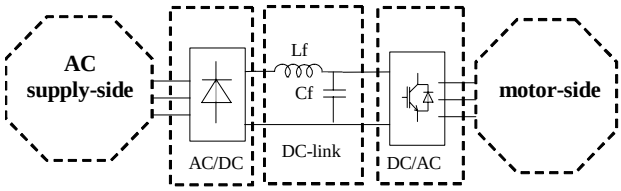

Fig.3. The PWM ASD case-study scheme.

With reference to Fig.3, in Table 1 the DC-filter inductance, L_f, the DC-filter capacitance, C_f, and the maximum value of the switching frequency of the PWM inverter devices, $f_{sw,max}$, are also reported.

Table 1. Values of the circuit main parameters

L_f [mH]	C_f [μF]	$f_{sw,max}$ [Hz]
30	400	450

With reference to the nominal power of the motor, the R*, and C* parameter values, to be utilized in the new three-phase rectifier scheme (as shown in Fig.2) for power factor correction, are calculated as indicated in section 2 and are reported in Table 2.

Table 2. PFC parameter values, utilized for the case-study analysis

C* [mF]	2.0
R* [Ω]	18

3.2 Simulation results

PSPICE has been utilized to perform numerical simulations under different working conditions, as fully referred in the following.

Nominal conditions are firstly considered; furthermore, different values of the power requested by the motor are also considered, in order to estimate the sensitivity of the corrected circuit to motor power variations.

Figure 4 shows the waveform and the THD of the AC line currents absorbed, under nominal conditions, by the corrected PWM ASD, by using different values of C*.

It is well evident as, with respect to the conventional PWM ASD, circuit performances are significantly improved, also for low values of C*.

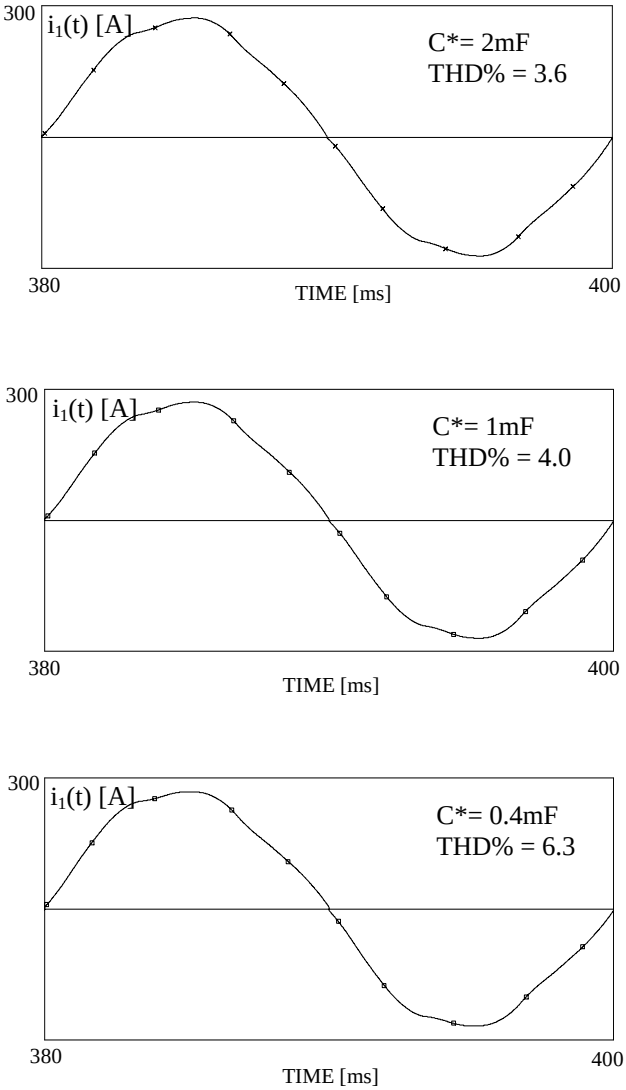

Fig.4. AC current waveforms absorbed by the rearranged PWM ASD case study circuit, under nominal condition and for different values of C*

In Figure 5, the AC absorbed current waveforms, obtained by loading PSPICE for different values of the power requested by the motor (from 100% to about 35% of the nominal value) and, consequently, for different values of the motor frequency and of the PWM inverter modulation index, are reported together with their THD percentage values.

In order to avoid a strong worsening of the current THD at very low motor power (for more details see [7]), a value of R* settled with reference to about the 80% of the motor nominal power has been used, instead of that previously settled referring to the motor nominal power (22 Ω instead of 18 Ω).

It is evident that at very low power the THD of the absorbed current is sensibly worsen (THD=23%), even if it results better to that previously calculated for the conventional circuit operating under nominal power working condition (THD=27%).

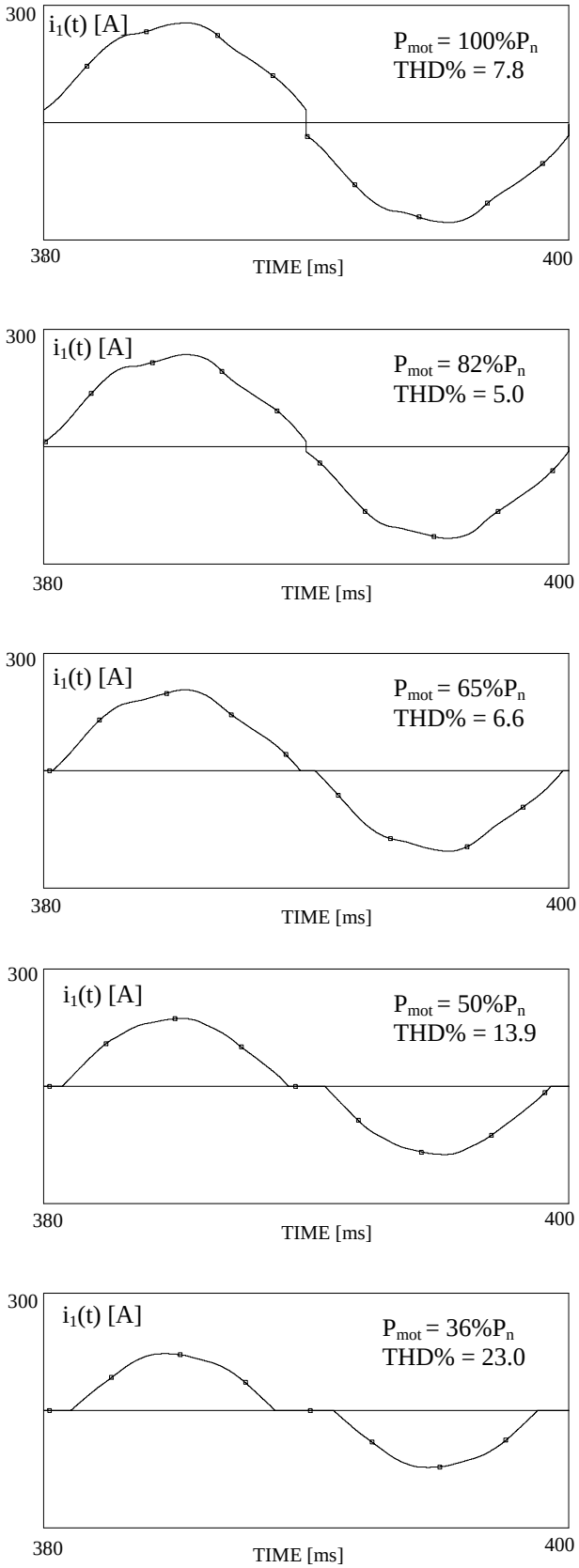

Fig.5. Waveforms of the AC absorbed currents, for the PWM ASD case study circuit rearranged as in Fig.2, for different values of the motor power and with R* settled with respect to the 80% of the nominal power (R*=22 Ω)

3.3 Circuit sensitivity to correcting resistor value

In order to evaluate how much the circuit is sensitive to the variation of the value of the resistor R* needed for the PF correction, a sensitivity analysis is performed referring to the nominal power working condition and taking into account of a resistance value variation between ±10% around its nominal value (R*=18 Ω), with a step of a 2%.

In Fig. 6, the results are reported in terms of AC side current THD versus the percentage variation of the value of the resistor requested for PF circuit correction, around its nominal value.

It clearly results that the AC current THD is very little sensitive to R* resistance variations.

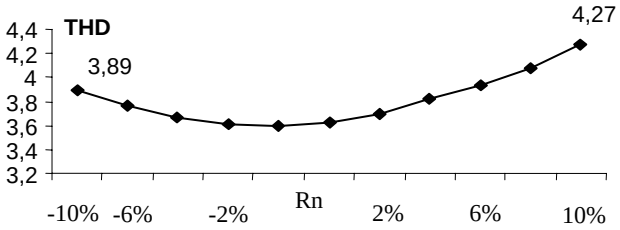

Fig.6. AC side current THD, under nominal working condition and versus the % variations of the R*, around its nominal value

3.4 Circuit efficiency

The efficiency of the circuit rearranged as indicated in Fig.2 results significantly worsen with respect to that of the conventional circuit, because of the additional power losses on the resistive elements, R*, of the correcting passive branches.

With reference to the case-study circuit working under nominal conditions and corrected by using for the resistors R* the value settled with respect to the 80% of the motor nominal power in order to better compensate the motor power variations, a circuit efficiency equal to 0.81 has been calculated.

It is important to underline that, under the same working condition, an efficiency significantly higher (equal to about 0.96) has been calculated for the conventional and uncorrected circuit.

Efficiency of the rearranged circuit can be improved by introducing the idea of a “resistance emulator” to be used instead of R*, as fully explained in the next section.

4 A resistance emulator circuit

The basic idea starts from the consideration that a single-phase rectifier corrected at the DC-

side terminals as previously indicated in section 2 practically absorbs, from the AC supplying system, a sinusoidal current, proportional to the supplying voltage; this is to say that it has a behavior like that of a resistor, then it can be utilized as a "resistance emulator" circuit, **RE**.

Starting from this idea, each correcting resistor R* in Fig.2 can be substituted by an electronic single-phase diode rectifier properly corrected at its DC-side terminals by using – low power - passive branches with Ce* and Re* correcting elements.

In order to give back to the motor the **RE** absorbed active power and to improve the circuit efficiency, the three single-phase and low power **RE**, to be utilized instead of R*, can be connected in series among them and in parallel to the inverter DC-side terminals.

Furthermore, in order to make actually possible the connection of the whole **RE** (three single-phase **RE** connected in series at the DC-side) with the inverter, first of all the whole **RE** output voltage mean value has to be made equal to that of the main (high power) rectifier, and to achieve this goal an input - low power - transformer is needed for each single-phase **RE**, to properly regulate its output voltage level.

Finally, the whole **RE** has to be decoupled to the main rectifier, in order to avoid interactions between them; this can be accomplished by using an uncoupling - low power – inductor, with an L_e* value as greater as possible, taking into account its cost, volume, weight together with the expected circuit performances.

The scheme of each single-phase **RE** is shown in Fig.7, while the scheme of the rearranged three-phase diode rectifier with the whole **RE** is shown in Fig.8 (the inverter scheme is omitted for the sake of readability).

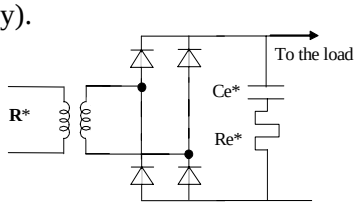

Fig.7. The proposed "Resistance Emulator" circuit

Once defined the circuit topology in presence of the whole **RE**, the procedure for calculation of the Ce* and Re* parameter values has to be investigated.

First of all, the transformation ratio, **n**, of the three **RE** single-phase transformers has to be calculated.

This can be done by firstly taking into account the constraint that the mean value of the whole **RE** output voltage has to be equal to that of the main rectifier and by calculating also the time domain voltage at the R* terminals, on the circuit without resistance emulation. From this last, the mean value of the whole **RE** output voltage with unity transformation ratio of the single-phase transformers can be easily estimated.

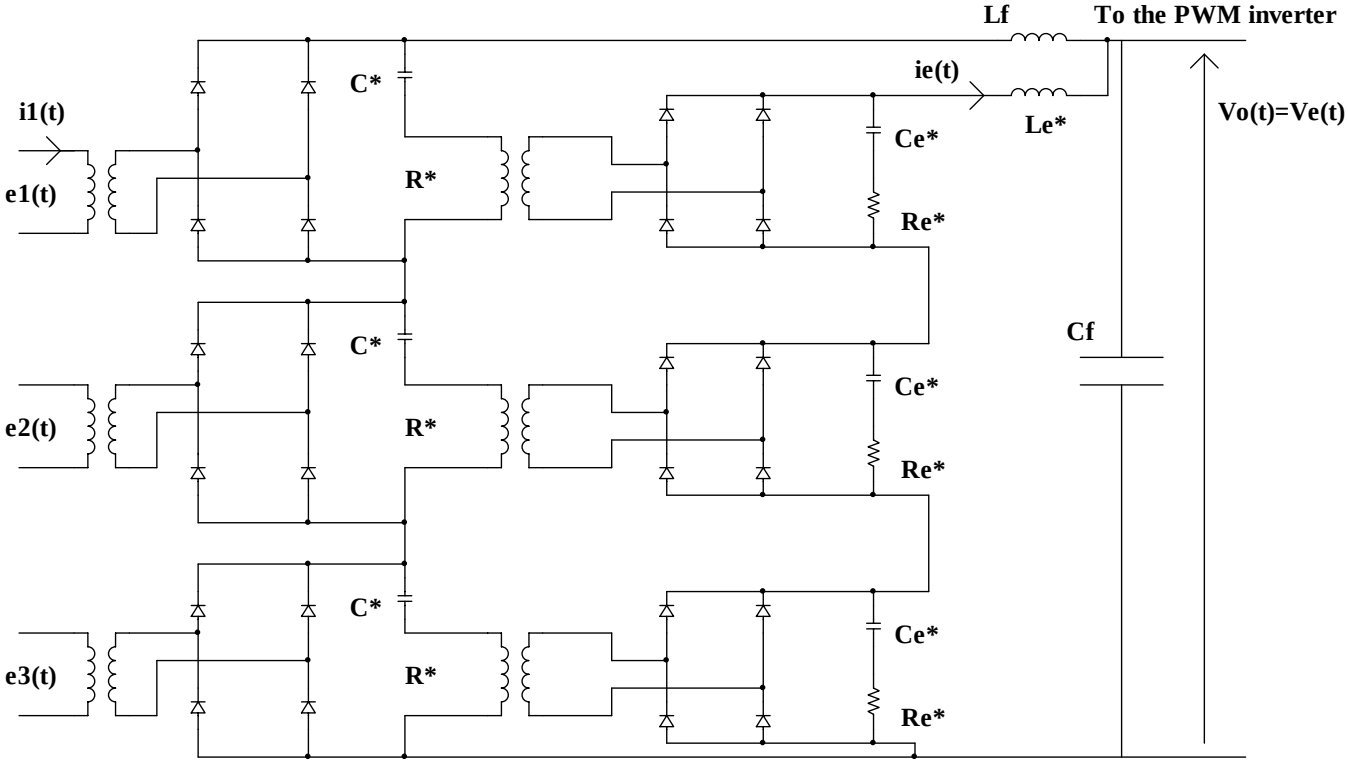

Fig.8. The rearranged three-phase diode rectifier with the whole "Resistance Emulator" circuit

Finally, the transformation ratio of the three single-phase transformers can be calculated as the ratio between the mean value of the main rectifier output voltage and the mean value of the whole **RE** output voltage with unity transformation ratio of the single-phase transformers.

Then, a procedure similar to that described in section 2 for the calculation of R* and C* values can be now applied to calculate the Re* and Ce* values.

Also in this case, an equivalent resistance, Re, as seen from the DC terminals of the whole **RE** can be defined:

$$R_E = \frac{Vo}{I_E} ,$$

where Ie is the mean value of the whole **RE** output current.

The following Re* value has to be used for PF correction of each single-phase **RE**:

$$\mathrm{Re}^* = \frac{R_E}{3} .$$

Also in this case and for the reasons explained in [5], for Ce* it is suggested to use a value as greater as possible, taking into account its cost together with the expected circuit performances.

In practice, in this new contest, the main problem to solve is the calculation of the aforementioned I_E value and this can be done by developing some considerations on the active power saved by introducing the **RE** circuit.

Firstly, the active power, P*, wasted on R* in the circuit without resistance emulation can be easily calculated, together with the rectifier input power, P_{IN}, the load voltage, V_0, and the load current, I_0, by simply simulating the circuit.

Assuming that the aforementioned power P* is a percentage of the rectifier input power, P_{IN}, the coefficient, K, defined as the ratio between the whole power (3P*) wasted on R* and the rectifier input power can be also calculated:

$$K = \frac{3P^*}{P_{IN}} . \qquad (1)$$

Likewise, - because of the circuit similarity - also the power, Pe*, wasted on the resistor Re* of each single-phase **RE** correcting branches of Figg.7 and 8 can be assumed to be a percentage of the single-phase **RE** input power (that is also equal to the power wasted on R*), with the same aforementioned coefficient K:

$$K = \frac{Pe^*}{P^*} . \qquad (2)$$

By following this approach, the power that the whole **RE** can give back to the load, P_S, can be expressed as a function of the rectifier input power:

$$P_S = 3P^* - 3Pe^* = (1-K)K\,P_{IN} , \qquad (3)$$

and then, the Re* value can be easily calculated:

$$\begin{aligned} P_S &= (1-K)K\,P_{IN} = V_0 I_E \\ P_{IN} &= P_{LOAD} + 3Pe^* = V_0 I_0 + K^2 P_{IN} \\ \frac{V_0}{I_E} = R_E &= \frac{V_0}{I_0}\frac{(1+K)}{K} \quad \Rightarrow \quad \mathrm{Re}^* = \frac{R_E}{3} = \frac{V_0}{I_0}\frac{(1+K)}{3K} \end{aligned} \qquad (4)$$

5 Performances of a rearranged PWM ASD with passive power factor correction and with resistance emulation

In order to give evidence of the effectiveness of the proposed resistance emulation technique, the case-study PWM ASD presented in section 3.1 is corrected as indicated in Fig.8 and analyzed with the help of several PSPICE simulations, under both nominal an low motor power working conditions.

The analysis is performed in terms of AC absorbed current THD, for all the examined working conditions, while circuit efficiency is calculated only with reference to nominal motor power working condition.

By following the designing procedure proposed in section 4 and with reference to the circuit depicted in Fig.8, the additional parameter values used for circuit simulations are reported in Table 3.

Table 3. Additional circuit parameter values, in presence of the whole **RE**

n	**Le*** [mH]	**Ce*** [mF]	**Re*** [Ω]
5.7	210	1.0	118.0

Figure 9 shows the AC line currents absorbed by the PWM ASD with the proposed whole **RE** and for different values of the motor power; the resulting current THD are also reported, as a percentage of their respective current fundamental components.

It is well evident that the current THD is always at acceptable levels and, at low motor power, it results also better than that obtained by means of the circuit without resistance emulation.

Furthermore, under nominal working condition, the efficiency of the circuit with the proposed whole **RE** has been calculated equal to 0.95, while a significantly lower efficiency of 0.81 was previously calculated for the circuit without resistance emulation.

It can be concluded that the introduced whole **RE** circuit produces positive effects on both circuit efficiency and AC absorbed current THD, both under nominal and low motor power working conditions.

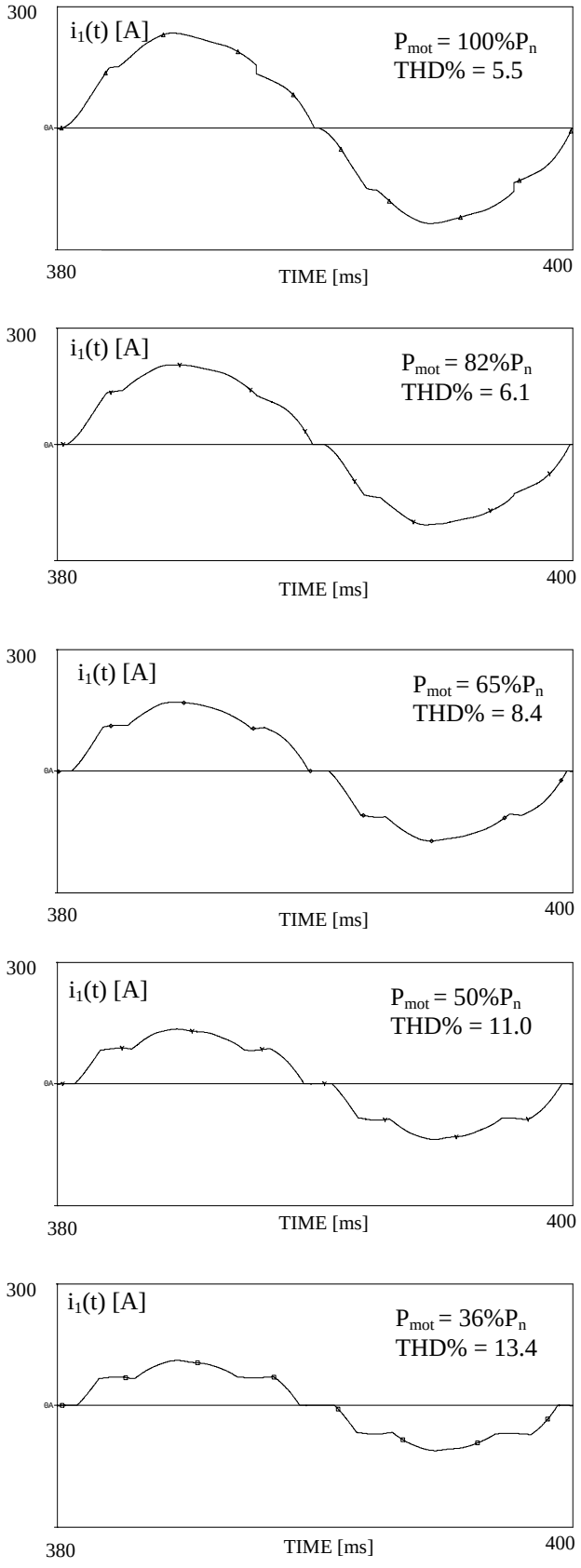

Fig.9. AC absorbed current waveforms for the PWM ASD case study circuit with the whole **RE**, for different values of the motor power

6 Conclusions

The AC/DC stage of a conventional PWM ASD has been rearranged by using three single-phase diode rectifiers connected in series at the DC-side terminals. Then, power factor of the whole circuit has been corrected by means of a very simple passive correction technique.

In order to improve efficiency of the rearranged circuit a "resistance emulator" circuit is introduced and utilized instead of passive resistors needed for passive power factor correction.

The analyses of the results, obtained by loading several PSPICE simulations on a PWM ASD case study for an asynchronous motor of about 1.5 MW of active power and under different working conditions, have shown the effectiveness of the introduced "resistance emulator" circuit.

The proposed circuit seems to be able to improve both the circuit efficiency and the AC line current THD, under both nominal and low motor power working conditions.

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