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Algebraic Simplification of Circuit Models

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Abstract: - The paper deals with simplification of symbolic formulas for network functions of linear circuits in the frequency domain. A method has been proposed for algebraic (error-free) simplification performed directly on circuit equations rather then on the resulting expression. The method is based on two-graph circuit representation.

Key-Words: - Symbolic Analysis, Linearized Circuits, Graph Methods

1 Introduction

The paper deals with symbolic analysis of linearized circuits in the frequency domain. The aim is to perform such modifications of circuit model that are equivalent to algebraic simplifications of symbolic formula for a network function. The result is the simplified mathematical model (system of linear equations) providing exactly the same result as the original model.

Let the circuit be described by a system of linear equations

$$\mathbf{H}\,\mathbf{x} = \mathbf{b} \ . \tag{1}$$

Any network function can be expressed as a quotient of two algebraic cofactors

$$K(s) = \frac{\Delta_N}{\Delta_D} = \frac{P(s)}{Q(s)} \ , \tag{2}$$

where Δ_N, Δ_D are cofactors of **H**, and $P(s)$, $Q(s)$ are polynomials. It is well-known that some methods of determinant expansion generate mutually canceling terms [1]. For example, the formula may contain terms $...+g^2-g^2+...$ that, of course, cancel each other. If we use unique names for all network parameters the resulting formula for the determinant will be linear in any circuit parameter.

The occurrence of mutually canceling terms is caused by the structure of network equations and the particular method of determinant expansion. There are graph-based algorithms that do not produce canceling terms at all [1]. Therefore, the mutual canceling will not be considered as simplification here as it is just the result of particular method used for the solution of (1).

2 Redundancy of Mathematical Model

The solution of (1) provides directly all primary circuit quantities. Any network function in the frequency domain is a quotient of two quantities. So, we do not use all the information obtained by the solution of (1). There is a possibility of circuit model simplification. Fig. 1 shows two examples.

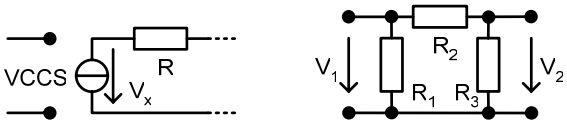


Fig. 1 Examples of redundant circuit model.

If we are not interested in voltage V_X in Fig. 1a) the symbol R will not occur in symbolic formula of any network function. Removal of the element simplifies the circuit model without any change to the network function of interest. Similarly, resistor R_1 has no influence to voltage transfer ratio of the circuit in Fig. 1b).

Generally, a reduction occurs in formula (2) for desired network function

$$K(s) = \frac{P(s)\,R(s)}{Q(s)\,R(s)} \ . \tag{3}$$

Let all circuit parameters have a unique name. Any network function can be written as

$$K = \frac{a\,q + b}{c\,q + d} \ , \tag{4}$$

where q is any network parameter. Let us admit both polynomials P and R in (3) contain q. Then

$$P(s)R(s) = (.... + p_{ij}\,q + ...)(.... + r_{ij}\,q + ...) \ ,$$

which is in contradiction to (4) (p_{ij} and r_{ij} are coefficients). Thus, the parameter q can occur either in P or in the common divisor R but not in both. The derivative of (4) with respect to q leads to a condition for independence of K on q

$$\frac{\partial K}{\partial q} = \frac{a\,d + bc}{(c\,q + d)^2} = 0 \;\Rightarrow\; ad = bc \;. \qquad (5)$$

It is easy to verify that condition (5) causes algebraic reduction of (4). The occurrence of q in the common divisor R can be tested by means of zero sensitivity. Thus, it is not necessary to generate the whole symbolic formula and then to search for the greatest common divisor of multivariate polynomials.

Let us consider a voltage-controlled current source connected between ports j and k (node pairs j_1, j_2, k_1, k_2) that is to be eliminated. The output current is $i_k = g_t\, v_j$. If $a \neq 0$ in (4) then also $c \neq 0$ because of (5). Setting $g_t \to \infty$ simplifies (4) to

$$\lim_{g_t \to \infty} \frac{a\,g_t + b}{c\,g_t + d} = \frac{a}{c} \;.$$

It can be done by means of transformation of **H** denoted as $\mathbf{H}_{k_1:j_1}^{[k_1>k_2:j_1>j_2]}$ (adding k_1-th row to k_2-th and removing k_1-th one; the same for columns j_1 and j_2). If $a = 0$ in (4) then $g_t \to 0$ should be applied instead.

Elimination of all zero-sensitivity elements simplifies the circuit mathematical model algebraically without solving (1).

3 Sensitivity Test

Sensitivity of any network function to any admittance can be expressed as a product of two transfer functions [3]. It can be generalized to any transconductance g_t connected between ports 3' and 3'' as shown in Tab. 2 and Fig. 2.

$$\frac{\partial K}{\partial g_t} = K_1\, K_2 \;. \qquad (6)$$

Table 1: Sensitivities of common network functions

network function	$K_1\, K_2$ (6)
voltage transfer ratio	$-K_{v13'}\, Z_{t3''2(1)}$
current transfer ratio	$-Z_{t13'(2)}\, K_{i3''2}$
input impedance (open output)	$-Z_{t13'}\, Z_{t3''1}$
transadmittance	$-K_{v13'(2)}\, K_{i3''2(1)}$

$K_{vab(c)}$, $K_{iab(c)}$, $Z_{tab(c)}$, are voltage transfer ratio, current transfer ratio and transimpedance respectively from port a to port b with port c shorted.

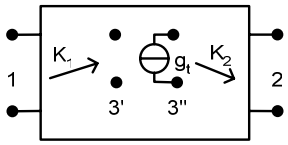


Fig. 2 Transfer functions for sensitivity computation.

Our aim is to test zero value of K_1 or K_2 symbolically, i.e. independently of numerical values of network parameters. Any floating-point calculation is affected by round-off errors and does not provide accurate information. The zero condition for K_1 and K_2 can be tested by means of zero value of numerators of those functions.

The zero-sensitivity test is based on the two-graph method [1]. It can handle any circuit by means of equivalent models for non-admittance elements. Computation of a circuit matrix determinant is equivalent to finding all common spanning trees (CSTs) of voltage and current graphs. To compute cofactors, the graphs should be modified according to row- and column operations [1], Fig. 3.

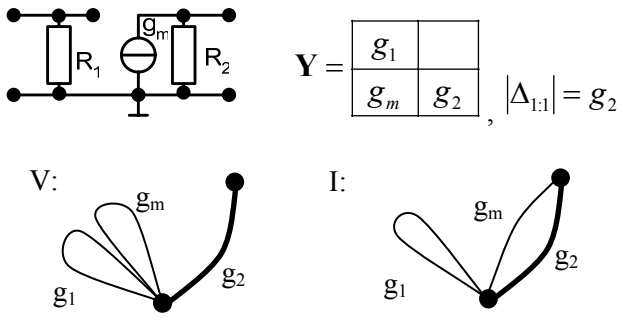


Fig. 3 Example of cofactor $\Delta_{1:1}$ computation by means of two-graph method.

The two-graph method does not generate canceling terms. Thus, if there is no CST of voltage and current graphs the cofactor is identically equal zero. Testing zero value of the cofactor is equivalent to testing the existence of CSTs. According to the Binet-Cauchy theorem the number of CSTs m is bounded by

$$\det(\mathbf{A}_I \mathbf{A}_V{}^T) \le m \le \min\left(\det(\mathbf{A}_I \mathbf{A}_I{}^T), \det(\mathbf{A}_V \mathbf{A}_V{}^T)\right), \qquad (7)$$

where $\mathbf{A}_I$ and $\mathbf{A}_V$ are reduced incidence matrices of current and voltage graphs respectively. If $\det(\mathbf{A}_I \mathbf{A}_I{}^T) = 0$ or $\det(\mathbf{A}_V \mathbf{A}_V{}^T) = 0$ the number of CSTs is zero. $\det(\mathbf{A}_I \mathbf{A}_I{}^T)$ is the number of spanning trees of the current graph itself. Its zero value can be tested simply by checking for the graph connectivity.

If $\det(\mathbf{A}_I \mathbf{A}_V{}^T) > 0$ the number of CSTs is

nonzero. As the incidence matrix entries are 0 and ±1 the determinant can be computed exactly using the integer arithmetic.

If it is still not possible to decide a more sophisticated test based on the matroid theory should be used. Graphic matroid is a structure $M = (E, \Im)$ in which *E* is a set of all columns of graph incidence matrix, and $\Im$ is a family of independent subsets of *E* (i.e. groups of edges – circuit branches). The elements of the incidence matrix are considered from a binary filed (0,1 – only). The linear independence means, the edges do not form cycles (loops). If the number of connected graph vertices is *n* then a set of (*n*-1) independent edges forms a spanning tree of the graph.

Reference [2] describes a polynomial algorithm for two matroid intersection. Let $M_I = (E, \Im_I)$ and $M_V = (E, \Im_V)$ be matroids for the current and the voltage graphs respectively. The matroid intersection is a group of edges that do not form a cycle in either graph. If the group consists of exactly (*n*-1) edges it is the common spanning three. So called *greedy algorithm* [2] allows finding the maximum cardinality intersection. If the number of edges of such intersection is lower than (*n*-1) then the cofactor is identically equal zero.

First, test (7) is carried out because of its simplicity. If it is not possible to decide the matroid test is performed. The process can be sped-up by numerical searching for elimination candidates.

4 Example

We are interested in voltage transfer ratio of the circuit in Fig. 4a). Using the nodal analysis and Cramer rule we can easily obtain a formula that evidently can be reduced

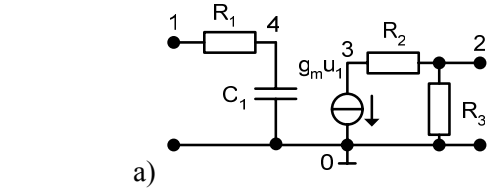
$$K_{U10->20} = \frac{U_{20}}{U_{10}} = \frac{-g_m g_2 (g_1 + sC_1)}{g_3 g_2 (g_1 + sC_1)} .$$

Parameters R_1, R_2 and C_1 are clearly irrelevant for the transfer function.

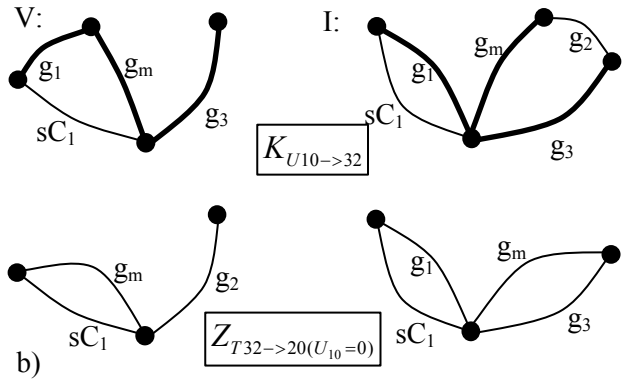
Let us consider resistor R_2. The sensitivity of voltage transfer ratio to g_2 is

$$\left| \frac{\partial K_U}{\partial g_2} \right| = K_{U10->32} Z_{T32->20(U_{10}=0)} = \frac{\Delta_{1,0:3,2}}{\Delta_{1,0:1,0}} \frac{\Delta^{[1>0:1>0]}_{1,3,2:1,2,0}}{\Delta^{[1>0:1>0]}_{1,0:1,0}},$$

where $K_{U10->32}$ is voltage transfer ratio from port 1,0 to port 3,2 ; $Z_{T32->20(U_{10}=0)}$ is transimpedance from 3,2 to 2,0 for 1,0 shorted. Fig. 4b) shows graphs for numerators of both transfer functions (see Tab. 1). There is at least one common spanning tree ($g_1 g_3 g_m$) for $K_{U10->32}$. But there is no intersection for $Z_{T32->20(U_{10}=0)}$. The element R_2 (g_2) can be removed from the circuit by $g_2 \to \infty$.



a)



b)

Fig. 4 Example of circuit model simplification.

5 Conclusions

The graph methods allow performing algebraic reduction of circuit model without necessity to generate symbolic form of network function and without knowledge of actual numerical values of network parameters.

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