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A Single-Phase Shunt Active Power Filter Based on Cycle Discrete Control for DC Bus Voltage

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Abstract:-A new control method for single-phase shunt active power filter (APF) is proposed. It integrates the DC bus voltage control and active power filter command current generation, according to the periodicity of source current and energy balance concept. The instantaneous harmonic compensation and linear DC bus voltage control are achieved, without complicated and involved control logic, by using cycle discrete control technique to DC bus voltage. A mathematical model of the scheme is developed. Detailed analysis and simulation in the PSCAD/EMTDC environment are presented. A laboratory prototype of this APF is developed to validate the result. Both of simulation and experimental results show the good behavior of this type of APF.

Key-Words:-Active power filter, Discrete control, Harmonic and Reactive power, PWM.

1 Introduction

Over the years, power electronics devices have become widespread in the industrial as well as in the domestic world such as cycloconverters, variable speed drives, personal computers. These non-linear loads draw reactive power and harmonic currents along with active power from ac mains. The reactive power and harmonic components of load current cause poor power factor, poor utilization of distribution system, overheating which deteriorate life expectancy of other equipments and cause low efficiency, disturbance to other consumers and interference to communication network. Conventionally, passive L-C filters and capacitors are employed to compensate harmonics and lagging power-factor of the linear and non-linear loads. But they have many demerits like fixed compensation, large size, resonance, noise, and increased losses [1,2,3]. Having the features of good transient response, accurate compensation, and eliminating resonance, APF has been used to replace the passive filters step by step ,and generated tremendous interest among the researchers.

Various types of active power filters are reported in the literature. References [4,5] introduce an APF based on instantaneous reactive power theory. Adaptive method for the harmonic extraction is utilized in the APF introduced in references [6,7]. It is a common observation that the calculation of harmonic decreases the response speed of APF. In order to maintain the DC bus voltage, general continuous PI control method is used in voltage control loop, which effects the compensation precision [1,8]. In paper [8], a LPF is used to get average value of DC capacitor voltage, this results in 2~3 cycle delay in response time. The non-linear PI controller for voltage loop makes the APF control more complex [9]. The approximating methods [10] can get linear control for DC bus voltage, but the overall performance is poor.

This paper proposes a new APF control technique, and in the proposed method, cycle discrete control is applied to DC voltage control loop. The salient feature of the proposed method is that it keeps the source current synchronized to the mains voltage, irrespective of the load transient. According to energy balance concept, the output of cycle discrete controller is equal to the magnitude of required active current to compensate the load active power and APF losses. The cycle discrete control method ensures that the source active current maintain perfect sinusoid path in each cycle, even during transient. This new method can minimize the source active current distortion at load fluctuations ,and in this control structure, there are no delay elements like LPF, hence the harmonic compensation is instantaneous.

2 Problem Statement

Fig.1 shows the power storage circuit diagram of the single-phase shunt voltage-mode APF. The filter consists of a PWM voltage source, inverter linked to the point of connection through a filtering inductor L_f and capacitor C_f. It is operated in a controlled current boost-type inverter mode, and the current drawn from the utility i_s is made to follow a sinusoidal reference current i_{rf} in a fixed hysteresis band.

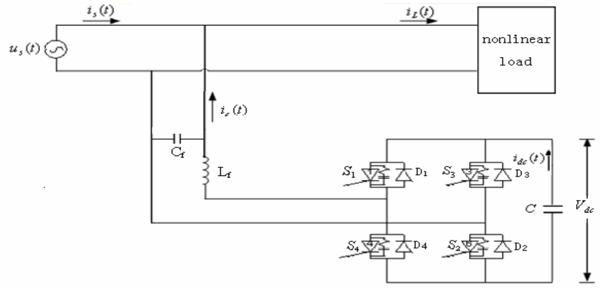

Fig.1 Basic Circuit of the active power filter

2.1 Classic Operation Principle of APF

Under normal circumstances, the utility can be assumed to be an ideal sinusoidal voltages source.

$$u_s(t) = V_{sm} \sin \omega t \tag{1}$$

Where ω is the fundamental frequency of the utility source voltage . In the case of a nonlinear load, the load current consists of fundamental component and the higher-order harmonic as follows:

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \theta_n) \tag{2}$$

From Fig.1, it can be found that the desired compensation current generated by power inverter can be represented as:

$$i_c(t) = i_L(t) - i_s(t) \tag{3}$$

In the classic control methods of active power filters, load current and source current is sensed to calculate the harmonic and reactive current. Owing to the losses in the inverter such as switching loss, capacitor leakage current etc., the utility not only provide the real power needed by the load but also the additional power required by the inverter to maintain the capacitor voltage at a prescribed value, hence the classical PI controller and LPF are often used in voltage loop [8]. Fig.2 shows one of classic schemes of generating single-phase APF output reference current reported in various papers e.g. [11].

In the Fig.2, the DC component I_{PL} obtained after LPF is equal to the peak value of active current of load current. The signal ΔI_p is the output of classical PI controller for the DC-bus voltage. If ΔI_p is free of harmonic ,then I_p is a fixed value throughout one cycle. However, a classical PI controller is applied, ΔI_p is not free of harmonics. And consequently, signal i_p can not be pure sinusoidal waveforms. Typical waveform of compensated source current in this case is shown in Fig.3. When the load current changes suddenly, I_p varies as the load current. Since i_p doesn't not change at the zero cross point of source voltage probably, hence distortion occurs in source current as shown in Fig.4 [10,12].

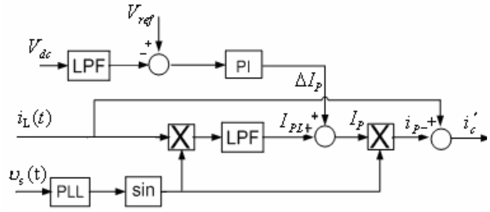

Fig.2. One of the classic schemes of generating single-phase APF output reference current

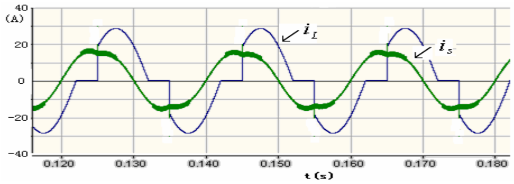

Fig.3. Compensated source current waves: Tr i_L is load current; Tr i_s is source current

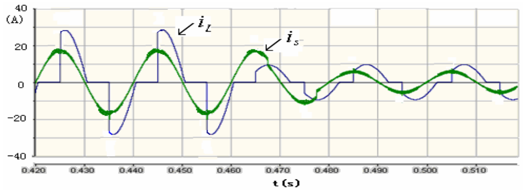

Fig.4. Source current in transient state: Tr i_L is load current; Tr i_s is source current

3 The Proposed Active PowerFilter

3.1 Principles of Operation

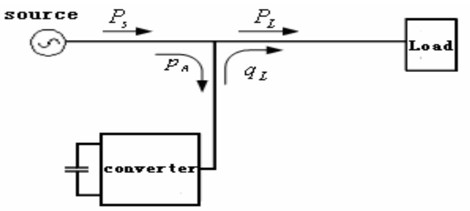

Fig.5 The power flow diagram of single-phase shunt APF

The power flow of single-phase shunt APF system is shown in Fig.5. At full compensation, source provides active power P_s which is equal to the sum of APF loss power P_A and active power of the load P_L. The load's reactive power q_L is provided by the APF. From eqution.1 and 2, P_s and q_L can be expressed as:

$$P_s = I_1 \cos\theta_1 V_{sm} \sin^2 \omega t \tag{4}$$

$$q_L = I_1 \sin\theta_1 V_{sm} \sin^2(\omega t) + \sum_{n=2}^{\infty} V_{sm} \sin(\omega t) I_n \sin(n\omega t + \theta_n) \tag{5}$$

Integrating the reactive power of load q_L in one fundamental cycle, we can get:

$$\int_0^T q_L dt = \int_0^T (I_q U_s \sin(\omega t) \cos(\omega t) + \sum_{n=2}^{\infty} U_s \sin(\omega t) I_n \sin(n\omega t + \theta_n)) dt = 0 \tag{6}$$

Where T is the fundamental period of the utility. Integrating P_s in one fundamental cycle results in following equation:

$$\int_0^T P_s dt = \int_0^T (I_1 \cos\theta_1 V_{sm} \sin^2(\omega t))dt = \frac{T}{2} I_1 \cos\theta_1 V_{sm} \qquad (7)$$

In a voltage-source inverter , the DC bus capacitor is used as an energy storage element of the system. Eqn.6 and 7 show that the reactive power q_L results in energy exchange between AC source and DC-side capacitor by inverter. The DC bus voltage fluctuates with the energy exchange. Whereas, the integration of q_L in one fundamental period T is zero, so the reactive power doesn't effect the T periodically sampled value of DC bus voltage. However integration of active power P_s is not zero, that is, if the DC bus capacitor provides active power for the load and inverter, then the periodically sampled value of DC bus voltage can not be constant.The T periodically sampled value of DC-bus voltage can supply the active power flow information, and the amplitude of the mains current can be obtained by using a voltage regulation circuit of the DC capacitor.

3.2 Model of Proposed Active Power Filter

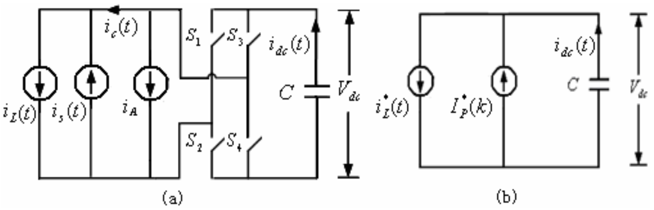

Fig.6 Simplified model of single-phase shunt APF

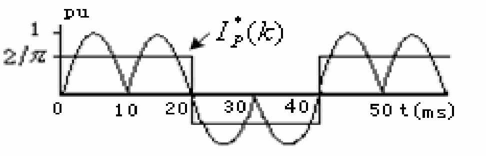

Fig.7 The waveform of signal $I_P^*(k)$

Generally, the APF output current consists of three components: load current i_L (t) , source current i_s (t) and the fundamental active current i_A which represents the loss of inverter. A simplified APF model of full bridge inverter acting as power storage is shown in Fig.6(a). The AC component of th capacitor current i_{dc}(t) doesn't change the periodically sampled value of DC-bus voltage, whereas the DC component of current i_{dc}(t) changes it. So the model in Fig.6(a)can be simplified toa model in the DC side of inverter shown in Fig.6(b). In this model the DC side capacitor current is given by $i_{dc}(t) = i_L^*(t) - I_P^*(t)$. The current $i_L^*(t)$ is equivalent to the sum of load current i_L (t) and current i_A, which consists of DC component and harmonic current. The DC current $I_P^*(k)$ multiply $\pi/2$ is the amplitude of source fundamental active current i_s (t) as shown in Fig.7. According to model in Fig.6(b), if DC current $I_P^*(k)$ can completely compensate the DC component of $i_L^*(t)$, the periodically sampled value of DC-bus voltage is maintained at a fixed value at the end of each cycle.Hence the APF just provides the harmonic and reactive component of load current meanwhile.

The equation mathematical model of the APF can be obtained as shown in Fig.8. In this model, the current $i_L^*(t)$ can be considered as a disturbance. As the signal $I_P^*(k)$ is a cycle discrete value, a zero-order hold with fundamental sampling period is used in the model. The transfer function of DC side capacitor plant $G(s)$ is

$$G(s) = \frac{1}{CS} \qquad (8)$$

Where C is the DC side capacitor. It can easily be verified that the discrete transfer function between the $I_P^*(k)$ and DC bus voltage can be written as:

$$G(z) = \frac{T}{C} \cdot \frac{1}{z-1} \qquad (9)$$

Where T=0.02ms is the period of system.

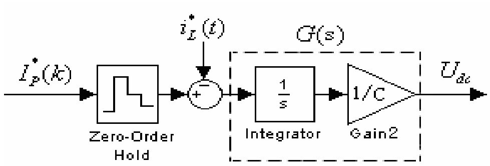

Fig.8 Mathematical model of proposed AFP in DC side of inverter

3.3 Design of Cycle Discrete Controller

The integration of the capacitor current i_{dc}(t) in one fundamental cycle can be written as following:

$$\begin{aligned} \int_{kT}^{(K+1)T} i_{dc}(t)dt &= \int_{kT}^{(k+1)T} (i_L^*(t) - I_P^*(t))dt \\ &= \int_{kT}^{(k+1)T} (I_L(k) - I_P^*(k))dt = T(I_L(k) - I_P^*(k)) = \Delta U_{dc} C \end{aligned} \qquad (10)$$

That is

$$\begin{aligned} I_L(K) - I_P^*(K) &= T/_C \, \Delta U_{dc} \\ &= T/_C \, (u_{dc}(k) - u_{dc}(k-1)) = u(k) \end{aligned} \qquad (11)$$

Where I_L(K) is the average value of currents $i_L^*(t)$ during the interval [(K-1)t , KT]. From eqn.11, the reference current input to the inverter to maintain DC bus voltage can be written as

$$I_P^*(k) = I_P^*(k-1) + u(k) \qquad (12)$$

The structure of this controller is illustrated in Fig.9.

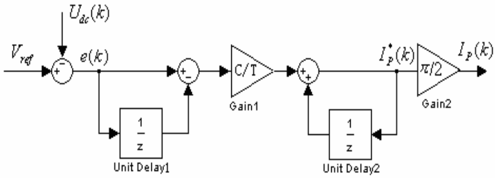

Fig.9. cycle discrete controller for DC-bus voltage using capacitor current

From Fig.9, the discrete transfer function $D(Z)$ can be given as

$$D(z) = C/T \qquad (13)$$

Eqn.13 is a P controller shown in Fig.10,and for C=10000uF, P is 0.5. In Fig11, the open-loop frequency response of this control system shows that the gain margin is 3 dB and phase margin is 45^0respectively. Fig.12 shows the good step response with one cycle delay and no steady error. In case of the disturbance, the output of this system will have an error shown in Fig.13.

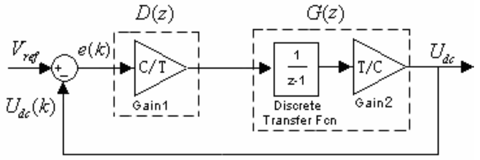

Fig.10. Transfer function model of the proposed APF

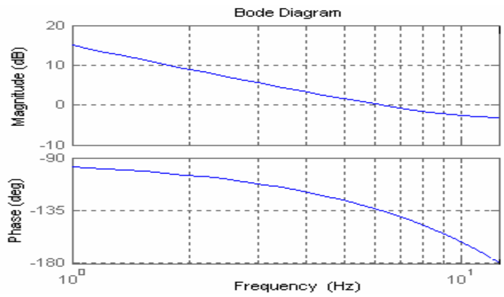

Fig.11. Open-loop frequency response of the control system using P controller

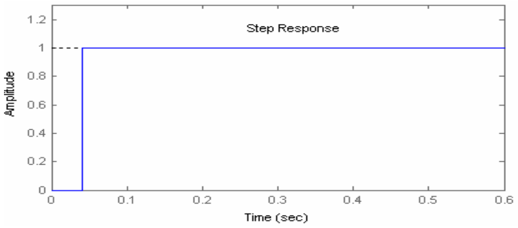

Fig.12 Step response of control system using P controller

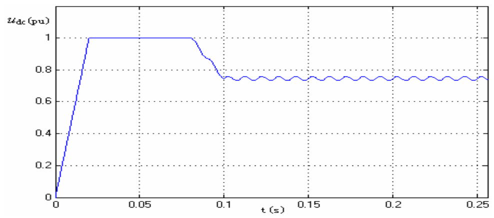

Fig.13 Output System of using P controller with disturbance

To eliminate the disturbance, a cycle discrete PI controller is used, which is shown Fig.14. When the PI controller parameters K_P and K_I is 0.45 and 0.1, gain margin of 6 dB and phase margin is 50^0 is obtained respectively shown in Fig15. Fig.16 shows the step response of this system. In Fig.17 it can be found that this close-loop system with cycle discrete PI controller can maintain the DC bus voltage near the reference value in spite of the disturbance.

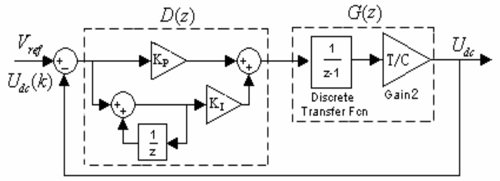

Fig.14 System model using periodic discrete PI controller

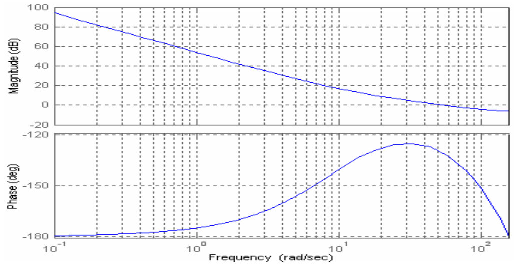

Fig.15 Open-loop frequency response of the control system using PI controller

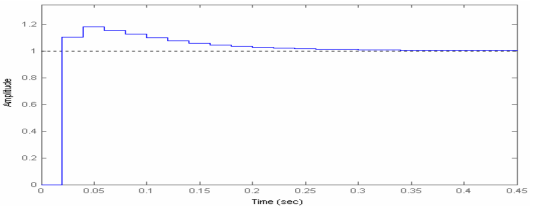

Fig.16 Step response of the control system using P controller

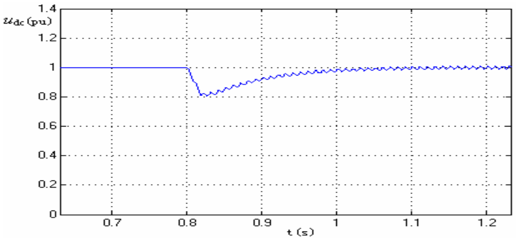

Fig.17 Output System of using periodic discrete PI controller with disturbance

3.4. Control Block Diagram

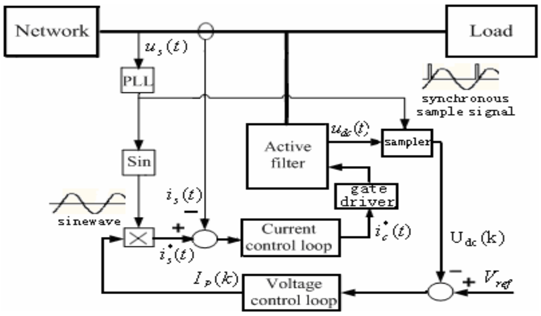

Fig.18 Basic control block diagram of the proposed scheme for single-phase APF

The basic control block diagram of the proposed scheme for single-phase APF is shown in Fig.18.It can be found that the DC bus voltage is sampled at the positive going zero-crossing instants. In this way, the high frequency disturbances in the whole system can be reduced[13]. The periodically sampled value of DC bus voltage $U_{dc}(k)$ is compared with a reference voltage V_{ref}. The compared output is fed to cycle discrete controller to generate the desired amplitude of source current $I_P(k)$. As the $U_{dc}(k)$ is sampled at the positive going zero-crossing instants of source voltage, it is ensured that the error information which passed to the cycle discrete controller is sampled only at the positive going zero-crossing point of source voltage. The desired amplitude $I_P(k)$ of source current is set at the beginning of each cycle, and is kept constant throughout the cycle. The desired source current and the detected source current are fed to the current control loop to generator the desired output current $i_c^*(t)$. The actual output current $i_c(t)$ is made to follow $i_c^*(t)$ within a hysteresis band. Since the amplitude of $I_P(k)$ is maintained constant throughout a sampled cycle of the source voltage, the source current remains distortion free and is in phase with the source voltage during both steady state and transient operation. Hence, the compensation process is instantaneous.

4 Simulation and Expereriment Results

4.1 Simulation Results

Simulation studies are carried out to predict the performance of proposed APF by PSCAD/EMTDC [14]. In the simulation, the system structure of APF is shown as fig.1, the nonlinear load is represented by antiparallel thyristors. The width of the hysteresis window is maintained at 0.5A, and the switching frequency is 10 KHz.

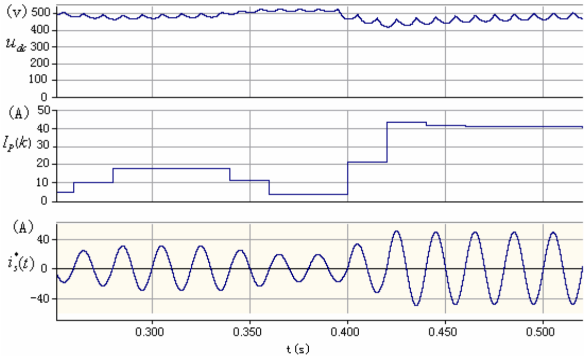

Fig.19 Waves of DC-bus voltage , the desired amplitude of source current and the desired source current

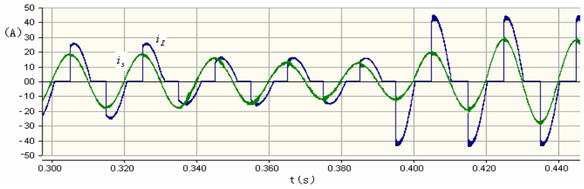

Fig.20 Simulation output of source current and load current; Tr i_L is the load current; Tr i_s is source current.

Fig.19 displays the waveforms of DC-bus voltage U_{dc}, the desired amplitude of source current $I_P(K)$ and the desired source current $i_s^*(t)$. It is shown that by using cycle discrete controller, the desired amplitude of source current $I_P(K)$ is a discrete value and keep constant in one cycle, so the desired source current $i_s^*(t)$ is always sinusoid. Since the switching frequency of inverter is 10K Hz, the fluctuations in DC-bus voltage are small, and the cycle sampled value of DC-bus voltage $U_{dc}(K)$ can be kept on reference value. When the load current decreases suddenly, the DC-side capacitor absorbs a part of instantaneous active power, the DC-bus voltage rises for a short period of time. On the contrary, while the load current increases, the capacitor injects some active power to AC source, and the DC-bus voltage dips for a short period of time. The distortion in transient-state is avoided by making use of the active power storage function of DC-side capacitor. The simulation output of source current i_s and load current i_L is shown in Fig.20, it can be observed that the source current maintains sinusoidal in despite of the fluctuation of load current.

4.2 Experiment Results

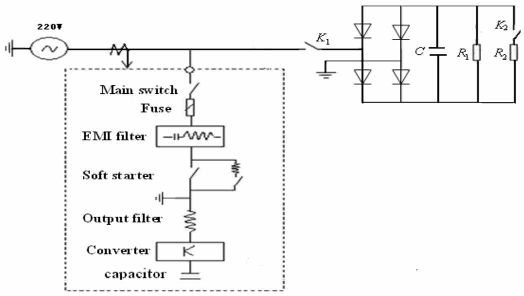

Fig.21 Experiment system structure

On the basis of the proposed control structure, a single-phase shunt APF prototype(220V/30KW) based on TMS320LF2812DSP is developed. The DC side capacitor C=10000 uF, filtering inductance L_f=0.1mH and capacitor C_f=30uF. DC-bus reference value U_{ref} =500V. The nonlinear load is represented by full-wave diode rectifier. The system structure is shown in Fig.21. Fig.22 show the steady-state performance of APF. It can be found that although the DC bus voltage has ripple ,it is stable and near the set value. It's fluctuation frequency is twice of the fundamental frequency of the AC source [1]. Furthermore the source current is almost sinusoidal. Fig.23and 24 show the harmonic spectrum of source current and load current. It is found that the THD of load current is approximately 50%, and the source current THD is less than 5%. Fig.25 is the transient performance of proposed APF .When switch K_2 opens suddenly, the load current decreases and the DC-bus voltage will rise a little for 3 period nearly. In the transient process, the source current doesn't show any distortion.

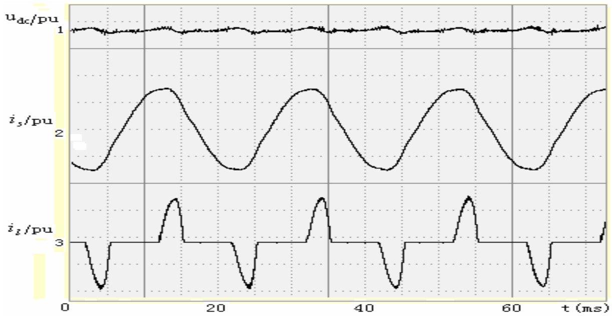

Fig.22 Steady-state performance: Tr1:DC-bus voltage (50v/div); Tr2:source current (10A/div); Tr3:load current (10A/div) time scale =5ms/div

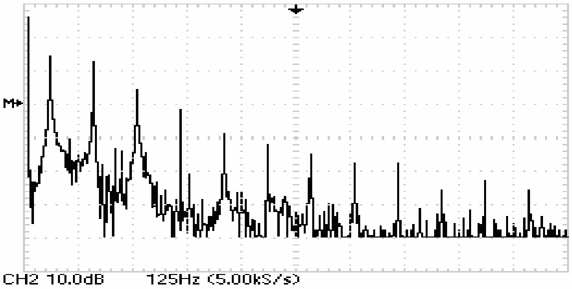

Fig.23 Harmonic spectrum of the nonlinear load current Y=10dB/div; X=125Hz/div

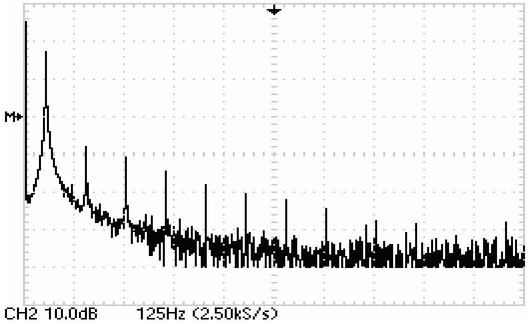

Fig.24 Harmonic spectrum of the nonlinear load current Y=10dB/div;X=125Hz/div

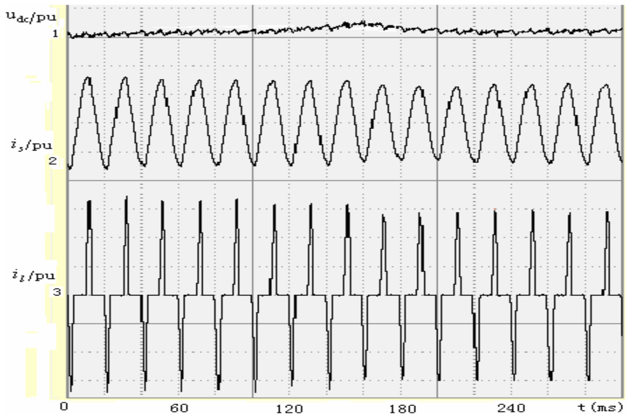

Fig.25 transient state performance: Tr1:DC-bus voltage (50v/div); Tr2:source current (10A/div);Tr3:load current (10A/div) time scale =5ms/div

5 Conclusions

A new type of single-phase shunt APF technique is proposed in this paper. The cycle discrete controller is used to simplify the APF control structure and to realize the linear control for the DC-bus voltage. The merits of this APF are:(a)Simplified the calculation of the active component of load current.(b)The control of DC-bus voltage is linear.(c)The AC source current maintain sinusoidal, even during the variation of load current.(d)system is stable under large fluctuation in load current. The feasibility of the above scheme is verified by PSCAD/EMTDC simulation and experimental results.

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