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A HIGH FREQUENCY HYBRID CHAOTIC OSCILLATOR

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Abstract - This paper reports the experiments of a high frequency Digital Signal Processing chaos generator. Many methods have been proposed in analog domain. However the high accuracy matching of the transmitter and the receiver, especially in high frequencies, is difficult to achieve in real systems. In the other hand high speed digital signal processing technology is bandwidth limited in high frequency applications like wireless LANs, mobile communications, e.t.c. To overcome the above deficiencies of the above technologies the proposed circuit merges the two domains in hybrid integration.

1. Introduction

Recently, using chaos for secure communications has become very popular. The theoretical background of this idea originates from the chaos synchronization concept proposed by Pecora and Carroll [1] [2]. The proposed systems work at laboratory level and with computer simulation. Furthermore the majority of the methods that have been proposed in this field, use analog circuits [3,4,5]. However, one major deficiency of these methods, is that both the transmitter and the receiver should be very accurate, in order to achieve synchronization. This means that the recovery characteristics of the analog circuits are very sensitive to parameter mismatch between transmitter and receiver. Besides, demodulation performance degrades severely due to gain reduction of the transmitted chaotic signal. Note that, the required mismatch of parameters should not exceed 1-2 % [6] [7]. Moreover, technological and temperature discrepancies of analog components of the transmitter and receiver circuits will cause additional difficulties in practical realization of such communication systems. Therefore, analog implementation seems very difficult thought not impossible.

From this point of view, digital processing seems rather attractive to avoid the tiresome routine of the circuit adjustments. Discrete time algorithm for quantized amplitude samples can be realized on various platforms: discrete logical elements or integrated logical chips (field programmable gate array, complex programmable logic devices), common microprocessors, or special microprocessor chips, e.g., digital signal processors (DSP). Fixed point DSP seems to be the optimum solution for the real-time information processing because of its simplicity, flexibility in operation and low cost. Its architecture allows us to realize the basic algorithms in the most effective way and to write the processor software in the most convenient manner.

This approach was realized by 16-bit digital signal processors (ADSP-2181), ensuring a high efficiency of 33 MIPS, along with a codec AD-1843, providing an additional opportunity of analog-to-digital and digital-to analog conversion up to 44 kHz..

The restriction of accuracy, that is caused by the transition from an infinite set of numbers to a finite set, in the case of chaotic systems, results in a specific set of conditions, that means that a chaos becomes a quasichaos. For the given processor 16-bit representation of data is chosen and the sequence period in the case of N variable does not exceed 2_{16}*N. For example, for 1-D map period of a sequence is less than 65536. However, in real system the exact transmission of 16-bit is provided by the channel with a level of noise less than -96 dB, which even though is small, in the real channel always breaks periodicity.

The use of a digital signal processor for chaos generation can produce casual signals but they are very processing power consuming and the analog to digital converter is bandwidth limited. As a solution, here is proposed the creation of a chaotic carrier using a digital processor. Then, the digital chaotic signal modulates an oscillator's signal, in order to transport the chaotic spectrum in a region of higher frequencies.

2. System Description

The digital system that produces the chaotic signal is described by the following set of equations :

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$$x_1(n+1) = g_1(x_1(n)) + s(n) + \theta_c \quad (1)$$

$$x_2(n+1) = g_2(x_2(n)) - \alpha x_3(n) + x_1(n+1) + \theta_M \quad (2)$$

$$x_3(n+1) = x_2(n) - \beta x_1(n) \quad (3)$$

Where,

$x_k(n): k = 1,2,3,4,5:$ Internal states of the chaotic neurons.

$g_1(*), g_2(*):$ Nonlinear functions.

$\theta_M, \theta_C:$ Threshold values.

The most important parameter which describes the characteristic of this system is combination of the nonlinear functions $g_1(*)$ and $g_2(*)$. Besides, the threshold values θ_M and θ_C are used to ensure the chaotic behavior of $x_k(n): k = 1,2,3,4,5$

The general overview of the hybrid chaotic oscillator is presented in figure 1. One of its main components, the D.S.P. Chaos Generator is responsible for the algorithmic realization of the above discrete system (1),(2),(3), using a digital processor. A high-frequency stable signal is produced by the PLL (Phase Locked Loop), using a crystal-based oscillator. In the mixer, the chaotic signal modulates the high-frequency signal, while the filter cuts-off the high-order frequencies.

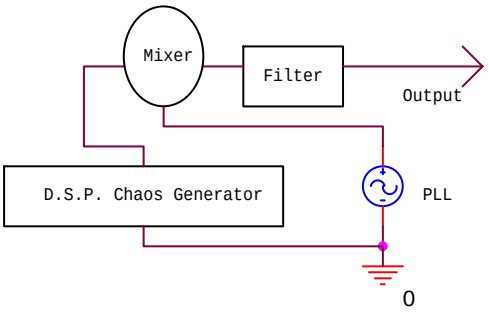

Figure 1. Block Diagram of High Frequency Chaos Generators

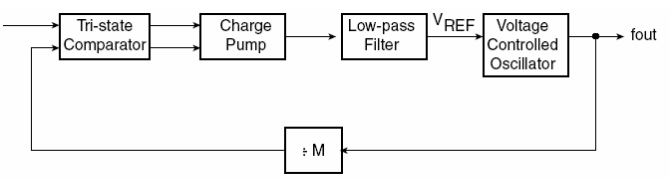

Figure 2. Block Diagram of Phase Locked Loop

A phase locked loop is made up of four blocks: Phase comparator, which measures the phase difference between two clocks, one of which is the reference clock (crystal base), provided externally.

- Charge pump and loop filter, which converts the phase comparison results into a command for the VCO.
- VCO, which creates the carrier.
- The divider, which creates a divided clock from the derived clock. This divided clock is compared with the reference clock.

The schematic in figure 2 represents the internal structure of the PLL.

3. Experimental Data

In figure 3, the output signal x_2 of the digital discrete system (eq. (2)) in time domain, is presented. Here, the non-periodic behavior of the system can be clearly observed.

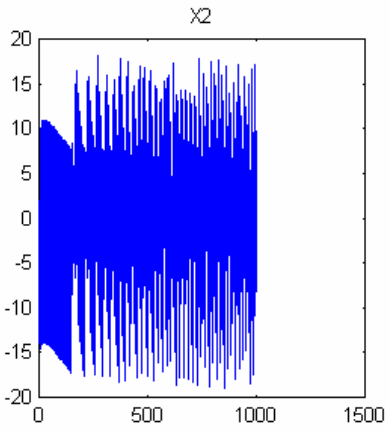

Figure 3.Time domain Output of x_2.

Moreover, the signal x_3, in time domain, that is described by equation (3) can be seen in figure 4.

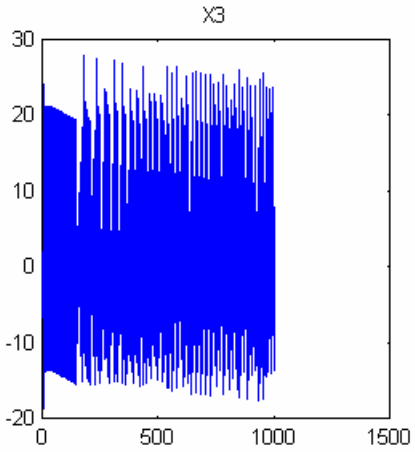

Figure 4.Time domain Output of x_3.

The figures 5 and 6 present the relative imaging of the output signals, for the pairs x_1, x_2 and x_2, x_3 respectively.
Note, that there are regions where almost all the values are possible outputs of the system. This is the main characteristic that distinguishes the chaotic behavior of the discrete digital system.

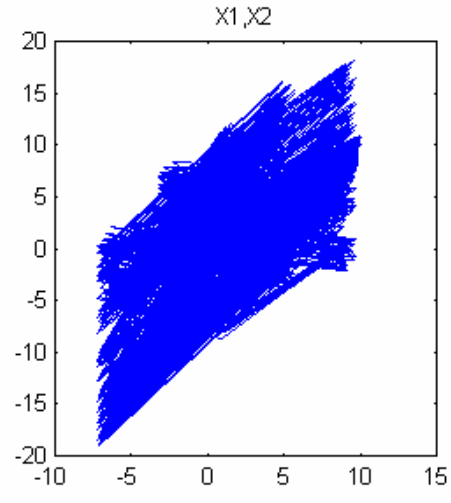

Figure 5. Lissajou Output of x_1, x_2.

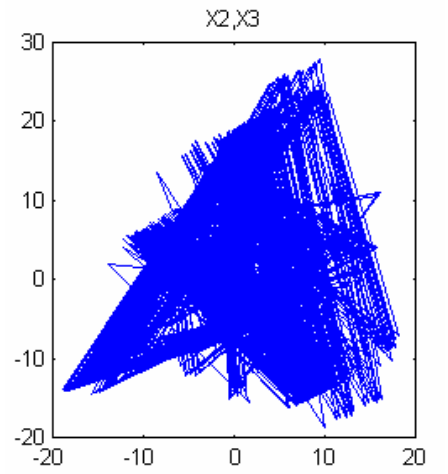

Figure 6. Lissajou Output of x_2, x_3.

Finally, in figure 7, the frequency characteristics of the output signal, after the base band, chaotic signal was transferred in a higher frequency band. Note that the continuous frequency information is the main indication of the chaotic behaviour.

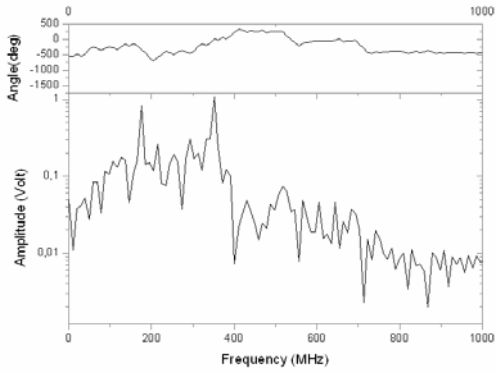

Figure 7. Output Spectrum

4. Conclusions

A Hybrid Chaos Generator has been designed to be capable of producing large numbers of chaotic signals. Another advantage of the presented circuit design is the relative ease of its actual construction and also its potential use in a wide variety of aplications in chaotic communication schemes, as the main functional element of chaotic oscillator. Finally electronic control of the chaotic carrier by the D.S.P circuit greatly facilitates the use of chaotic frequency modulation methods.

5. References

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