Serial to Parallel Conversion of Pulse-rate Signals using Binary Rate Multiplier Principle

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Abstract: - A novel representation of process variables as frequency signals is presented in this paper. Traditional analog computers and transfer function analyzers built using the binary rate multiplier principle did not explicitly consider negative numbers. It is proposed to introduce a two-pin system in which the sign of the variable is made available as 1-bit data on one pin and a series of pulses, whose frequency is proportional to the magnitude of the variable on another pin. Using this concept, the binary rate multiplier had been redesigned to accept signals of both the polarities. Integrators can be constructed, feedback of a variable can be realized and summing operation could be performed easily using this new representation.

Key-Words: - Binary Rate Multiplier, Data Converter, Rate Signal, Polarity Signal

1 Introduction

A novel representation of process variables as frequency signals is presented in this paper. Ordinarily positive numbers can be directly translated into a pulse frequency or rate signal. Negative numbers can be represented by the application of a positive bias. In analog computers and transfer function analyzers, which were built using the binary rate multiplier principle, negative numbers were not explicitly considered. It is proposed to introduce a two-pin system in which the sign of the variable is made available as 1-bit data on one pin and a series of pulses, whose frequency is proportional to the magnitude of the variable on another pin. Section 2 gives a brief overview on the working of a Binary Rate Multiplier. Section 3 introduces the new 2-pin representation and the redesigned summer, difference elements and the integrator units. A serial to parallel converter which helps us in visualizing such variables is detailed in Section 4. Section 5 concludes this paper by looking at possible future work.

2 Binary Rate Multiplier

A binary rate multiplier is used for scaling down the frequency of a pulse stream by a specified fraction. The non-carry pulses (1→0) from the serializing counter and a value set in an Up-Down Counter (register content) serve as the inputs. The output is a series of pulses whose frequency is proportional to the product of input pulse rate and the register content. The block diagram of the Binary Rate Multiplier (BRM) is shown in Fig.1. The register has a maximum storage capacity of (2^n-1) where 'n' is the number of stages in the Up-Down counter. The output non-carry pulses of the serializing counter of each stage and the value in the corresponding stage of the register are processed by an 'AND' gate and the 'n' outputs of these 'AND' gates are processed by an 'OR' gate to get the output of BRM.

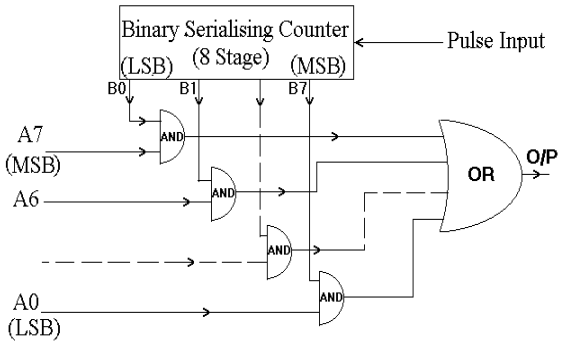

Fig.1 Binary Rate Multiplier

Fig.2 shows the input and subsequent division waveforms of a 3-stage binary counter. It is seen in Fig.2 that pulses derived from the non-propagating (1→ 0) transitions of any one counter stage do not coincide with those from any other stage and that their frequencies are binary weighted. This makes it possible to derive a combination of counter stages to yield any number of output pulses (0, 1, 2, 3….7) in a cycle of operation.

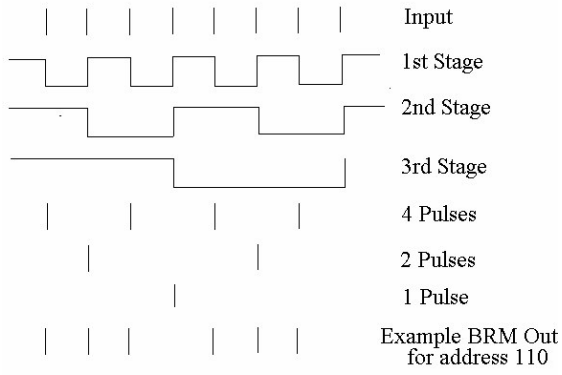

Fig.2 BRM Input-Output Signals

3 Two-pin Variable Representation

In this 2-pin system, the sign of the variable is represented as a 1-bit data on one pin and a series of pulses on the other pin representing the magnitude of the variable as a frequency. The binary digit '1' is used for representing negative sign and '0' for positive sign. The 2-pin representation of +6 and –3 are shown in Fig.3. The new scheme for integrators, summing, difference element is described below.

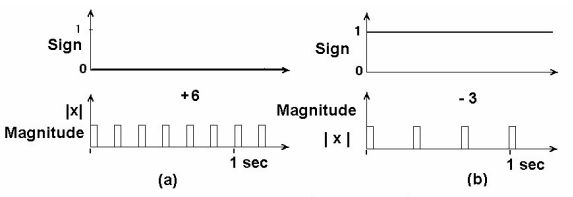

Fig. 3. Sign Magnitude Representation

3.1 Summer

The summer block is used to add the input pulse trains. The block diagram is as shown in Fig. 4. The summer has to consider the polarity of the incoming signals while generating the output pulse streams. Thus, there are four inputs to the summer block namely, the two input pulse streams and the polarities of each of these streams. Similarly, the output consists of the output pulse stream (magnitude) as well as the polarity.

Fig 4

1. If the pulses from the two input streams are non-coincident and have a positive polarity, then the output polarity set to '**0**' indicating a positive output pulse stream frequency.
2. Similarly, if the pulses from the two input streams are non-coincident and have negative polarity (active high) then the output polarity also set to '**1**' (the output pulse frequency then has a negative polarity) and all the pulses are passed.
3. If both a positive and a negative pulses are present at the same instant, then the resultant output is zero and the output polarity is irrelevant (default '**0**').
4. If one of the pulse streams is positive while the other is negative, and if the pulses are not coincident, then all the pulses are passed with the output polarity equal to the polarity of whatever input pulse which is being passed at that instant.
5. If two input pulses are coincident and are of the same sign, an extra pulse is generated and passed to the output immediately after the pulse corresponding to the input. The sign of both the pulses is the same as the sign of the input pulses.

The various cases are illustrated in the Fig: 5

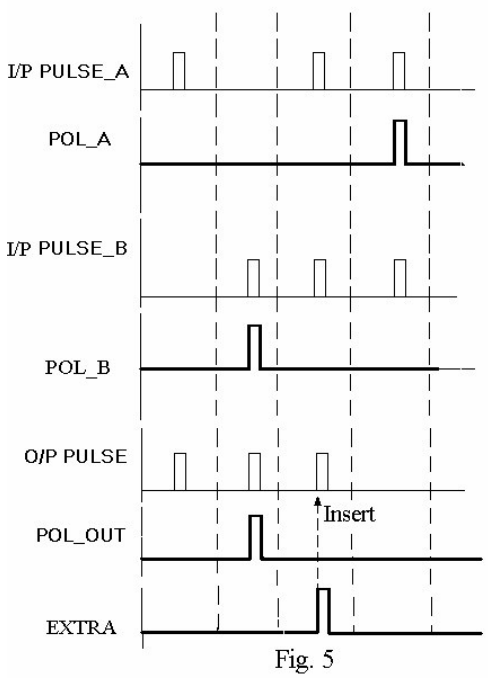

Fig. 5

3.2 Difference Element:

The difference element acts like a summer element except that the polarity of one of its input signals is reversed and then added to the other signal. The block diagram is as shown in Fig. 6.

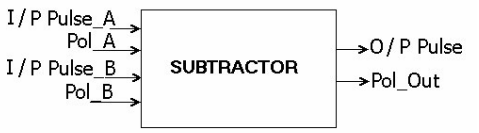

Fig. 6

1. If the pulses from two inputs are coincident and are of same polarity the output is zero.
2. If the pulses from the two input pulse streams are coincident and are of opposite polarity the output pulse is OR operation of two pulses; further, an extra pulse will be generated and passed to the output. The polarity of these two pulses is same as I/P Pulse_A polarity.
3. If the pulses from two input pulse streams are non-coincident, the output pulse stream will be simple OR operation of the two input pulse streams but the polarity at every instant depends on which signal is passed on to the output, at that instant. If I/P Pulse_A is present the output polarity is same as the input polarity. If I/P Pulse_B is present, the output polarity is the complement of the input polarity.

3.3 Integrator:

A counter performs the operation of integration in pulse rate systems. It accepts the input pulse stream and generates an 8-bit value corresponding to the integral of the input. However, it has not been possible to represent negative values as a pulse stream frequency. To overcome this difficulty, the concept of polarity of the rate signal was introduced. This polarity signal can be used to specify whether a rate signal is a positive pulse stream (high) or a negative pulse stream (low).

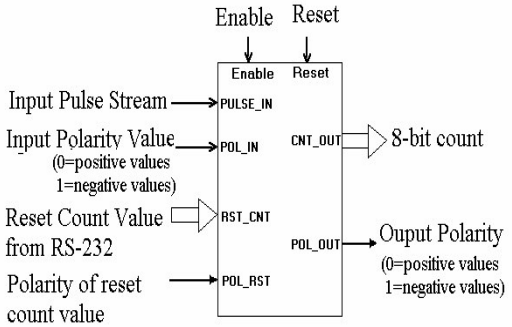

Fig. 7

Using the concept of polarity we state that:

(i) The counter must count up when:

1. Both the input and the output streams are of positive polarity.
2. Both the input and the output streams are of negative polarity.

(ii) The counter should count down when

1. The polarity of the input is positive and that of the output is negative.
2. The polarity of the input is negative and that of the output is positive.

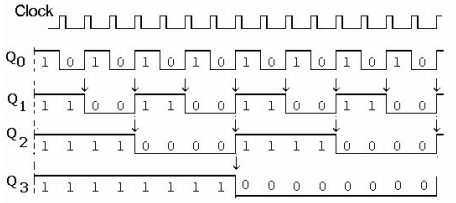

Fig.8 4-bit U/D Sync.Counter Timing Diagram

Every stage of the U/D counter Changes State at the rising edge of the preceding stage, synchronously with the clock's rising edge as shown in Fig.8

4 Serial to Parallel Converter - An Interesting Application

The pulse rate signal with sign however cannot be easily visualized. If a "**steady**" pulse rate signal of any polarity could be converted into a ***steady byte*** or a word, it would be easy to display it using a digital display system or even a D/A converter. We will

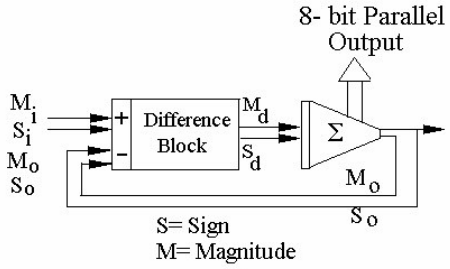

Fig.9

assume that the pulse rate is reasonably steady and any changes are only gradual.

4.1 Results:

The entire arrangement was simulated using Modelsim software.

For various input frequencies the resulting byte (see table in Fig.10) was found to be reasonably stable.

The transient response to step frequencies S_i, eventually converted to parallel data in the U/D counter is shown in Fig.11.

$f_i = 10^3$ Pulses/sec	Steady Byte
24.44	1
48.80	2
97.60	8
195.3	14
390.60	31
781.25	60
1562.50	116
3125.00	217

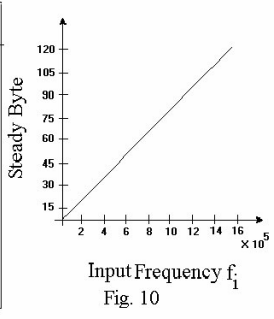

Fig. 10

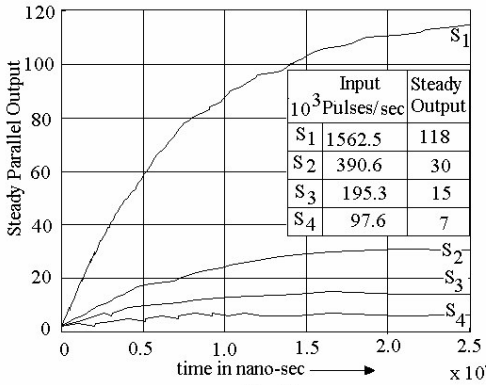

Fig. 11

4.2 Analysis

The block diagram shown in Fig 12 describes the serial to parallel converter as a block schematic in the z-domain. The time constant of the converter can be derived from system parameters as follows:

Serializing Counter: $f_s = 12.5$ MHz

Period = 0.08 µs = 80ns

Size of Integrator = 10 bits

A separate 1-bit Flag is used for representing the polarity for the Integrator Register.

Normalized Open Loop BRM output Frequency

$$F_0 = \{ f_o / f_s \} = [m / (N+1)]$$

Where,

m = Content of Integrator

N = Maximum Value that can be stored in the Integrator-register = 2^{10}-1.

Assuming that all frequencies are normalized to Serializing Counter-Frequency. i.e., T= 80ns

$$\frac{G(z)}{1+G(z)} = \frac{\frac{k}{z-1}}{1+\frac{k}{z-1}} \qquad \frac{\frac{1}{1024}}{z-\left(\frac{1023}{1024}\right)}$$

$$e^{-aT} = \frac{1023}{1024} \; ; \quad a = \frac{-\log_e(1023/1024)}{80 \, x \, 10^{-9}}$$

Time constant of the Serial to Parallel Converter =

$$\frac{1}{a} = \frac{80^{-9}}{9.77 \, x \, 10^{-4}} \approx 82 \, \mu s$$

This had been verified from the simulation output for a step like frequency input for which the converter works like a Low Pass Filter with a time constant of about 80 µs.

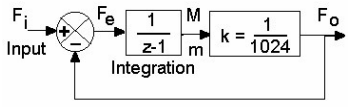

Fig.12. Equivalent Block Diagram

5 Conclusion

The concept of two-pin representation of signals of both positive and negative polarities has been presented with the Binary Rate Multiplier as an integrator. The modified integrator accepts signals of both the polarities and gives out signals with magnitude as well as polarity. These elements were used for making a converter, which will give out a steady parallel byte when the input is effectively, a constant pulse-rate signal. This principle can be further extended for control applications.

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