Electromagnetic Compatibility of Connecting-lead Systems in Integrated Circuits

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Abstract: - The electromagnetic compatibility (EMC) is one of the most important reliability parameters of electronic systems and devices. When EMC effects are properly taken care of during the design, the additional work and expense will return handsomely in a better reliability and competitiveness of the final product. Integrated circuits in high level integration technologies require multilayer connecting lead systems employing high lead density and resulting in diminishing distances between individual leads. The small distances result in increased signal crosstalk inside the integrated circuit. By applying a method of crosstalk prediction in digital circuits using simple passive LCR circuit models.

Key-Words: - electromagnetic compatibility, integrated circuit, microsystems, crosstalk, parasitic coupling

1 Definition of the problem

For optimum efficiency of electronics systems composed of both analog and digital circuits it is required that the changes of states of the active devices are performed as quickly as possible. The rapid variations of voltage and the resulting rapid variations of current create time-variable electric and magnetic fields around the devices and, even more important, around the connecting electric leads. These fields can cause operational faults in the system itself as well as in electronic systems located in close vicinity, sometimes even at larger distances. A similar behavior with just minor differences appears in analog or mixed-signal systems and devices. Software tools kept emerging lately, permitting relatively detailed simulations of the effects connected to the propagation of time-variable signals along lines inside integrated circuits. Unfortunately, in practical application these tools have proven to be rather inaccurate. Of course the accuracy of simulation procedures is limited when applied to real situations due to, among others, the degree of knowledge of the physical parameters of the simulated system. The designer only rarely knows these parameters accurately enough even in passive and active electronic devices while even fewer data are usually available for the ICs proper. Yet, in terms of mutual influencing, the material parameters and details of processing of the ICs have a paramount importance. In order to simplify the simulations of electronic systems on ICs we have designed a method of forecasting the parasitic mutual couplings in an IC using simple circuit models of connecting lines with crosstalks. These models can be inserted in the electrical circuit connections of the systems to be simulated and so the crosstalk effects in well-defined digital systems can be analyzed.

2 Solution

The electromagnetic couplings cause a transfer of interfering energy from the interference source (transmitter) to the interference receiver. Parasitic couplings may be created by designs that are unsuitable in terms of the EMC. According to the prevailing type of coupling, the parasitic couplings can be divided in categories:

- galvanic
- capacitive
- inductive
- by radiated electromagnetic field.

Only two categories usually appear as critical in the integrated circuits, namely the capacitive and the inductive couplings. Galvanic coupling between individual leads is usually totally negligible due to the high resistivity of the silicon oxide and the coupling through radiated electromagnetic field applies to distances comparable or larger than the free-space wavelength of the interfering spectral components and, consequently, usually presents no problem in ICs.
We have chosen four typical representative variations of mutual influencing and their models:

3 Parameters of the signal lines

It is necessary to find the primary electrical parameters of the lines in order to be able to design modeling circuits of particular lines on ICs. During the process of extraction of the line parameters the parasitic couplings are transformed to elementary electrical elements. The capacitive coupling is transformed into an ideal capacitor and the inductive coupling into ideal inductors with mutual inductance [5]. The overall accuracy of forecasts of parasitic couplings depends on the accuracy of electrical values extraction of individual elements modeling the couplings. In some cases, when it is not necessary to find accurate values of individual coupling parameters between the lines, we may use empirical formula to find their values [2]. Since the accurate finding of parasitic couplings is an extremely time-consuming procedure, it is reasonable to use simplified formulae for the first approximation. The parameters found by this method are then set into the simulation models and some improved-accuracy method has to be used for the vicinity of the disturbance only when a significant disturbance state appears at a particular spot of the circuit.
Numerical modeling presents one of the methods of rather accurate calculation of the values of individual elements. For example, the method of finite element variations was used to model the electrostatic fields. One of the results of the electric field distribution modeling are the calculations of electric induction flux and capacitances between individual conductors of the model derived from them (see Fig. 1 and 2).

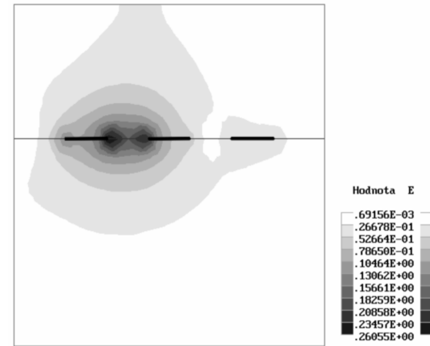

Fig. 1: Electric field distribution of a triple-conductor line

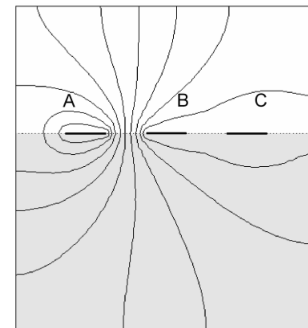

Fig. 2: Electric potencial of a triple-conductor line

4 Capacitive coupling

The capacitive coupling is the predominant type of coupling in high-impedance circuits, like NMOS and CMOS IC's. Fig. 3 shows the way of transforming the capacitive coupling between conductors inside an IC to ideal capacitors [1]. The C_S capacitors represent the capacitive coupling between particular leads and the substrate; the substrate is usually connected to common ground or a power supply lead, depending on the particular IC fabrication technology. The capacitor C_V represents the capacitive coupling between individual leads inside the IC. In Fig. 3 the interference source lies in the IC1 gate, creating a rectangular signal waveform in the active part of the line. The IC4 is the interference receiver, having a logic "0" at its input when there is no interference present.
Figure 4 shows a twin lead line inside an integrated circuit in 2.4 μm Mietec CMOS technology. The lead dimensions correspond to the design rules for this technology.
Further there are indicated the leads parasitic capacitances: C_C – the mutual capacitance between the A and B a twin line leads, and C_S – the lead-substrate capacitance, all according to the simplified equivalent circuit (Fig. 3).

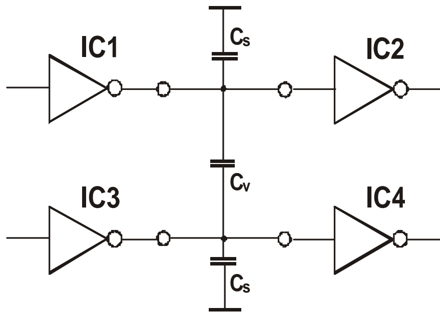

Fig. 3: Equivalent circuit of a capacitive coupling between leads inside an IC

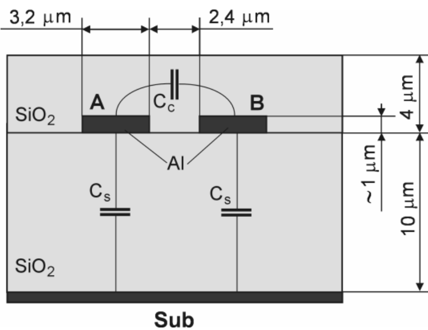

Fig. 4. A twin line in a Mietec 2.4 μm CMOS IC; the leads are aluminum tracks inside the SiO_2

5 Simulation

The actual magnitude of crosstalk between leads inside an integrated circuit depends on the geometric parameters of the line and on the electrical parameters of gates connected to the line.

Most of the geometric parameters of the line are usually predetermined by the design rules of the particular technology. The electrical parameters of the gates are bound to the standard digital cell libraries and the designer can only select from a limited assortment of available digital cells.

In general, it can be expected that the crosstalk magnitude will rise with increasing length of mutually influencing leads. Results of parametric simulations for various line lengths are shown in Fig.6. The graphs show the time-dependent voltage at the far end of the non-active line. A non-active line in an interference-free situation is assumed to be in the state of logical zero. The interfering impulses are transferred by parasitic capacitive coupling. The interference source was a CMOS gate-driven line, with the gate operating off a $U_{CC} = 5V$ power supply, generating a rectangular waveform signal (Fig. 5).

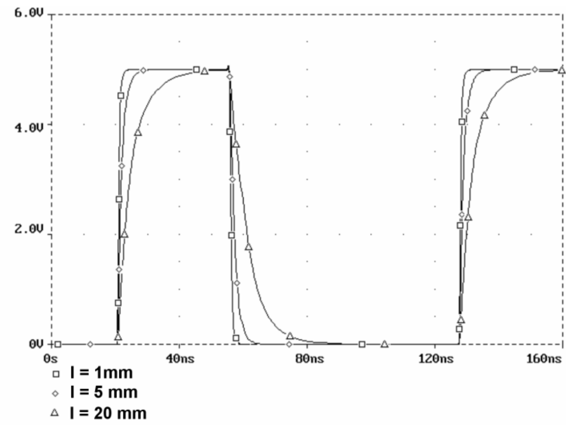

Fig. 5. Waveforms at the far end of the active (interfering) line.

Plotting the parametric simulation results in a graph showing the interfering pulse amplitude versus line length (Fig. 7), we can see that the crosstalks indeed rise with increasing line length but that the rate of rise drops. It can be stated that the amplitude of the interfering pulses is asymptotically approaching a certain maximum value.

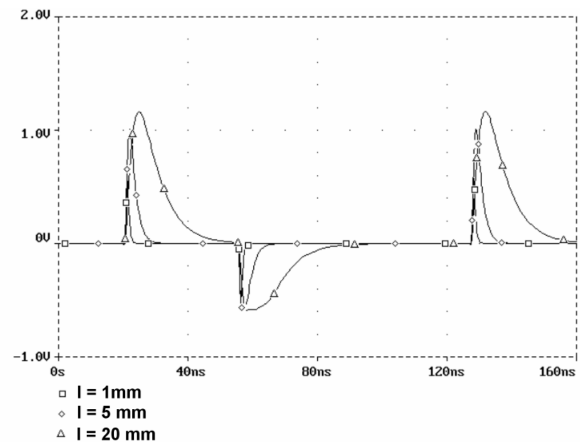

Fig. 6. Waveforms at the far end of the non-active (interfered) line.

6 The limit case

In order to be able to derive the maximum crosstalk amplitude regardless of the line length it is necessary to adjust the simplified IC twin-lead line equivalent circuit (Fig. 3) into a form permitting to set up the crosstalk transfer function. This equivalent circuit adjusted for AC crosstalk analysis (Fig. 8) contains capacitances C_V and C_S with the same meaning as in Figs. 3 and 4, the capacitance C_S must also include input capacitances of the gates connected to the line.

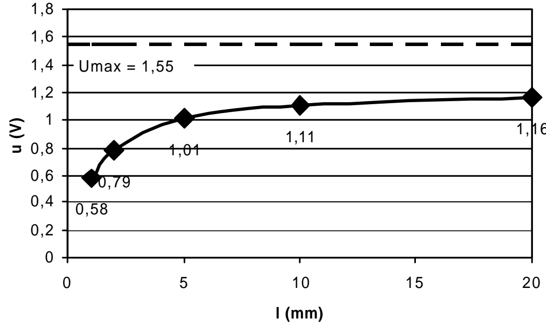

Fig. 7. A plot of interfering impulse u versus line length l.

The driving CMOS gates connected to the line were transformed to resistors with a value R, representing the actual resistance of the MOS transistor in the "on" state [4].
The interference source is represented by the driving gate connected to the active line, in this case a U_Z voltage source while the interference receiver is a gate connected to the far end of the non-active line, in this case the interference is represented by the U_P voltage.

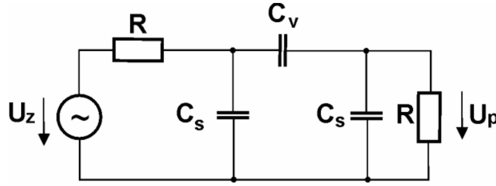

Fig. 8. Adjusted equivalent circuit for A.C. analysis

The adjusted circuit (Fig. 8) was used to set up the crosstalk transfer function (1) in the form of a ratio of the U_P voltage at the interference receiver input to the U_Z voltage from the interference source. It is also possible to consider this transfer function to be a coupling coefficient showing the measure of coupling between the interference receiver and transmitter.

$$P = \frac{U_P}{U_Z} = \frac{jwRC_V}{-w^2R^2C_S(C_S+2C_V)+2jwR(C_S+C_V)+1} \quad (1)$$

Differentiating the transfer function P against the angular frequency ? we can find a local maximum and so find the critical frequency $?_0$ for which the maximum transfer takes place. By setting the $?_0$ frequency into the transfer function equation (1) we can find the maximum transfer P_0.

$$P_0 = \frac{1}{2}\frac{C_V}{C_V+C_S}, \quad (2)$$

$$w_0 = \frac{1}{R\sqrt{C_S^2+2C_SC_V}} \quad (3)$$

Cv [fF/μm]	0,69
Cs [fF/μm]	0,42
R [Ohm]	1740

Tab. 1. Typical values of the coupling capacitances and output resistance of the CMOS gate

No resistances *R* appear in equation (2). From that follows that a long as the driving gates connected to the interfering and interfered lines have the same internal resistance, it will have no effect on the maximum coupling coefficient.

7 Conclusion

Applying the equation (2) and table 1 to a particular twin-lead line in an IC, according to Fig. 3, it is possible to determine the maximum value of inter-line crosstalk. The numerical values of parasitic capacitances C_V and C_S were found with the aid of finite-element modeling of the electric field distribution [3]. By application of this method it is possible to forecast the maximum value of crosstalk between connecting lines inside an IC without the need to resort to time-consuming analog simulations respecting the parasitic coupling effects.

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