Symbolic Analysis of Switched-Mode DC-to-DC Converters

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Abstract: A method of modeling PWM switches for symbolic analysis of pulse-width-modulated (PWM) dc-to-dc converters operating in the continuous conducting mode (CCM) is described for switches with both fixed and modulated duty ratio. The well-known average models of PWM switch according to Vorpérian are implemented by means of modified nodal analysis into the SNAP program to analyze transfer and immittance functions, especially the line-to-output and control-to-output transfer functions in the symbolic and semisymbolic forms, and the corresponding frequency responses. An example of the analysis of boost converter is shown.

Keywords: - PWM converter, PWM switch, CCM, symbolic analysis, SNAP

1 Introduction

The method of modeling DC-to-DC converters via average models of the PWM switch [1-4] is widely used in a few modifications for effective computer analysis of small-signal AC analysis, as well as the transient and DC analyses. Its main benefit is the easy implementation of the switch model into the SPICE-family circuit simulators [5]. However, these programs, based on conventional numerical algorithms, do not generate – with a few exceptions – some outputs, which are often required, especially for AC analyses of line-to-output and control-to-output behavior: zeros and poles of transfer functions and these transfer functions in the symbolic form, i.e. in the form of formulas. To obtain them, one has to perform complicated analytical calculations [3]. The availability of such "hand-and-paper" procedures is strongly limited by the complexity of the converter model.

In the paper, the procedure of analysing the PWM-circuits by symbolic-oriented circuit simulators is described. These programs work mostly on the principle of modified nodal approach (MNA), when each circuit component is modeled by its matrix-stamp. The currently available generalized model of the PWM switch generates analysis results that are equivalent to those of the method of state-space averaging [4]. However, this model has to be compiled individually, by inspection the concrete converter topology. In addition, only the switch model with fixed duty ratio is described in [4]. That is why the original Vorpérian switch models [3] seem to be more convenient for automated computer analysis. For these models, the matrices-stamps were compiled and implemented into the component library of the SNAP program [6] for the symbolic, semisymbolic, and numerical analyses of linearized circuits.

The paper has the following structure: In Section 2 following this introduction the conventional average models of the PWM switch with fixed and modulated duty ratio are summarized [3]. In contrast to the original work [3], the notation is slightly modified with regard to the following transcription of the equations into the algorithmic form. Section 3 describes the transformation of these models into the MNA and their implementation into the SNAP. In Section 4, we demonstrate the symbolic and the related analyses of the boost converter. A comparison with analytical results in [3] and with recently published outputs from commercial circuit simulators [5] is given.

2 Conventional model of PWM switch [3]

The pair of so-called active and passive switch, modeled by the commutator in Fig. 1, appears in the basic variants of PWM converters.

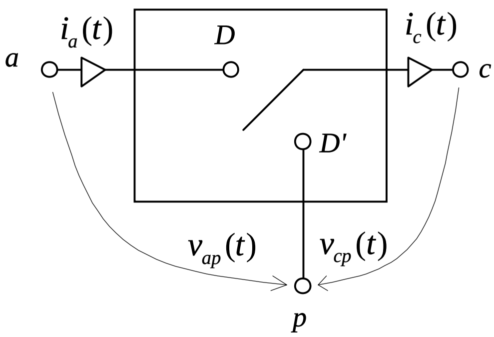

Fig. 1: PWM switch.

The c (*common*) terminal is connected either with the a (*active*, the active switch is on) terminal or with the p (*passive*, the passive switch is on) terminal. The symbol D represents the switching duty ratio, and $D'=1-D$.

As shown in [3], for <u>fixed duty factor $D=D_0$</u>, the average voltages and currents of the switch within each switching period are related as follows:

$$\bar{i}_a = D\bar{i}_c\,, \qquad (1)$$

$$\bar{v}_{cp} = D(\bar{v}_{ap} - D' r_e \bar{i}_c)\,. \qquad (2)$$

Here, r_e is an auxiliary resistance which is generally dependent on the lossy resistance R_c (ESR) of the condenser and on the load resistance R_o. For instance, r_e is given by a parallel combination of two above resistances for the boost and buck-boost converters, and simply by R_c for the Cuk converter.

When the duty ratio is perturbed by deviations $d \to 0$ around its bias value D_0, the branch voltages and currents of the switch will vary around their bias values according to equations $\bar{i} = I_0 + i$, $\bar{v} = V_0 + v$, $i \to 0$, $v \to 0$. The „i" and „v" declinations are described as follows [3]:

$$i_a = D_0 i_c + dI_{c0} \qquad (3)$$

$$v_{ap} = \frac{v_{cp}}{D_0} + r_e D_0' i_c - \frac{V_D}{D_0} d\,, \qquad (4)$$

where

$$V_D = V_{ap0} + (D_0 - D_0') r_e I_{c0}\,. \qquad (5)$$

DC values, i.e. bias values of the operating point, are labeled by suffixes „0".

Eqs. (1) and (2) are starting points for modeling the switch with fixed duty ratio. This model can be used e.g. for computing the line-to-output transfer function. The switch with modulated duty ratio will be modeled by Eqs. (3)-(5), especially for computing the control-to-output transfer function.

3 PWM switch and its matrices - stamps

Let us regard the PWM switch as a floating three-terminal device in Fig. 2. The voltages and currents are given in the operator form (they are labeled by capitals). Then Eqs. (1) and (2) of the switch with fixed D can be transposed into an operator-form matrix-stamp as follows:

I_1					D	V_1	(6)
I_2	=				-1	V_2	
I_3					D'	V_3	
0		$-D$	1	$-D'$	$r_e DD'$	I_c	

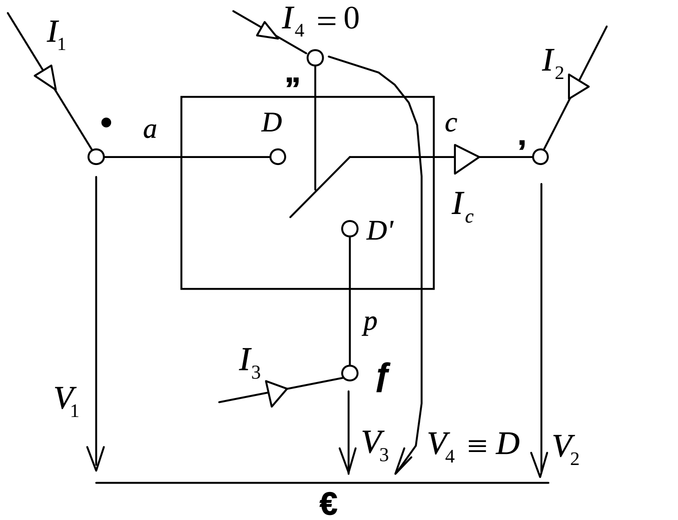

Fig. 2: PWM switch as a floating three-terminal device (fixed D) or a four-terminal device (modulated D).

The first equation for current I_1 is a transcription of Eq. (1). The second equation for current I_2 states that this current is – except for the sign – equal to current I_c. The third equation represents current balance for node ***f***. The last equation is a transcription of Eq. (2).

For the switch with modulated duty ratio, the model has to be completed with the fourth, the controlling node **„**. The appropriate nodal voltage V_4 will then be made identical with the operator form of the declination d, i.e. D. Current I_4 flowing into the controlling input has to be considered to be zero. The transcription of Eqs. (3)-(5) into the matrix-stamp of the switch with modulated duty ratio is as follows:

I_1					I_{c0}	D_0	V_1	(7)
I_2	=					-1	V_2	
I_3					$-I_{c0}$	D_0'	V_3	
$I_4=0$							$V_4=D$	
0		$-D_0$	1	$-D_0'$	$-V_D$	$r_e D_0 D_0'$	I_c	

The fourth row of pseudoadmittance matrix contains zeros. However, this fact does not represent any problem: After connecting a controlling voltage source to node 4, the simulation program computes the transfer functions from the algebraic minors, which result from omitting row No. 4.

The above matrices-stamps are implemented into the component library of the SNAP program under the names XPWM (switch with fixed D) and XPWMD (switch with modulated D).

4 Demonstration of computer analysis

The results of analytical computations involved in DC and small-signal analyses of a boost converter are given in [3]. Its model in the SNAP program is shown in Fig. 3.

In [5], some outputs of the SPICE – and the MicroCap simulations of this converter are presented. Component parameters are in Fig. 3. The switching frequency is 200kHz and the 2.8V input voltage should be converted to an output voltage of 6V.The duty ratio used is D = 1/1.875 = 0.533.

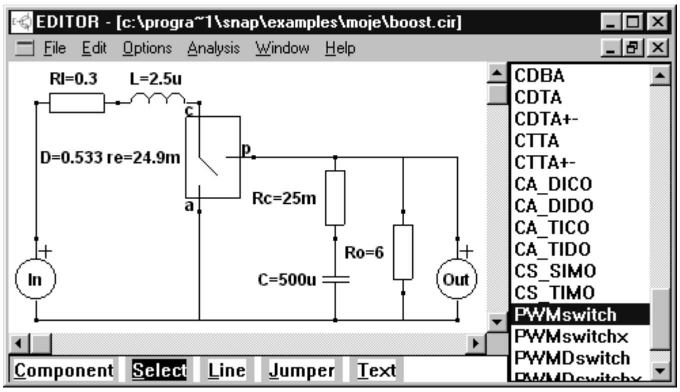

Fig. 3: SNAP model of DC-to-DC converter.

The auxiliary resistance r_e is given as a parallel combination of R_o and R_c, i.e. approx. 24.9Ω. The switch with fixed duty ratio in Fig. 3 is modeled by a pair of parameters D = 1-D‘ and r_e (see also Eqs. 6). Selected results of the analysis are given below:

Voltage Gain (open output):

_____________symbolic__________________
Ro*Di
+s*(C*Rc*Ro*Di)

D*Di*re +Rl +Ro*Di^(2)
+s*(C*Rc*Rl +C*Rc*Ro*Di^(2) +C*Ro*D*Di*re
+C*Ro*Rl +C*Rc*D*Di*re +L)
+s^(2)*(L*C*Rc +L*C*Ro)

____________semisymbolic_______________
Multip. Coefficient = 4.65062240663900E+0003
8.00000000000000E+0004
1.00000000000000E+0000 * s

2.14404233546888E+0008
1.24982944431369E+0005 * s
1.00000000000000E+0000 * s^(2)

_______________zeros___________________
-8.00000000000000E+0004

_______________poles___________________
-1.23243261211045E+0005
-1.73968322032420E+0003

Results can be interpreted as equations of the line-to-output transfer function including its zeros and poles.

For instance, the DC voltage gain (for s = 0) can be obtained from the above formula:

$$\left.\frac{V_{out}}{V_{in}}\right|_{DC} = \frac{R_o D'}{R_l + D'(r_e D + R_o D')} \doteq 1.735 .$$

This result is in accordance with [3]. Input voltage 2.8V will be converted to an output voltage of 4.859V.

A simple arrangement of the transfer function leads to the formulae published in [3].
Computing the input impedance yields

Input impedance (open output):

_____________symbolic__________________
D*Di*re +Rl +Ro*Di^(2)
+s*(C*Rc*Rl +C*Rc*Ro*Di^(2) +C*Ro*D*Di*re
+C*Ro*Rl +C*Rc*D*Di*re +L)
+s^(2)*(L*C*Rc +L*C*Ro)

1+s*C*(2*Ro*D*Di +Ro*D^(2) +Rc*Di^(2) +Ro*Di^(2)
+Rc*D^(2) +2*Rc*D*Di)

____________semisymbolic_______________
Multip. Coefficient = 2.50000000000000E-0006
2.14404233546888E+0008
1.24982944431369E+0005 * s
1.00000000000000E+0000 * s^(2)

3.31950207468880E+0002
1.00000000000000E+0000 * s

_______________zeros___________________

-1.23243261211045E+0005
-1.73968322032420E+0003

_______________poles___________________
-3.31950207468879E+0002

Setting s = 0 yields the equation for input resistance

$$R_{in} = R_l + r_e D D' + D'^2 R_o \doteq 1.615\Omega ,$$

which corresponds to [3], the same as the formula of the complete impedance function.

DC current flowing out of the input source I_{in} = 1.734A can be established from the input resistance, and load current I_{out} = 0.8908A can be derived from the output voltage. Then the input power will be 4.855W and the output power to the load will be 4.328W. The corresponding efficiency is 89%. These numerical results are in good agreement with the MicroCap simulation published in [5].

In a similar way, one can obtain other circuit functions such as output impedance including the corresponding

$$\frac{R_o D' + sD' R_o R_c C}{DD' r_e + R_l + R_o D'^2 + s[CR_c(R_l + R_o D'^2 + DD' r_e) + CR_o(DD' r_e + R_l) + L] + s^2 LC(R_c + R_o)} \doteq \frac{5.646x10^3(8x10^4 + s)}{2.970x10^8 + 1.265x10^5 s + s^2}$$

frequency responses. A matter of course is the stepping of component parameters, e.g. duty ratio, and so is the monitoring of the respective influences.

A demonstration of modeling the control-to-output transfer function is in Fig. 4. The switch model with modulated duty ratio is used. This model is identified by four parameters (r_e and bias values of D, V_{ap}, and I_c, see Eqs. 7 and 5).

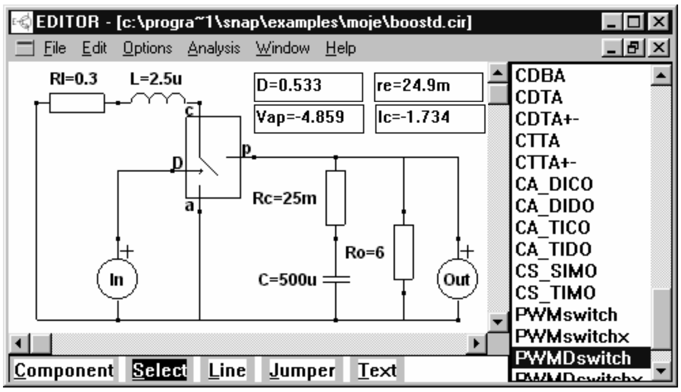

Fig. 4: Modeling the control-to-output transfer function.

The analysis leads to the same denominator and poles as for the line-to-output transfer function. The formula for the numerator is generated as follows:

Ro*Di^(2)*re*Ic +Ro*Rl*Ic -Ro*Di*Vap
+s*(C*Rc*Ro*Rl*Ic -C*Rc*Ro*Di*Vap
+C*Rc*Ro*Di^(2)*re*Ic +L*Ro*Ic)
+s^(2)*(L*C*Rc*Ro*Ic)
________________zeros___________________
-8.00000000000000E+0004
4.01277199188604E+0005

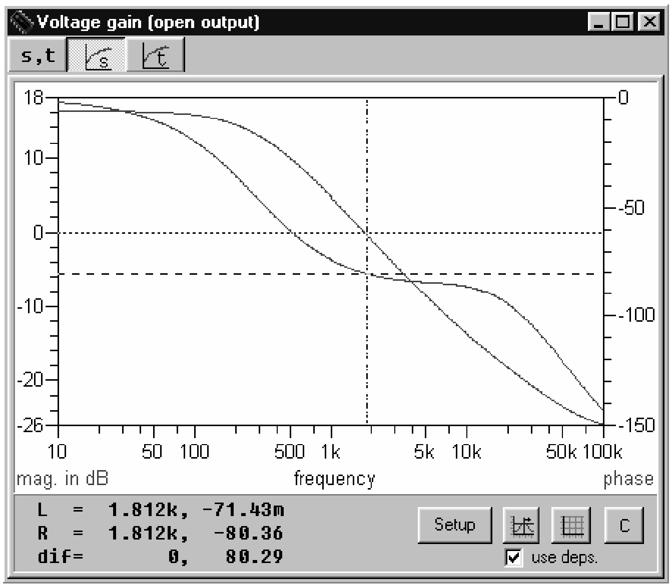

Fig. 5: Control-to-output frequency response.

In accordance with [3], the transfer function exhibits two real zeros. The corresponding magnitude and phase frequency responses are in Fig. 5. The gain crosses 0dB at a frequency of 1.812kHz when the phase shift is –80 degrees, and the phase margin is 100 degrees.

The formula for DC gain in [3] can be derived from our general symbolic result by successively neglecting numerically less important terms. Note that such simplification will cause indispensable inaccuracy.

5 Conclusion

A method of implementing the average models of PWM switch into a program for symbolic analysis is shown. The matrices-stamps of the switch with both the fixed and modulated duty ratios are found. After the inclusion of these models into the component library, one can utilize all the program features to perform the symbolic, semisymbolic, and numerical analyses of various topologies of switched DC-to-DC converters.

Acknowledgments

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