Modern microcontroller building set for teaching and development of industrial applications

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Abstract: - The article describes the concept of the evaluation board based on a single-chip microcontroller (mainly Atmel AT89C51CC01, Atmel ATmega162 and Motorola Star12), developed especially for teaching purposes. The main board can be expanded by supplementary modules - a power module with communication interfaces, and a variety of other modules. This contributes to the flexibility of the whole system.

Key-Words: - microcontroller, module concept, evaluation board, teaching, development

1 Motivation

At the Department of Applied Electronics and Telecommunications, it became necessary to solve the problem of efficiency in the courses devoted to single-chip microprocessors (especially subjects "Industrial Fieldbuses" and "Microprocessors and Microcomputers"). The experimental boards and software tools we had been using became obsolete and the necessity of their fast innovation became imperative. We, therefore, decided to develop a completely new experimental platform with a set of fundamental and expansion modules. We respected the requirement imposed on the new system in the development of more sophisticated applications (advanced courses or diploma projects).

2 Main concept

The fundamental philosophy is to separate the power supply and communication interfaces from the main processor module. This modularity has a lot of advantages, for example:

- all interfaces are galvanicaly separated by optocouplers
- all voltage levels (±5V, ±15V and +12V) are generated by the DC/DC converters
- all processor modules use the same common interfaces
- in the case of failures, it is possible to change only one part

A 50-pin connector „Amphenol"-type was selected due to its mechanical robustness and it connects both parts. The number of pins allows for leading all signals by two parallel wires. It contributes to high reliability in intensive utilization.

3 Power supply module

A power supply module can be powered by a stabilized voltage source in the range of 7 to 12V. We use the supply 12V/2A, which should be sufficient for most of the connected modules. The external power supply can be added for modules with higher power consumption (motor drivers, large LED displays, etc.). A standard stabilizer generates the basic voltage +5V (type 7805 with maximum current 2A). The DC/DC converters generate auxiliary voltages +12V and ±15V with current range depending on the type of a converter (max. hundreds of mA). This power is sufficient to supply the peripherals such as A/D and D/A converters or circuits with operational amplifiers.
A set of serial interfaces on the power supply module provides the following:

- 2 x RS232 - only signals RxD and TxD, both using one converter type MAX232
- 2 x CAN with proper bus drivers
- 1 x RS485 with a proper bus driver

There are two serial interfaces (for supporting processors) and two CAN lines between the processor and the power supply module. The interface (communication connector) can be selected by software or via jumpers. Control signals are connected to selectable microcontroller pins.

It is possible to disable (disconnect) signals from any interface if a user application in the processor module needs the alternative pins for other purposes.
A programmable logic device GAL22V10 controls serial interface circuits. It reduces a number of jumpers to minimum, maintaining full functionality. A pair of triangular LED, which reflects the data flow direction, indicates a data transition.
The new improved version (signed as 1.2) can be alternatively powered directly from the 5V/2A power supplyiesthat are available at laboratory work places. The second improvement adds the new serial interface based on FTDI232-chip to simplify connection with a PC via USB.

4 Processor module

4.1 Design and conception

A processor module conception is independent of the specific single-chip microcontroller type. For correct function of each type of microcontroller, the signals of power/communication connectors (Amphenol-50-M) must be preserved. Peripheral modules can be connected to two ports/connectors with the following groups of signals:

- **Peripherals interfaced directly on port** (2-row connector, 26 pins)
  - power supply ±5V, ±15V
  - 14 (8 + 6) pins connected directly with microcontroller ports

- **Peripherals mapped into memory space** (2-row connector, 40 pins)
  - full set of supply voltages
  - 16-bit address bus
  - 8-bit data bus
  - /CS0 - /CS7 signals decoded from address – 2kB memory blocks
  - signals to access the data memory (/RD, /WR) and code memory (/PSEN)
  - ALE signal for the acknowledgment of address validity (multiplexed address/data)

The signal structure is based on a processor compatible with Intel 8051 type. It is also possible to use control signals typical for other microcontroller families. Peripheral connectors are placed only on one board edge, which allows expanding on other board edges.
The peripheral modules can be concatenated by bus, it is possible to select a concrete module via module select signals (/CS0-7). Peripheral connectors are doubled so that it is possible to create 2 groups of peripheral modules. One of them is connected to the board directly and the second one by a flat cable.

4.2 Processor module with AT89C51CC01

In the first step we selected a product of Atmel from the CANary series as a primary single-chip microcomputer for the processor module. This processor type contains the proven kernel of single-chip microcomputers Intel-8052 with the following peripherals:

- 32kB FLASH memory for application program
- 2kB FLASH memory with a manufacturer Boot Loader. It allows programming of a user FLASH via serial line and software on PC (Boot-Loader exists in version working on CAN bus too)
- 1kB RAM memory mapped as an XRAM memory
- 2kB EEPROM memory
- a 10-bit resolution analog to digital converter (ADC) with 8 multiplexed inputs
- CAN controller fully compliant with CAN Rev 2.0A and 2.0B. CAN signals are attached to the new port P4 (only 2-bits)
- Five-channel 16-bit PCA with PWM (8-bit), high-speed output and timer and edge capture
- package PLCC 44 (with pin layout incompatible with common 8051)

A 32kB SRAM memory is added on evaluation board. It can work in a *standard mode* as a data memory or in an *extended mode* as a code memory. In a *standard mode*, the program (called *Monitor*) is stored in an internal FLASH memory. *Monitor* can load an application program into an on-board RAM in cooperation with any software in a PC terminal. Other functions of the *monitor* are memory dumping and editing. The monitor can invoke the processor RESET and switch the RAM to the code memory mode (*extended mode*). Program is then executed from external memory (using signal /EA similarly to the 8051 standard). Switching back into the *standard mode* is only possible by pushing the RESET button. It is located on the power supply module.
Memory switching is implemented in the PLD circuit Altera EPM7064 (TQFP100 package). Input signals for PLD are full address- and data bus from microcontroller, and all control signals. The PLD generates signals for RAM control, selects signals /CS0-7 for peripherals attached to the peripheral 40-pin connector. The PLD realizes bus demultiplexing, because the x51-series processor uses time-multiplexed address and data bus. The PLD can generate clock signal for processor using a 48-MHz oscillator and a programmable divider. Some functions are controled by the microprocessor by special

registers in the data address space (addresses 0xFFFE and 0xFFFF).
Two LEDs on the processor board indicate memory mode. In the latest version, "AutoBaud" function is implemented, when Monitor adjusts the communication rate of a serial line according to the connected terminal (max. 38400 Bd).

4.3 Processor module with ATmega162

The next processor module is based on ATmega162 from AVR family by Atmel. Main features of Atmega62 are:

- 16kB FLASH memory for program
- 512B EEPROM memory
- 1kB SRAM for data
- External memory multiplexed bus
- JTAG interface for programming and on-chip debugging
- Two 8-bit and two 16-bit timer/counters with capture/compare modes
- Two USARTs and SPI serial interfaces
- 40-pin DIP or 44-lead TQFP package

Besides standard connectors, additional connectors are added on module, namely for JTAG and non-standard hardware connection. Function of shared pins can be selected by jumpers.
Memory bus is demultiplexed by latch 74HC574 and can be found on connector for standard peripheral modules.

4.3.1 Application of LIN bus testing

Another example of the application of microcontrollers in educational process will now be shown. For better imagination how the hardware-in-loop (HIL) testing system works, a simple testing system for LIN bus communication monitoring was developed by students. Electronic control units (ECUs) are connected together via LIN bus and compose the tested system.
The testing system is divided into two main parts, the first one is testing hardware and the second one is testing software. The block diagram of the testing system is shown in Fig.1.
The testing hardware is connected with tested system and allows the LIN bus communication monitoring, stimulating ECUs inputs and timing all of these operations. It is also connected with a PC where the testing software application runs.
The hardware is based on the processor module with Atmega162 mentioned above.
The first of the integrated USARTs is used for LIN bus monitoring, and the second one is used for communication with the PC. One of the 16-bit timer/counters is used for generating the timestamps for operations timing. Remaining parallel input/output ports are used for stimulating the ECUs inputs by means of drivers. The LIN communication protocol is implemented by UART hardware interrupt routine, whereas the interrupt occurs as soon as a byte is received. Communication between testing hardware and the PC uses special protocol and is implemented in the processor by interrupt routines with buffering.
The testing software was developed as a standard Windows GUI application. It allows to control and to evaluate the testing process by stimulating the inputs of ECUs and monitoring messages on the LIN bus. The timestamps of every operation which are generated by testing hardware are used to evaluate timing conditions in tested system.

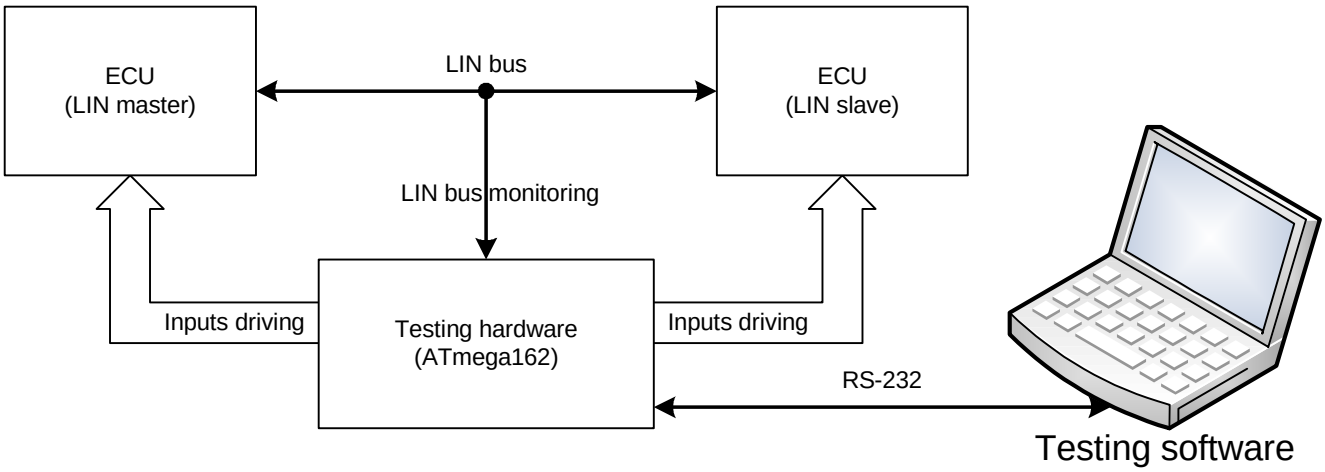

Fig. 1 – LIN bus monitoring system

4.4 Peripheral modules – ports connected

- **Keyboard + speaker** - matrix keyboard with 16 buttons (4x4 bits attached to port P1 of x51-processor), speaker separated by a transistor switch. Pull-up resistors are supposed to be present on processor pins. Jumpers select signal from the processor to the speaker.
- **Bar-graph + PWM** - column of 8 LEDs connected by 74HC245 driver on port P1 + speaker attached to PWM output with RC filter (R and C are variable)
- **Wireless communication 433MHz** - standard modules for transmission and reception are attached to jumpers which select signals

4.5 Peripheral modules – mapped into the memory space

- **Raster LED display** – containing a local controller implemented by a PLD circuit, a module with 32x32, 2-colour LEDs with possible extension up to 2x2 modules. The PLD also contains a video-memory (in RAM cells) accessible as 64 bytes in selected memory space.
- **7-segment LED display** - 8-digit display implemented as a matrix, lower 3 bits of address bus select the driver, data corresponds to 7 LED segments + dot
- **16-segment LED display** - 8-characters display implemented as a matrix, address bit A0 selects segments A-H or I-P, address bits A1-3 select digits, data-bits correspond to segments, too
- **Character LCD display (16 chars x 2 lines)** – standard LCD display with HD44780 controller compatible, address bit A0 selects instruction/data (signal R/S), bit A1 controls read/write (signal R/W on display)
- **Graphic LCD display (128x64 pixels)** – standard LCD display with KS170 controller compatible, address bit A0 selects data/instruction (signal D/I), bits A1. A2 selects video/memory page (signal CS1, CS2 on display)

All modules can be selected by signal /CS0-7. LED segment current is enhanced because LED displays must operate in a time-multiplex mode.

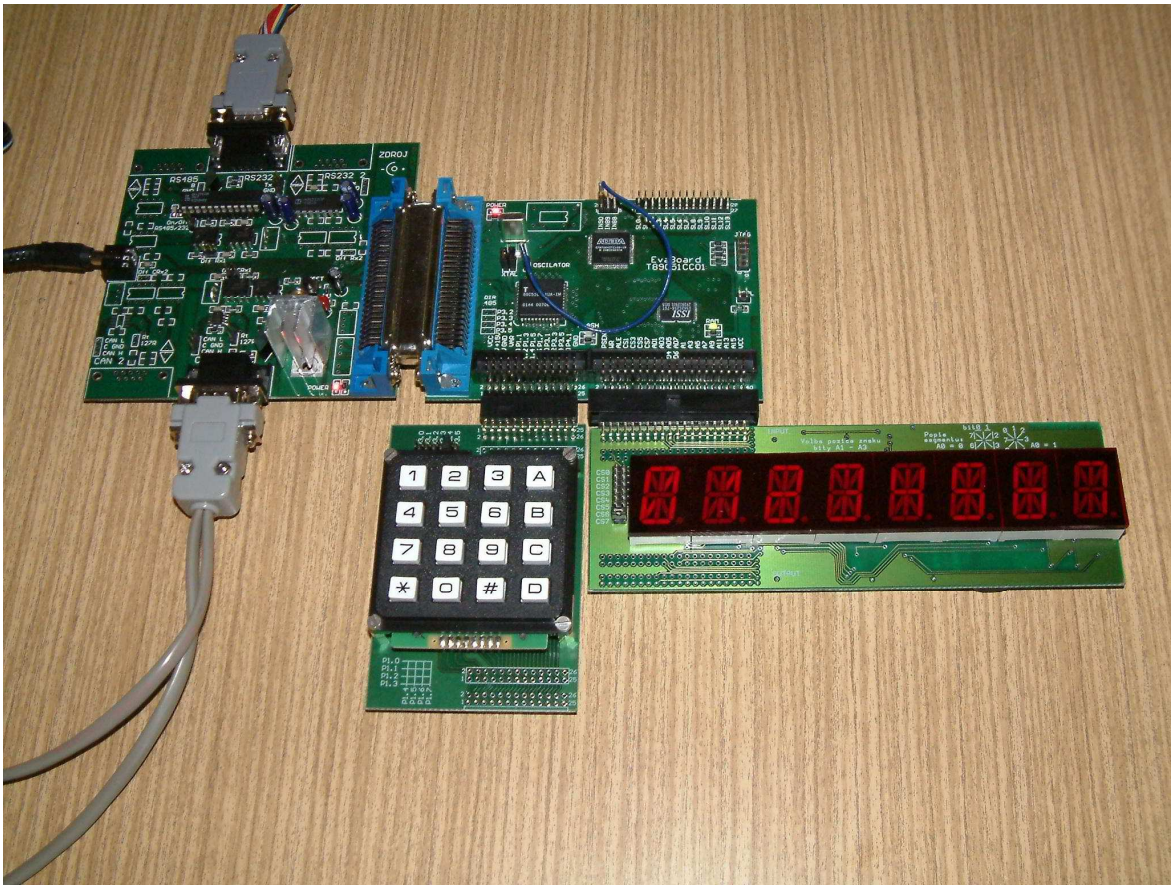

Fig. 2 – power module + processor module + 16-segment LED module + keyboard module

5 Further features

Further improvements and modifications can be done in two possible ways:

- adding peripherals
  - analog part for A/D converter input for interfacing microphones, etc. It will be utilized for acoustic information transmission
  - improved PWM filters
  - D/A converter and amplifier for a loudspeaker
- processor portfolio expansion
  - **Motorola 68HC12 or Star12** – advantages: full power 16-bit architecture + simpler board + evaluation tools available at the Department of Applied Electronics
  - **NIOS** - VHDL processor kernel for PLD circuits with C/C++ GNU compiler

Our conception allows for easy further expansion and will be utilized in special laboratory courses for several forthcoming years.

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