SDR Compliant Multi-Mode Digital-Front-End Design Concepts for Cellular Terminals

GERNOT HUEBER*, LINUS MAURER† GEORG STRASSER‡, KARIM CHABRAK§,
RAINER STUHLBERGER¶, and RICHARD HAGELAUER*
*Institute for Integrated Circuits, Johannes Kepler University, Linz, Austria
†Danube Integrated Circuits Engineering (DICE), Linz, Austria
‡Linz Center of Compentence in Mechatronics (LCM), Linz, Austria
§Institute for Technical Electronics, University of Erlangen, Germany
¶Institute for Communications and Information Engineering (ICIE), Linz, Austria

Abstract: – The software-defined-radio concept received increasing attention due to necessity of multi-mode/multi-system capable terminals for next generation communication systems. This paper summarizes the requirements of a multi-mode compliant digital-front-end (DFE) and describes concepts for cellular terminal implementations on silicon. A partitioning is proposed wherein functionality, normally located in the analog-front-end, is shifted to the digital-front-end. This work concentrates on the receiver part of the digital-front-end.

1 Introduction

Due to the diversity in mobile communications standards, the concept of software-defined-radio (SDR) has grown major importance. Key advantages of SDR include shorter terminal development cycles and greater debugging opportunities. The ability of adopting standards requirements by updating the firmware or reconfiguration of the processing units is a crucial advantage, whereas the cost of silicon area and application dimensions is reduced drastically, strengths up the competitiveness of network providers and semiconductor manufactors as well. Another major issue are the strong requirements to 3G hardware in terms of the compatibility to existing 2G networks.

This paper discusses trade-offs and design considerations of a digital-front-end for for multi-mode communication systems (e.g. EDGE, IS-95, CDMA2000 and UMTS) and presents a concept for an applicable digital-front-end partitioning for cellular terminals.

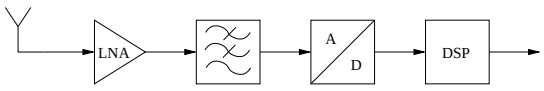

Fig. 1. Ideal software-defi ne-radio receiver

The architecture of the ideal software-defined-radio ([1], [2]) receiver with a minium of analog components is shown in fig. 1. After the signal is received by the antenna, it is amplified in a low-noise-amplifier (LNA). Before analog-to-digital conversion a lowpass anti-aliasing filter is needed. The analog-to-digital converter (ADC) is followed by the digital-front-end, for channelization and decimation. Due to the fact that the channel selection filtering is performed in digital domain (digital-front-end), the analog-front-end and the analog-to-digital converter have to process twice the signal bandwidth of the standard consideration.

A special challenge in digital-front-end concept design are the two interfaces. First, the ADC provides the signal to the digital-front-end at a specified bitwidth and data rate. Second, the baseband interface where the data is transfered from the DFE to the baseband integrated circuit (IC). Again, data rate and bitwidth are design criteria which significantly influence system power and noise sensitivity.

First of all sec. 2 copes with the pivotal issues of a digital-front-end. The requirements of analog-to-digital converters, their respective of ADC in ideal and non-ideal software-defined-radio systems are presented in sec. 3. Finally a concept for a digital-front-end partitioning is presented in sec. 4.

2 Conceptual Design Layout

For maximum flexibility the number of analog components in SDR receivers should be minimized. This implies that channel selection filtering and gain control are performed in the digital domain. The concept of the digital-front-end has to cope with several system realization related constraints which have to be considered (e.g.

area, power) as well as data transfer between digital-front-end on RF IC and baseband IC.
Usually the most important challenge in IC design for mobile terminals is the IC area and power consumption. The interface data rate (DR) has to be minimized because high data rates requires strong buffers (power consumption), inject noise into the analog-front-end (e.g. wire electromagnetic (EM) coupling from data pin to sensitive RF pins like LNA input pins) and support data rates of 2x and 4x chip/symbol rate for each supported mobile communication standard.
Before sample rate can be reduced to 2x or 4x chip/symbol rate channelization filters have to remove spectral power in the adjacent channels. This step reduces the required dynamic range and therefore less bitwidth is required. As a result data rate of BB- and RF-IC interface is minimized.
For the realization of SDR mobile systems a proper partitioning of processing units for RF and BB IC has to be defined.
The functionality of the DFE is divided into three parts. *Decimation* reduces sample rate by an integer factor concerning anti-aliasing filtering. *Channelization* covers the extraction of a single user channel and *fractional sample-rate-conversion* (FSRC) decreases sample rate by a non-integer factor.
This separation of functions allows using optimized filter architecture selection for each of them.

2.1 Reducing Sample Rate

In a first step the sample rate is reduced by a decimation stage where oversampling is lowered using efficient filter architectures at minimum cost in area and power by relaxing the filtering requirements to remove anti-aliasing effects. Filtering of the wanted channel (channelization which is described in sect. 2.2.) is moved to a separate more complex filter structure.
In tab. III a sample decimation partitioning for a 4 bit $\Delta\Sigma$ ADC clocked at 104 MHz is described for 2 times chip/symbol rate at the output. The major part of the sample-rate-conversion is processed in the decimation stage where a large integer decimation is performed. Before a fractional sample-rate-conversion is done at minimum data rate (to reduce power consumption), the channelization stage performs only a decimation of factor two.

2.2 Implementation aspects in terms of bitwidth

Before channelization, regarded as the task of extracting a single user channel by proper filtering (fig. 2), the required dynamic range at the input of the ADC and therefore at the input of the digital-front-end (e.g. $\approx$ 100 dB for EDGE, $\approx$ 100 dB for IS-95, and $\approx$ 70 dB for UMTS) is very high due to the presence of adjacent channels and for this reason a high bitwidth is required. Thus the channelization filters have to attenuate adjacent channel interferers and satisfy the blocking requirements of the standard of operation.

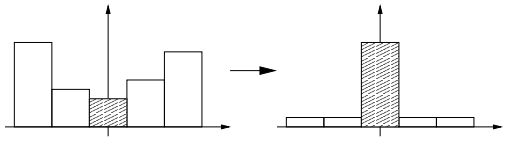

Fig. 2. Channel with adjacent channels before and after channelization

The quantization process introduces distortions of the sampled signal data due to representing the signal value by a limited number of bits. Due to the fact that quantization is a nonlinear operation, additional frequency components are created, which are not necessarily part to the original signal. These components are harmonics and intermodulation products of the original frequency components. If the signal amplitude is sufficiently high the quantization error can be modeled as additive white noise that is uncorrelated with the original signal.
The most general case of signal-to-noise ratio with the bitwidth N is formulated as

$$\mathrm{SNR}{=}20\log\frac{\sigma_x}{V_{pp}} + 10.8 + 6.02\mathrm{N} \qquad (1)$$

Wherein the $\frac{\sigma_x}{V_{pp}}$ is the ratio of the standard deviation σ_x of the signal and the peak-to-peak voltage V_{pp} of the quantizer.
In oversampled systems the total noise power is distributed over a wider bandwidth which benefits the signal-to-noise ratio with $10\log\mathrm{OSR}$

$$\mathrm{SNR}_{\mathrm{OSR}}{=}20\log\frac{\sigma_x}{V_{pp}} + 10.8 + 6.02\mathrm{N} + 10\log\mathrm{OSR} \qquad (2)$$

In $\Delta\Sigma$ ADCs of order L sampling systems SNR calculation has to cope with highpass filtering behaviour

TABLE I
DECIMATION PARTITIONING FOR 2X CHIP/SYMBOL RATE WITH THREE SIGNAL PROCESSING STAGES: DECIMATION, CHANNELIZATION, AND FRACTIONAL SAMPLE-RATE-CONVERSION

Mode	ADC	Decimation		Channelization		FSRC	
	OSR	Dec	OSR	Dec	OSR	Dec	OSR
EDGE	384	64	4	3	2	1	2
IS-95	84.64	21	4.03	2	2.02	1.01	2
UMTS	27.08	6	4.52	2	2.26	1.13	2

of the quantization noise due to noise-transfer-function (NTF). As a result above equation expands for $\Delta\Sigma$ ADCs to

$$\begin{aligned}\mathrm{SNR}_{\mathrm{OSR}}^{L}=&20\log\frac{\sigma_x}{V_{pp}}+10.8+6.02\mathrm{N}\\&+10(2L+1)\log\mathrm{OSR}\\&+10\log\frac{2L+1}{\pi^{2L}}\quad\text{for}\quad\mathrm{OSR}\geq 4\end{aligned}\tag{3}$$

With these equations bitwidth requirements can be estimated for the case before and after channelization, which are summarized in tab. II. Effective bitwidth after ADC is 11.5 bits for UMTS and 14 bits for IS-95 and EDGE. After decimation the number of bits increases due to the term $10(2L+1)\log$ OSR in eq. 3. Channelization reduces bitwidth again, because adjacent channels are removed. The factional sample rate conversion does not influence bitwidth.

TABLE II
BITWIDTH PARTITIONING FOR 2X CHIP/SYMBOL RATE OUTPUT RATE WITH THREE SIGNAL PROCESSING STAGES: DECIMATION, CHANNELIZATION, AND FRACTIONAL SAMPLE-RATE-CONVERSION

Mode	ADC	Decimation	Channelization	FSRC
EDGE	14	17	16	16
IS-95	14	17	12	12
UMTS	11.5	14	9	9

2.3 Baseband IC Interface

Primary concern is the data rate (DR) at the interface between RF and baseband IC, which is a off-chip connection. The interface data rate (DR) has to be minimized, because high data rates requires strong buffers (area and power consumption) and deteriorate analog signal quality due to noise injection into the analog-front-end. Intermediate rates concern filter design and affect therefore power consumption and IC area significantly, as well. Specification of decimation and channelization stages are strongly related and have to be chosen propriately.
The data rate per channel is expressed in terms of the chip rate CR, the bitwidth N and the oversampling ratio OSR

$$\mathrm{DR}=\mathrm{CR}\cdot\mathrm{N}\cdot\mathrm{OSR}\tag{4}$$

For the minimization of the data rate the OSR has to be lowered by decimation (which has been described in sec. 2.1). As well as the bitwith (N) has to be reduced by channelization, which has been discussed in sec. 2.2. The fractional sample-rate-conversion is less important for data rate considerations due to the fact, that the decimation factor is approx. 1.
In tab. III data rates in the interim stages of decimation and channelization and at the output are summarized for EDGE, IS-95, and UMTS.

TABLE III
BASEBAND DATA RATE PARTITIONING FOR 2X CHIP/SYMBOL RATE FOR I AND Q WITH THREE SIGNAL PROCESSING STAGES: DECIMATION, CHANNELIZATION, AND FRACTIONAL SAMPLE-RATE-CONVERSION

Mode	ADC [MB/s]	Decimation [MB/s]	Channelization [MB/s]	FSRC [MB/s]
EDGE	832	110.5	17.333	17.333
IS-95	832	505.143	59.429	58.982
UMTS	832	728	156	138.240

3 ADC Architectures

The ADC has become a key component of mobile communications systems especially in ideal SDR systems where the ADC is placed next to the LNA being the interface from analog to digital domain. Current technologies do not allow the realization of RF signal sampling converters at reasonable power consumption and IC area to meet the requirements of an ideal software-defined-radio system.
For this reason the RF signal is mixed and filtered in the analog domain, providing a zero-IF or low-IF signal to the ADC. Thus the strong requirements on the ADC in sample rate and bandwidth can be relaxed by magnitudes. Nevertheless constraints in power consumption, SNR, bandwidth and area are a major challenges in design, where the architecture has to be chosen carefully. There are two main ADC architectures which allow sufficient sample rate at reasonable bitwidth. Both architectures are discussed in the following.

3.1 Pipelined ADCs

The pipelined analog-to-digital converter (ADC) has become the most general used ADC architecture for sampling rates from a few megasamples per second up to 100+ MS/s with bit resolutions of 16 bits at lower and 8 bits at higher samples rates.
The architecture is based on a cascade (pipeline) of fast low-bitwidth flash ADCs and DAC stages (fig. 3). The results of the flash ADCs are fed into an alignment and digital error correction block where the results are combined and the output values are generated.

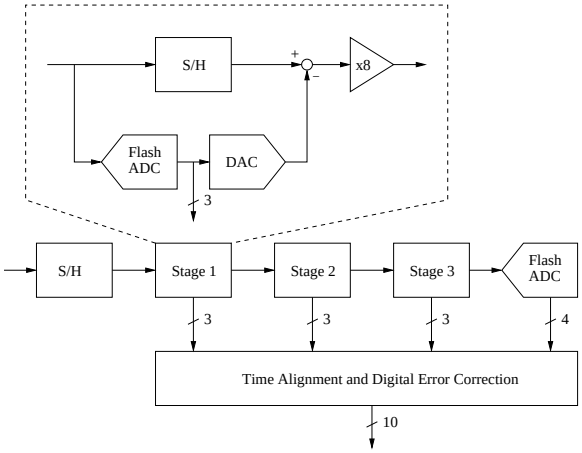

Fig. 3. Architecture of a pipelined ADC with three 3-bit stages

ADCs based on pipelined architecture capable of multi-mode applications requirements have been designed recently ([3]). Although the architecture topology provides maximum usable bandwidth for the signals, the area requirements of this ADC is about 25 mm^2 and the power consumption is 1 W. Therefore this ADC architecture is not suitable for the strong power contraints of mobile terminals.

3.2 $\Delta\Sigma$ ADCs

Employing noise-shaping technique increases resolution gain in the channel of interest if oversampling is used. Fig.4 shows a second order $\Delta\Sigma$ ADC.

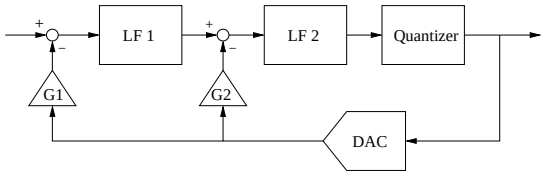

Fig. 4. Architecture of a second order $\Delta\Sigma$ ADC where the loopfi lter is split into LF_1 and LF_2 and the weights of the feedback are G_1 and G_2.

Two types of $\Delta\Sigma$ ADCs are known, which are distinguished on their type of loopfilter. First type is based on a *discrete time* loopfilter, which allows ADCs that are most favourable for maximum sample rate applications. Second type is built using a *continuous time* loopfilter. This design is known to be more power efficient than *discrete time* $\Delta\Sigma$ and *pipelined* ADCs ([4]), which is a very desireable advantage in mobile battery driven applications. There is an area of $0.55mm^2$ and a power consumption of $4.5mW$ reported in [5]. Additionally the characteristic of the signal transfer function (STF) provides inherently anti-aliasing filter behaviour relaxing the requirements of the analog anti-aliasing filter significantly.

Major trade-off is the high sensitivity to clock jitter, which limits the maximum achievable signal-to-noise ratio (SNR).

In multi mode appliciations the analog-to-digital converter (ADC) has to adapt to the required channel bandwidth in each mode and provide sufficient dynamic range according to the standard specifications.

The crucial design criteria for low power consumption are loop-filter order, OSR and quantizer levels.

4 DFE Architectures

The receiver architecture considered is built as shown in fig. 5. First an analog front-end (Filter, LNA, and Demodulator) converts the signal from the antenna down to zero-IF frequency. The IF signals are fed into an I and

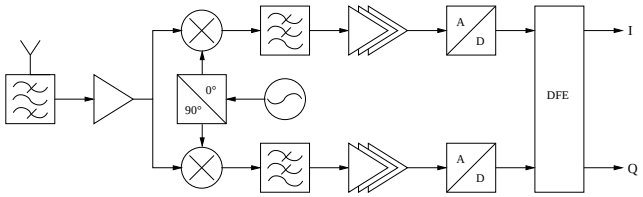

Fig. 5. Proposed SDR Receiver Architecture

Q $\Delta\Sigma$ ADC, respectively. In a cascaded-integrator-comb filter (CIC) the signal is decimated due to the simplicity of the filter at minimum area and power consumption cost. The channelization is performed in wave-digital filters (WDF), at reasonable cost in area and power due to the reduction in data rate. Before the frequency offsets are corrected in a CORDIC, common mode offsets are eliminated by a notch filter. Pulse filtering is done in a polyphase FIR filter and finally the data rate is reduced in a fractional sample-rate-converter to obtain an exact 2x or 4x chip/symbol rate output signal.

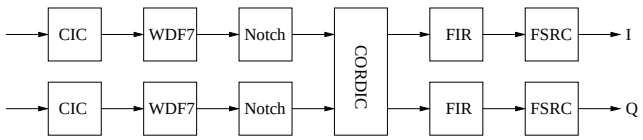

Fig. 6. Proposed SDR Receiver DFE Architecture

For the digital front end depicted in fig. 6 an estimation of number of gates has been done. The synthesis estimation has given a number of 50k gates for the receive digital-front-end, which gives an area of approximately 0.6 mm^2.

5 Conclusion

This paper presents an implementable derivation of the ideal software-defined-radio cellular terminal, which reflects todays technologies limits especially limits of sample rate and bandwidth for ADC, digital-front-end, power consumption and IC area.
Current ADC technology provides sufficient dynamic range and bandwidth for shifting functionality from the analog-front-end to the digital domain. This transfer relaxes requirements on the analog filters which can be downsized significantly. Additionally this concept benefits flexibility and is perfectly suitable for multi-mode communication systems.

Acknowledgment

The authors would like to thank Zdravko Boos of Infineon Technologies for his support and fruitful discussions.

References:

[1] Tim Hentschel, Matthias Henker, and Gerhard Fettweis, *The Digital Front-End of Software Radio Terminals*. IEEE Personal Communications, August, 1999

[2] Paul Burns, *Software Defined Radio for 3G*, Artech House Publishers, Boston - London, 2002

[3] Alfi o Zanchi, Frank Tsay, and Ioannis Papantonopoulos, *Impact of Capacitor Dielectric Relaxation on a 14-bit 70-MS/s Pipeline ADC in 3-V BiCMOS*, IEEE Journal of Solid-State Circuits, December, 2003

[4] L. Doerrer, *A 10bit Continuous-Time Sigma-Delta ADC with Quantizer Dynamic Element Matchin for UMTS in a 0.12 μm CMOS process*, Austrochip 2003, Linz, Austria, 2003.

[5] R. H. M. van Veldhoven, *A Triple-Mode Continuous-Time $\Sigma\Delta$ Modulator Width Switched-Capacitor Feedback DAC for GSM-EDGE/CDMA2000/UMTS Receiver*, IEEE Journal of Solid-State Circuits, December, 2003

[6] T. Hentschel, *Sample Rate Conversion in Software Configurable Radios*, Artech House Publishers, Boston - London, 2002