A New Recursive Active Filter in MMIC

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Abstract: The principle of recursive filters is well known in digital filtering. This paper deals with active recursive filters. A new design approach is presented. It will be shown that how active elements can be used in the design of amplification elements and large microwave time delay. The analytical and computer-simulated results will be presented for an active bandpass filter in the C-band.

Key-Words: recursive filter, active filtering, time delay, monolithic microwave integrated circuit (MMIC).

1 Introduction

With the increase of mobile communications, filters must be miniaturized in order to be integrated into MMIC modules along with other microwave functions such as amplifiers, mixers or oscillators. While conventional passive filters need plenty of space as well as presenting high losses, active filters appear as a promising solution. Recent realizations of recursive filters have shown that a given signal flow graph may be translated into any number of physical design [1]. This research deals with recursive filters. It focuses on a new recursive filter design based on the use of active elements in time delay and amplification sections design.

2 Simplified recursive filter

The general signal flow graph of a simplified recursive filter is shown in figure 1.
The transfer function is given by:

$$H(j\omega) = \frac{a_0}{1 + b_1 e^{-2j\pi f\tau}} \quad (1)$$

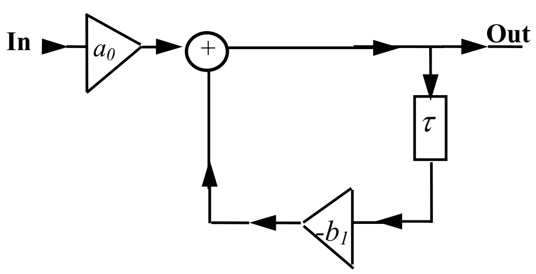

Fig.1: Flow graph of a simplified recursive filter

The novel approach, qualified cellular, consists of synthesizing a transfer function in association with poles and zeros which could be characterized individually. It means that instead of studying a complex recursive structure with transfer functions in the form of product of elementary functions, we can study simplified recursive structures.
The synthesis of the filter consists of determination of coefficients a_0 and b_1 and time delay τ. We choose a second-order bandpass filter (f_0 = 4GHz, Q = 50) as a goal function; a_0, b_1 and τ are determined by minimizing the average quadratic difference around the center frequency (figure 2).

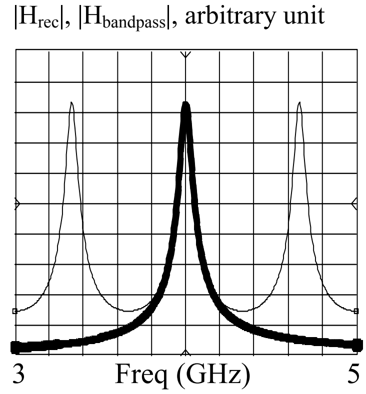

Fig.2 : Bandpass second order filter(Q=50) ▬▬ and simplified recursive filter —— transfer function

3 Electrical topology

The modified flow graph for the electrical circuit topology is given in figure 3. The filter works in the microwave range, and is characterized by its S-parameters. Furthermore, in the vicinity of the center frequency, the filter should be matched both at input and output ($S_{11} = S_{22} = 0$).
The result is valid if the following requirements are fulfilled. Phase shifters are pure time delays at f_0 =

4GHz, and matched at input and output to 50Ω. The gain stages are unilateral.

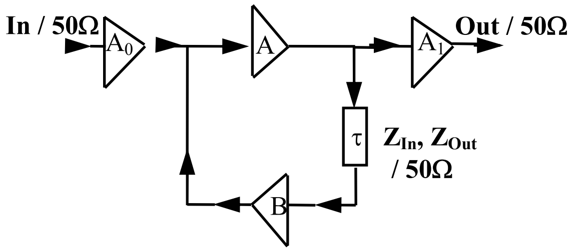

Fig.3 : Electrical topology of a simplified recursive filter

To design the transfer function of simplified recursive filter, we propose the topology of figure 4.

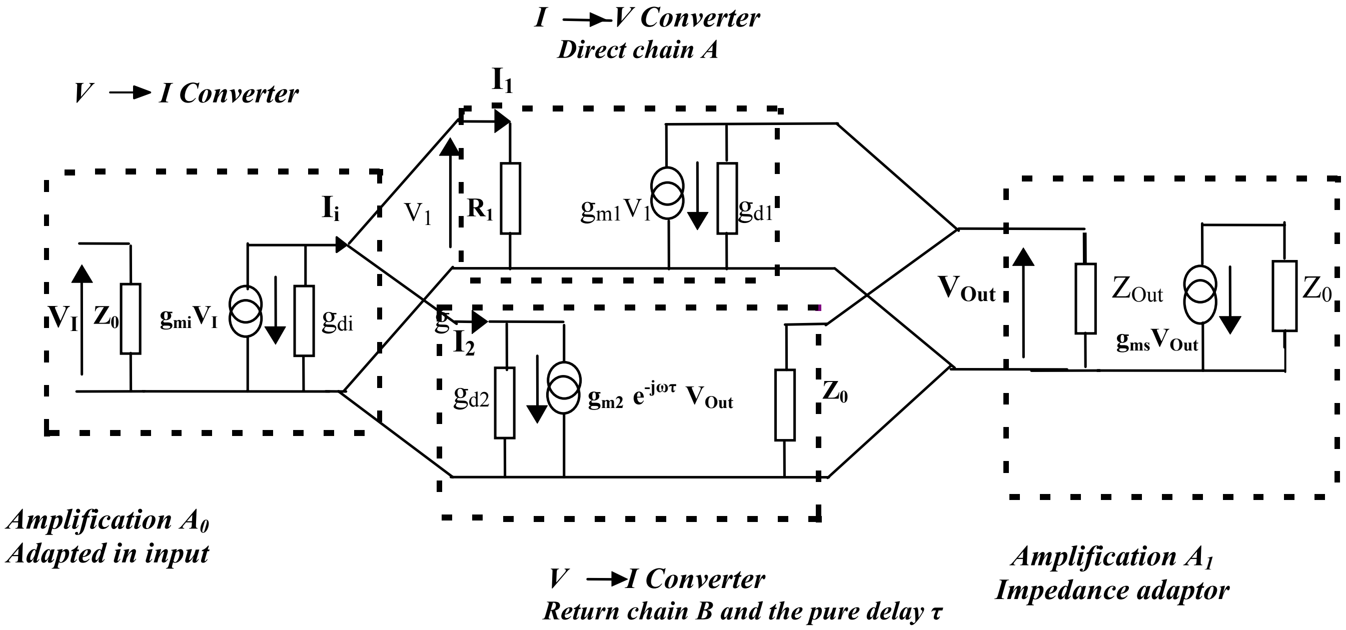

Fig. 4 : Electrical topology equivalent for a simplified recursive filter

This is a parallel voltage type of retroaction. The gain voltage of this structure is:

$$\frac{V_{Out}}{V_I} = g_{mi}\alpha \frac{1}{1+\alpha\beta e^{-j\omega\tau}} \qquad (3)$$

if $\frac{1}{g_{di}} \gg R_1$ and $\frac{1}{g_{di}} \gg \frac{1}{g_{d2}}$.

Where:

$$\alpha = g_{m1}\frac{R_1}{1+R_1 g_{d2}}\frac{1}{1+Z_0 g_{d1}}Z_0 \approx g_{m1}R_1 Z_0$$

$$\text{if } R_1 g_{d2} \text{ and } Z_0 g_{d1} \ll 1 \qquad (4)$$

$$\beta = -g_{m2}$$

4 Phase shifter (pure time delay τ)

The phase shifter is designed with bridge-tee all-pass cells [2]. Each all-pass cell generates an 180^0 phase shift around the center frequency f_0. By cascading two identical cells, we obtain a 360^0 phase shift and a large time delay. Insertion losses are 0dB if loss less inductors are used in the circuit.

By using actual inductors models (foundry models), we notice an important gain drop, without any change in the phase shift. According to these results, it is necessary to add an active compensation for the inductor losses. Loss compensation is based on two-cascaded all-pass cell transfer function analysis.

It has been shown [3,4] that the compensation two-port must exhibit the following features:

- Input impedance Z_{in} = 50Ω
- Phase shift multiple of 2π
- Unilaterality
- High output impedance
- Sufficient gain for loss compensation.

These conditions are achieved by cascading two common source transistors (figure 5).

Both cascaded common source transistors are inserted between the time delay cells. For the design, we choose the HEMT PML D02AH technology. The transistors used for this application have 0.2µm gate length and a two-finger 30µm wide gate. They are biased through active loads. This phase shifter is input-output matched to 50Ω (figure 6), and works as a pure time delay over 800MHz frequency band (figure 7).

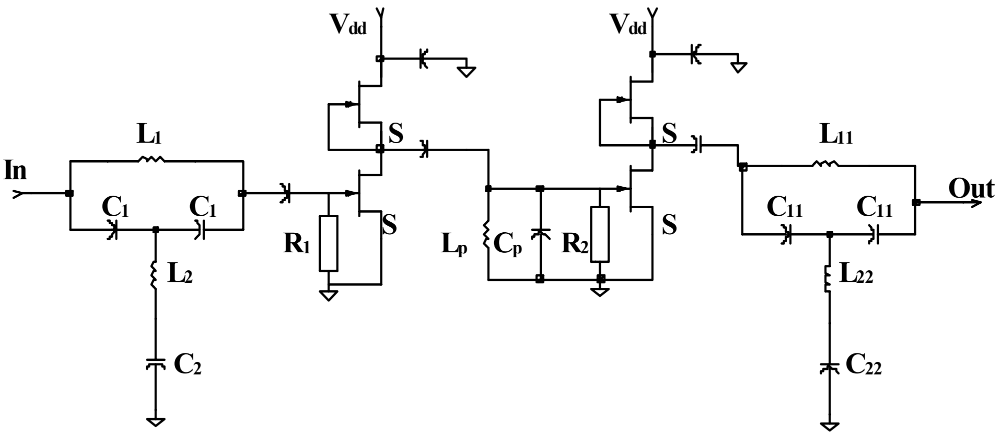

Fig.5: Schematic diagram of active delay

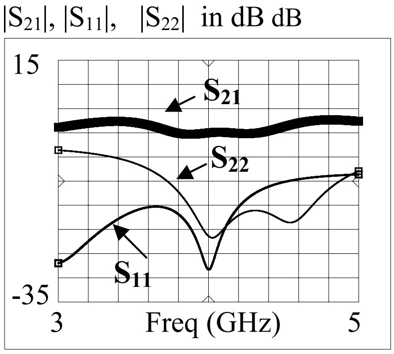

Fig.6: S_{ij} post layout simulation of active delay

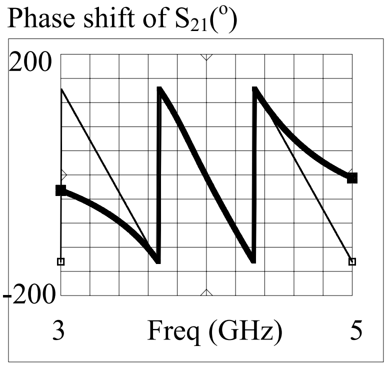

Fig.7: comparison between theoretical time delay —— and post layout simulation time delay ▬▬

5 Gain stages

The cell (A_0) must have input impedance equal to 50Ω and high output impedance. The input impedance condition is fulfilled with a gate common transistor. The common source transistor permits us to obtain high output impedance and the desired gain. The biasing of common source transistor is achieved by cascode active charge (figure 8).

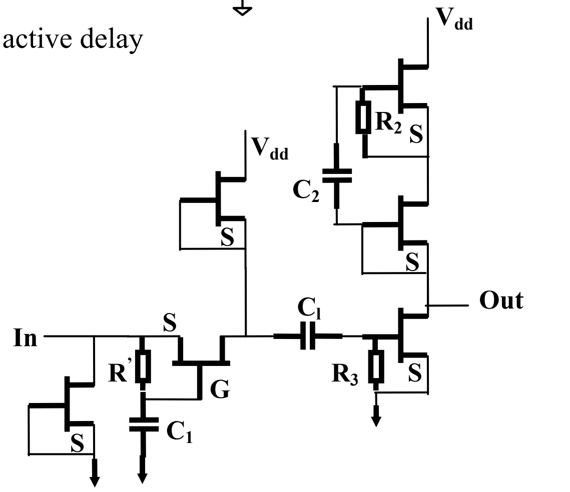

Fig.8: Schematic diagram of the amplification A_0

Current-voltage converter (cell A) must have very small input impedance compared to output impedance of cell A_0 and output impedance of the return chain B. The output impedance of cell A must be very high compared to the characteristic impedance Z_0(50Ω) of the delay cell. Cell A is designed with a cascode circuit and biasing with cascode active charge in order to obtain the high gain and high output impedance (figure 9).

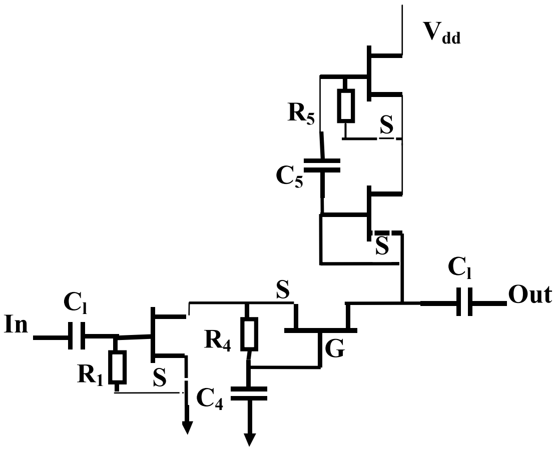

Fig.9: Schematic diagram of the amplification A

Voltage-current converter of the return chain (B) must have input impedance equal to characteristic impedance Z_0 of the time delay cell and must have the output impedance very small compared to output impedance of stage A_0. These conditions are obtained with a common source circuit (figure 10).

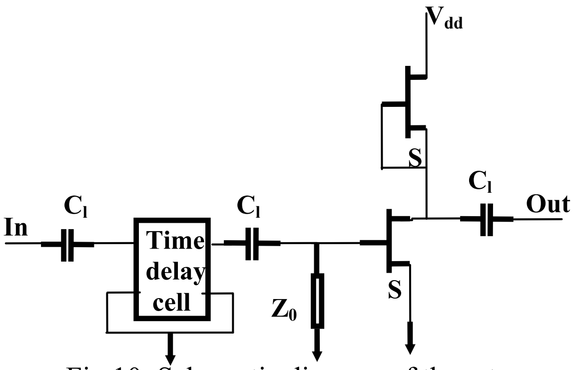

Fig.10: Schematic diagram of the return amplification B and the time delay cell

Cell (A_1) must have input impedance very high in order not to charge the output and have output impedance equal to 50Ω. These two conditions are fulfilled with a drain common transistor (figure 11).

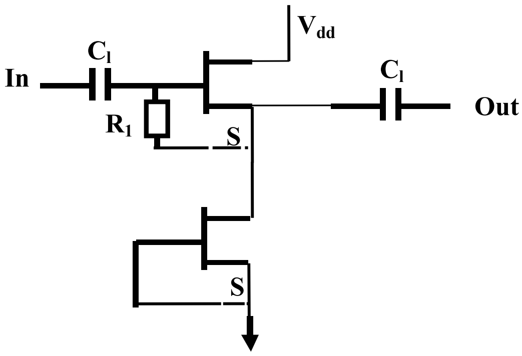

Fig.11: Schematic diagram of the cell A_1

6 MMIC design

The active filter may be compared to an ideal active filter on an 800MHz bandwidth around a center frequency f_0 = 4GHz (figure12).

The input-output matching is good (< -25dB) in the frequency band (figure 13).

We have studied the influence of technological parameter dispersion. The circuit is not sensitive to parameter dispersion. The stability of the filter has been studied by Rollett coefficient (K) for external stability and by normalized determinant function (NDF) for internal stability.

We have designed the layout (figure14). The chip size is 1×2 mm^2. The circuit power consumption is 150 mW.

7 Conclusion

A new approach for recursive filters has been presented and illustrated with active element implementation in C-band using MMIC technology. Whereas wideband applications are concerned with this kind of filter. We have demonstrated here that relatively narrowband applications can also use this structure.

The same approach for simplified recursive filters in cascade could be used to obtain a more selective response with narrower bandwidths.

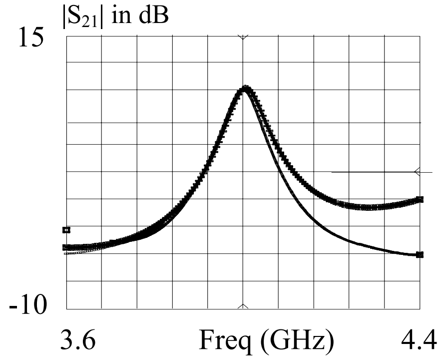

Fig.12: S_{21} comparison between theoretical —— and post layout ▬▬ simulation of a simplified recursive filter

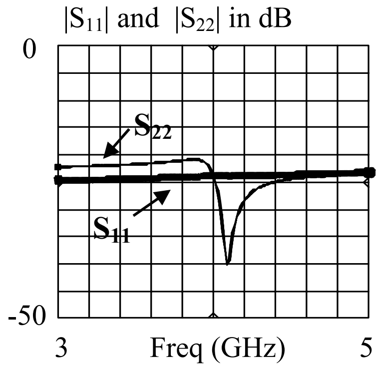

Fig.13: Input and output post layout simulation of simplified recursive filter

References

[1] C. Rauscher, "Microwave Active Filters Based on Transversal and Recursive Principles," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-33, Dec. 1985, pp. 1350-1360.

[2] D. Adler and R. Popovich, "Broadband Switched-Bit Phase Shifter Using All-Pass Network," *IEE MTT-S Dig.,* 1991, pp. 265-268.

[3] M. Dousti and J.L. Gautier, "Active MMIC Wide Band Time Delay," *Microwave and Optical Technol. Lett.*, Vol. 16, No. 6, Dec. 1997, pp. 382-385.

[4] M. Dousti and J.L. Gautier, "New Design approach For Active Filter Using MMIC Technology," *Microwave and Optical Technol. Lett.*, Vol. 19, No. 1, Sep. 1998, pp. 66-69.

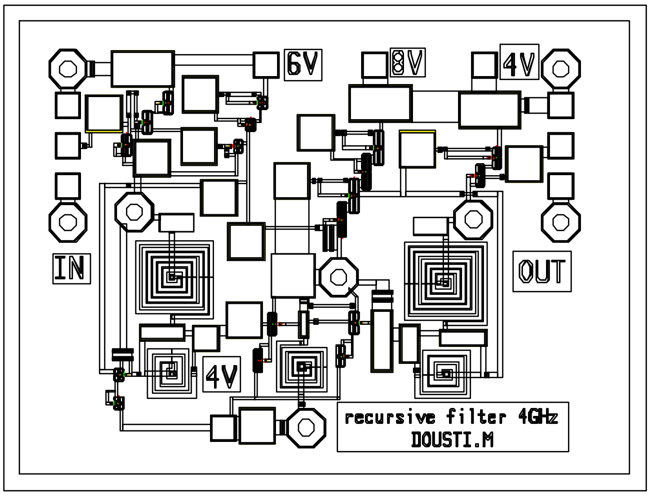

Fig.14: layout of simplified recursive filter