Towards a Paradigm for Adaptation in Pulse-Coupled Neural Networks

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Abstract: - We demonstrate that pulse-coupled neural networks can be regarded in terms of classical logic operations. This opens the possibility that algorithms used for adapting logic circuits might be employed for adaptation in pulse-coupled neural networks.

Key-Words: - neural networks, pulse-coupled, VLSI, classification

1 Introduction

Pulse-coupled neural networks (PCCN) have numerous applications in image processing [1], and in clustering and classification [2]. Treatments of PCNN have focused on their synchronous firing character and how this can be exploited in image processing. Little has been reported on adaptation algorithms for PCNN. Possibly the primary difficulty here lies with their recurrent network structure combined with their pulse-mode, bursting behavior that would seem to make existing adaptation algorithms inapplicable to PCNN. Yet, the growing number of small, easily implemented pulse-mode neurons [3]-[5] makes the adaptation problem for PCNN rather an urgent one. The question is: Where does one begin?

From their earliest conception, neural networks have had a special relation to logic circuits. The McCulloch-Pitts model in the hands of von Neuman produced the computer. Classification and other image processing tasks are describable in logic terms in a well-known manner [6], e.g. the cluster classification problem illustrated in Figure 1. Recently methods have been reported for making logic circuits adaptive. Martinez introduced the method of Adaptive Self-Organizing Concurrent Systems for adaptation of logic circuits based on a dynamic programmable logic scheme [7]. Wells and Brennan developed a Quine-McCluskey-like algorithm for adaptation based on a content-addressable parallel processor [8]. If an analogy is drawn between PCNN and logic functions, then approaches such as these may contain a framework for PCNN.

2 PCNN Logic Circuits

We show by demonstration that such a logic analogy can be drawn between PCNN and logic functions. We employ a previously reported pulse-mode neuron [4] with multiple synaptic inputs for charging and/or discharging a capacitive storage node. Each synaptic input can be programmed independently as excitatory or inhibitory through binary synaptic weights. The storage node is applied to Schmitt triggers to control a pulse generator circuit. The programmable weights give the neuron the capability of being made adaptive.

Consider the three-way classification problem illustrated in Figure 1. This problem is solved by dividing the input space into subregions according to the given line equations. For this simple problem the solution is easily obtainable by hand according to standard methods [6]. The logic function is given by Table 1 and a PCNN implementing this function is shown in Figure 2. Integer inputs X and Y are represented using two bits (X1, X0) and (Y1, Y0). The input layer contains a neuron for each boundary line used to partition the input space. The output layer contains one neuron for each classification.

The logic equations are given in Figure 1, where Nx denotes a specific subregion and the corresponding neuron from the input layer; an overbar denotes logical negation. It is easy to correlate these equations

with the excitatory and inhibitory inputs in Figure 2. Two implementation details are worth note. To perform the logical inversion of the output of neuron 3 at neuron 10, an excitatory input ("High") is provided to N10. This input provides a constant weak excitation to N10 which, when combined with a weak inhibitory input from N3, realizes the complement of the boundary line in Figure 1. If N7 and N3 are not active (firing), the "High" input causes N10 to begin firing. If N7 is inactive but N3 is firing, the inhibition it supplies prevents N10 from firing. Finally, the excitatory connection from N7 to N10 is weighted such that if N3 and N7 are both firing then N7 dominates the inhibition from N3 and N10 begins firing.

The second detail is the ease with which standard logic connectives are implemented by the neurons. An AND function is the summation of excitatory inputs with small weight values. An OR uses large weight values such that any input excites firing. The function A AND not-B uses a large inhibitory weight that dominates if B is firing and a medium excitatory weight such that A in the absence of B can produce firing. Other logic connectives are easy to obtain with proper choice of weights.

Simulation results for each of the input combinations from Table 1 are illustrated in Figure 3. The circuits were simulated using Pspice for a 1.2 micron process. Burst firing by a neuron is analogous to a logic "1" output. In every case, the response of the network correctly matches the logic in Table 1.

4 Conclusion

This simple illustration demonstrates that an analogy can be made between PCNN functions and logic equations. This opens the door for the application of the mathematical theory of switching circuits to PCNN. It also suggests strongly that methods developed by researches into adaptive logic circuits might equally well apply to adaptation algorithms for PCNN. Of course, the issues involved with adaptation in recurrent networks remain formidable. We believe that the "logic paradigm" presents a new way of looking at adaptation in neural networks.

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Table 1 Truth table showing the input stimulus and desired neuron outputs for the network in Fig. 2.

Input Patterns				Input Layer				Hidden Layer			Output Layer		
X1	X0	Y1	Y0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0	1	0	0	0	1	0
0	0	1	0	0	1	1	0	0	0	0	1	0	0
0	0	1	1	1	1	1	0	0	1	0	0	1	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	1	0	1	0	0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0	0	0	0	1	0	0
0	1	1	1	1	1	1	0	0	1	0	0	1	0
1	0	0	0	0	0	1	0	1	0	0	0	1	0
1	0	0	1	0	0	1	0	1	0	0	0	1	0
1	0	1	0	0	1	1	0	0	0	0	1	0	0
1	0	1	1	1	1	1	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	1	0	0	0	1	0
1	1	0	1	0	0	1	1	1	0	0	0	1	0
1	1	1	0	0	1	1	1	0	0	0	1	0	0
1	1	1	1	1	1	1	1	0	0	1	0	0	1

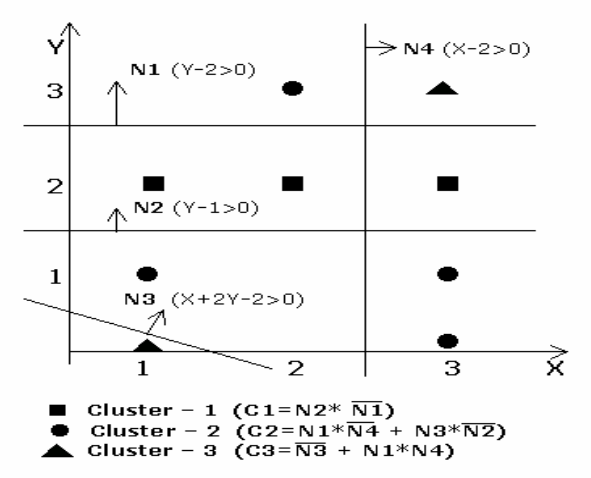

Figure 1 Distribution of patterns and the formation of subregions through Boolean combination of linear classifiers.

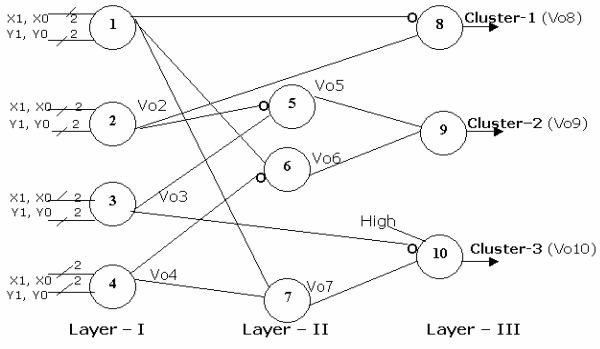

Figure 2 Each neuron in the input layer represents one linear classifier. Neurons in the hidden and output layer form Boolean combinations to produce the final cluster outputs.

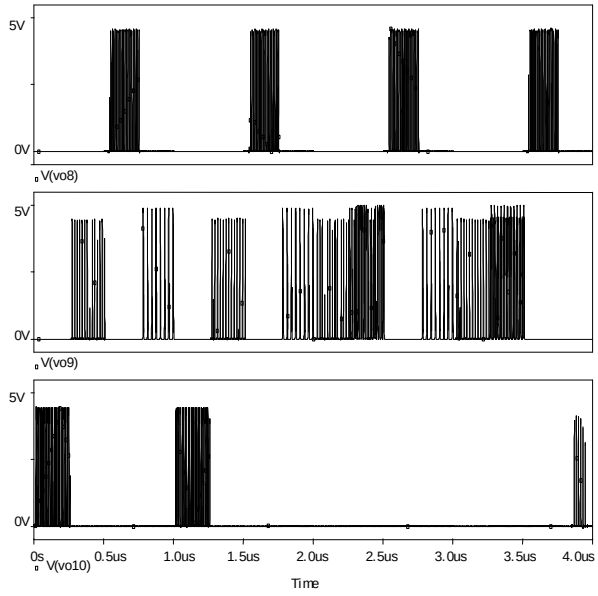

Figure 3 Simulation results for a 1.2 micron CMOS process. Each input pattern from Table 1 was applied for 250 ns. Waveforms correspond to the output layer of Fig. 2 and indicate cluster membership.