Application of a CMOS Neuron for PCNN: Hopfield Auto-Associative Memory

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Abstract: - Application for a biologically inspired pulse-coded CMOS neuron, Hopfield auto-associative memory is presented. Given corrupted versions of the stored images, the trained network will able to recall the corresponding stored image near in Hamming distance (HD).

Key-Words: artificial neural networks, pulse-coded, VLSI, Hopfield memory, associative memory

1 Introduction

The work presented in this paper focuses on the application of a pulse-coded CMOS neuron developed by Liu and Frenzel [1]. The functionality of a biological neuron can be found in electrically stimulated pulse coded neurons. Circuits based on pulse stream encoding techniques with current as an external stimulus can be realized as pulse coded neural networks (PCNN). In PCNN, circuits weighting and summing of stimulating inputs are done to control the firing rate of a pulse generating circuitry [2]. Faster PCNN can be built for circuits with dedicated functionality for which the connectivity requirements are less [3].

The basic structure of the CMOS neuron is shown in Fig. 1. The neuron has multiple synaptic inputs, which are connected to a capacitive storage node. This storage node is connected to a threshold circuits block, which is followed by a ring oscillator to provide the final output of the neuron. Each synaptic input can be programmed as excitatory and/or inhibitory based upon the values of stored binary weights, WE2–0 and WI2–0. The storage node voltage is converted to a digital control word by multiple threshold circuits for control of the pulse generator circuit. The pulsed nature of the neuron output enables the construction of pulse-coded neural networks (PCNN). The use of programmable weights allows for the implementation of learning, adaptation, and reconfiguration. Garcia-Lamont et al. [4] demonstrated clustering and classification of data by neurofuzzy techniques using CMOS current-mode circuits with fixed weights. These simple analog current-mode circuits can approximate complex arithmetic processes that appear in neurofuzzy systems.

2 Problem Description

Hopfield associative memory is an auto-associative memory [5] used to “store and recall” a set of bit-map images. Hopfield introduced an associative memory model with emergent collective properties like familiarity recognition, categorization, error correction, time sequence retention and generalization [6]. Implemented algorithms using Hopfield networks have found wide applications in associative memory, A/D conversion and optimization problems [7]. Properties of HD are demonstrated in [7]. Given any N-bit input, the network output settles on an N-bit stored pattern, which has the least HD from the input.

3 Problem Solution

A 4-Hopfield network as shown in Fig. 2 is constructed and the patterns (1,0,1,0) (0,1,0,1) (0,1,1,0) & (1,0,0,1) are stored. The input patterns are mapped to the stored patterns with respect to the HD, resulting in correct theoretical outputs for these patterns. These input-output mappings are shown in Table. 1.

The weight matrix is calculated for the 4-bit Hopfield network and the resulting weights are imposed on the network connections. This weighted network is trained to produce a final weight matrix for the best convergence of the output. Increasing or decreasing the weights by checking the charge on the storage node to meet the threshold and by checking the output to be correct for all the input combinations performs the training. This process is

repeated until good convergence on the output is observed. Changing the thresholds of neurons in the network by changing the Schmitt triggers inside the neurons can also be useful for training. It is beneficial in cases where the output of the neuron is used as an input to other neuron and vice-versa.

Calculating synaptic weights for N-bit Hopfield network: For storing 'n' patterns, the weight matrix for the Hopfield network, W can be computed as follows [8].

$$W = \sum_{p=1}^{n} S_p S_p^T \qquad (W_{ij} = 0 \text{ for } i = j) \tag{1}$$

where, S_p is the pattern to be stored and S_p^T the transpose.

The weight matrix is symmetrical and its dimension depends on the number of bits of the input pattern. The size of weight matrix for a N-bit Hopfield network is N*N. The increase in the size of the network with respect to the increase in number of bits of the input patterns is quadratic.

4 Conclusion

Simulations were performed using Microsim Pspice with models for a 1.2 micron CMOS process. Each input combination was applied for a period of 125 Ns in binary order. The simulation results are shown in Fig. 3 and are in agreement with Table 1.

This successful application implies the validity of testing of the neuron developed by Liu and Frenzel [1].

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Table 1 Input stimulus and desired outputs.

Input	Hamming distance from the Stored patterns (1 0 1 0)	(0 1 0 1)	(0 0 1 0)	(1 1 0 1)	Output
(0 0 0 0)	2	2	**1**	3	(0 0 1 0)
(0 0 0 1)	3	**1**	2	2	(0 1 0 1)
(0 0 1 0)	1	2	**0**	4	(0 0 1 0)
(0 0 1 1)	2	2	**1**	3	(0 0 1 0)
(0 1 0 0)	3	**1**	2	2	(0 1 0 1)
(0 1 0 1)	4	**0**	3	1	(0 1 0 1)
(0 1 1 0)	2	2	**1**	3	(0 0 1 0)
(0 1 1 1)	3	**1**	2	2	(0 1 0 1)
(1 0 0 0)	**1**	2	2	2	(1 0 1 0)
(1 0 0 1)	2	2	3	**1**	(1 1 0 1)
(1 0 1 0)	**0**	4	1	3	(1 0 1 0)
(1 0 1 1)	**1**	3	2	2	(1 0 1 0)
(1 1 0 0)	2	2	3	**1**	(1 1 0 1)
(1 1 0 1)	3	1	**4**	**0**	(1 1 0 1)
(1 1 1 0)	**1**	3	2	2	(1 0 1 0)
(1 1 1 1)	2	2	3	**1**	(1 1 0 1)

Figure 1 Block diagram of a single neuron with multiple synaptic inputs, each independently programmable as excitatory or inhibitory.

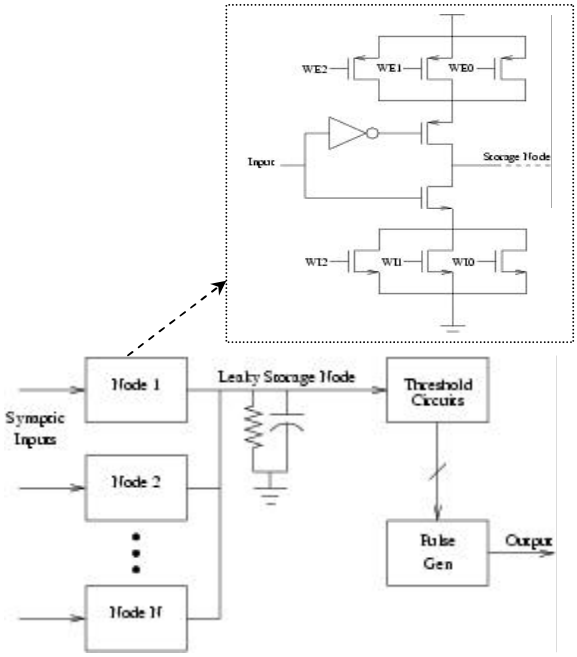

Figure 2 Network topology for 4-Hopfield associative memory.

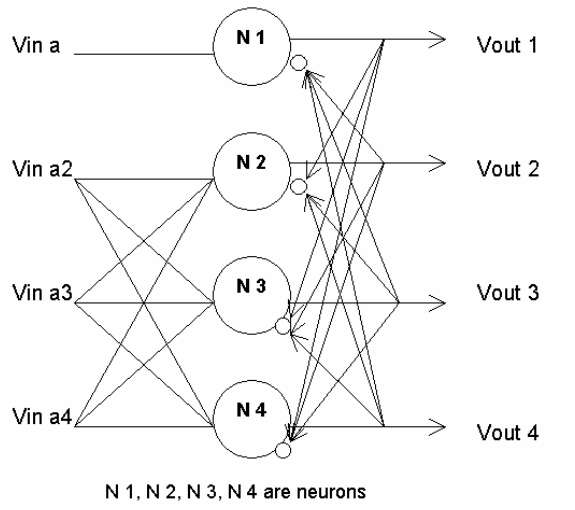

Figure 3 Waveforms correspond to the four neurons in Fig. 2 and indicate autoassociative recall of patterns shown in Table 1.