Large-Signal Model Generation of the Dual-Gate Microwave MESFET from Multi-Bias S-parameter Measurements

M. ABDEEN and M.C.E. YAGOUB
School of Information Technology and Engineering
University of Ottawa
800 King Edward Ave, Ottawa, Ontario, K1N 6N5
CANADA

Abstract: - In this paper we present a technique for automatically generating the large-signal lumped element model for the dual-gate MESFET. Values of the large-signal model are extracted from two-port S-parameter measurements at many DC-bias points. The automatic model generation is accomplished by integrating multiple software tools. The technique is tested on a 6-gate 1x100 μm dual-gate MESFET manufactured by Nortel Networks. The large-signal model is then verified through a variable gain large-signal amplifier application based on the dual-gate MESFET. The model is first imported to a commercial simulator. Harmonic balance simulations and experimental measurements of the verification circuit showed very good agreement of the first harmonic. For the second and third harmonic, some discrepancies between the measurements and the model are observed. This is mainly due to some model simplifications and second order effects.

Key-Words: - Semiconductor Device Modeling, Dual-Gate FET, Design Automation, Neural Network Applications, Microwave MESFET, Microwave Measurements.

1 Introduction

The increasing need for advanced communication technologies in the 21st century is leading to continuous development of new and more complex active devices and systems. Transistors such as HBTs, FETs, and HEMTs are fundamental components in today's personal, corporate and global communication systems.

The single- and dual-gate MEtal-Semiconductor Field Effect Transistors (MESFET) are popular devices with wide areas of RF/Microwave applications. They have been used in high frequency, high-gain, and low-noise applications such as amplifiers, oscillators, mixers, etc.

The dual-gate MESFET is a variation of the single gate with a second gate between the first gate and the drain. Its advantages over the single gate of comparable size include higher gain, better input gate-to-drain isolation, and higher output impedance. That made it attractive for various nonlinear applications such as mixers, frequency multipliers, and power combiners and splitters. Despite the existence of some modeling work for the dual-gate MESFET, there is a need to develop more efficient, accurate, and faster nonlinear modeling methodologies.

There exist fewer attempts to model the large signal behavior of the dual gate FET [1]-[3] than for the single-gate FET. The main focus of previous works was to model the nonlinearity of the drain current. Other significant elements such as the gate-to-source and gate-to-drain capacitances are not accounted for. Accurate dual-gate FET models, however, require the inclusion of nonlinear elements of significance besides the drain current. This work presents a framework to automatically obtain the large-signal dual-gate MESFET model including the nonlinear elements such as junction and overlapping capacitances as well as the trans- and output conductances.

Artificial Neural Networks (ANNs) have emerged as a powerful technique for modeling input/output relationships. They have been used for many complex applications such as control, telecommunications, biomedical, and pattern recognition. In recent years, however, ANNs are being used more and more in the area of RF/microwave design and applications. Many examples include the modeling of transmission-line components [4][5], coplanar waveguide (CPW) components [6], FETs [7], and amplifiers [8]. Recently, the work on straight applications of standard neural network techniques to microwave problems has now led to advanced work in RF and microwave-oriented neural network structures, training algorithms, knowledge-based networks, and methodologies for libraries of microwave neural models developments.

Neural networks are used as the modeling paradigm of this work. Training data for the large-signal dual-gate neural model is obtained by performing three-port S-parameter measurements for the device over a wide range of DC bias points. The three-port S-parameter measurements are then used to calculate the two-port S-parameters for the two single gate FETs (Fig. 1). A parameter extraction procedure is applied on the resulting sets of two-port S-parameters to obtain the device nonlinear component values. This procedure is repeated over a wide range of DC bias values as explained below. The numerical data of the model parameter values are then fitted to neural network functions. These functions are used to obtain other parameter values such as drain current from the transconductance. This step is important in implementing the nonlinear model in a commercial circuit simulator.

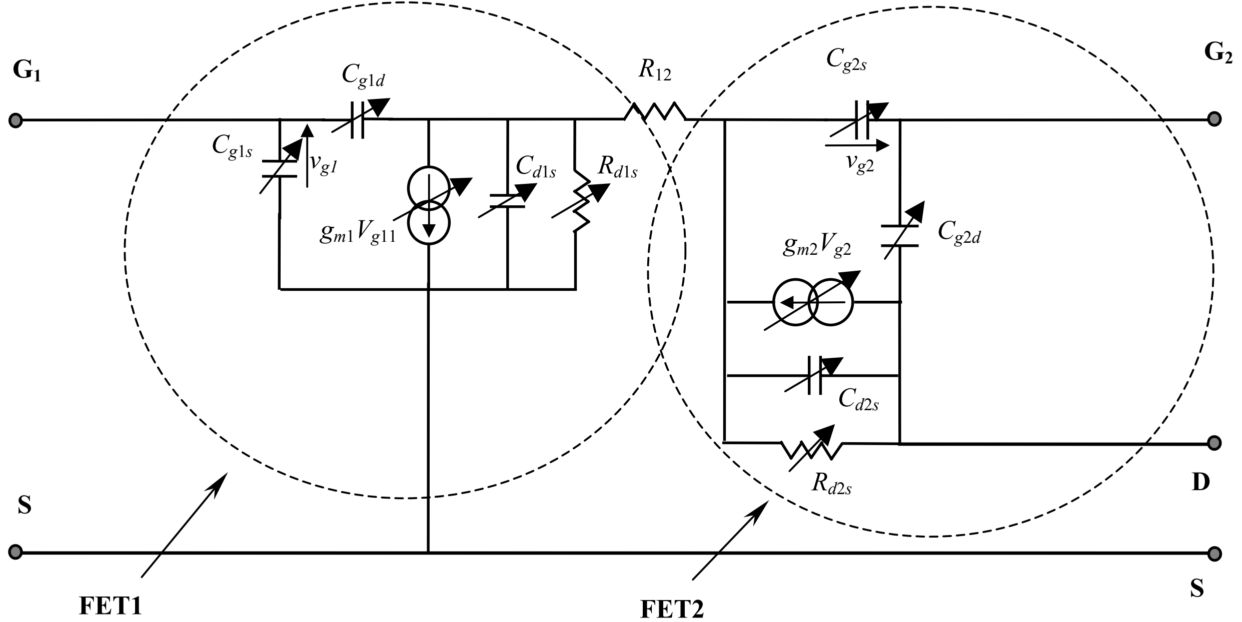

Fig. 1. A simplified dual-gate FET model as two single-gate FETs connected in cascode.

2 The Dual Gate Large-Signal Model

The large-signal active device behavior can be characterized in a variety of ways. Large-signal S-parameter measurements or load-pull measurements are two of the techniques that can be used but require special instruments. Another method that is common in most RF/Microwave laboratories is to perform small signal S-parameter measurements at many DC bias points. Parameter extraction from S-parameter measurements at a given bias point gives the small-signal lumped element model values of the device at that bias point. Repeating this process at other bias points produces a bias dependent lumped element model, i.e. the large-signal model.

For a four-terminal device such as the dual-gate MESFET, three port S-parameter measurements are required. Three port network analyzers are quiet expensive devices and are rare to find due to their high level of sophistication. An alternative to obtain three-port S-parameters is to perform multiple two-port S-parameter measurements between a given set of two ports while terminating the third in its characteristic impedance. For the three-port dual-gate MESFET, three two-port S-parameter measurements are needed to obtain a one-set of three-port S-parameters. Redundant S-parameters resulting from multiple two-port S-parameter measurements can be discarded.

The dual-gate MESFET can be modeled as two single-gate FETs connected in cascode [9]. In this case, the problem of obtaining a large-signal model for the dual-gate MESFET is solved by obtaining the nonlinear dependence of the elements of each of the two single-gate FETs in the cascode connection. In order to achieve that, the Scott and Minasian technique is used [10]. In that technique, the two-port S-parameters for each of the single-gate FETs at various bias points is obtained. Model elements of each single-gate FET, i.e. C_{gs}, C_{gd}, C_{ds}, g_m, and g_{ds} are then obtained by performing parameter extraction using the two-port S-parameters at each bias point. The results in this case give the nonlinear dependence of FET parameters with the DC bias, i.e. V_{gs1}, V_{gs2}, and V_{ds}. For our modeling purposes we

adopt a simplified dual-gate MESFET model as shown in Fig. 1. The following equation relates the three-port z-parameter matrix [Z] of the dual-gate MESFET (which may be derived from the measured three-port S-parameter as in [10]) to the individual two-port z-parameters of the single-gate FET's

$$\begin{array}{lll} Z_{11} = Z_{11}^{I} & Z_{12} = Z_{12}^{I} & Z_{13} = Z_{12}^{I} \\ Z_{21} = Z_{21}^{I} & Z_{22} = \left(Z_{22}^{I} + Z_{11}^{II}\right) & Z_{23} = \left(Z_{22}^{I} + Z_{12}^{II}\right) \\ Z_{31} = Z_{21}^{I} & Z_{32} = \left(Z_{22}^{I} + Z_{21}^{II}\right) & Z_{33} = \left(Z_{22}^{I} + Z_{22}^{II}\right) \end{array} \quad (1)$$

It can be shown from (1) that three of the four two-port z-parameters of FET1 (i.e. Z_{11}^{I}, Z_{12}^{I}, and Z_{21}^{I}) are given explicitly. The fourth z-parameter is given under the assumption that $Z_{12}^{II} << Z_{22}^{I}$ [10], by as $Z_{22}^{I} << Z_{23}$.

3 Results

We have modeled an on-wafer 6-gate 1x100 µm dual gate MESFET manufactured by Nortel Networks. Three-port S-parameter measurements are performed for the device over a DC bias range of gate and drain voltages. The retained ranges are: V_{gs1} = -1.4V ∼ 0.6V (step of 0.2V), V_{gs2} = -1.4V ∼ 0.6V (step of 0.2V), and drain voltage, V_{ds} = 0.0V ∼ 6.0V (step of 0.5V). For each set of three-port S-parameter measurement, the frequency is swept from 0.1 to 26.5 GHz with a step size of 0.25 GHz. For this bias ranges there is a total of 1573 bias points. At each bias point there is a set of two-port S-parameters for each of the two single-gate MESFETs, resulting in 1573 S-parameter files (for each FET). Applying parameter extraction on each S-parameter file produces a set on nonlinear elements (C_{gs}, C_{gd}, C_{ds}, g_m, g_{ds}) at the given bias point. The result is that there are 1573 data points representing the nonlinear dependence of each element on V_{gs1}, V_{gs2}, and V_{ds}. This data is used to generate a neural network model for each FET.

The data points (1573 in total) are first randomized and then split into two sets, a training set and a testing set. About 70% of the data is used for neural model training. The remaining 30% are used to test the validity of the produced neural model.

Three neural models were tested: a three-layer, a four-layer, and a five-layer perceptron models (MLP3, MLP4 and MLP5 respectively). With roughly similar number of neurons, the four-layer model error was 1.2% while that of the three-layer model was 2.7%. No significant improvement is noticed with a five-layer neural model. The four-layer dual-gate MESFET neural model, Fig. 2, has a total of 35 neurons, 22 neurons for the first hidden layer and 13 neurons for the second hidden layer.

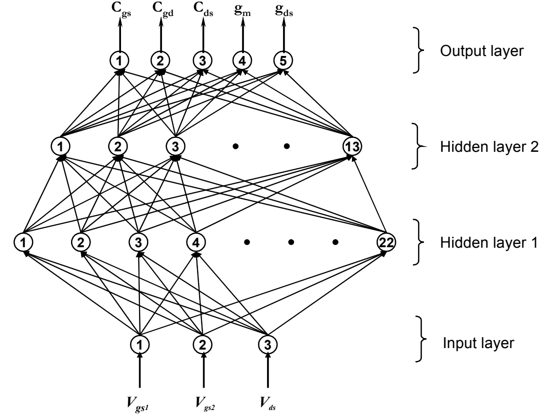

Fig. 2. A four-layer large-signal neural model for the dual-gate MESFET

To illustrate the model results, Fig. 3 shows the modeled and measurement (extracted) values at various bias conditions for the gate-to-source capacitance. The Figure has very good agreement between modeled and measured data.

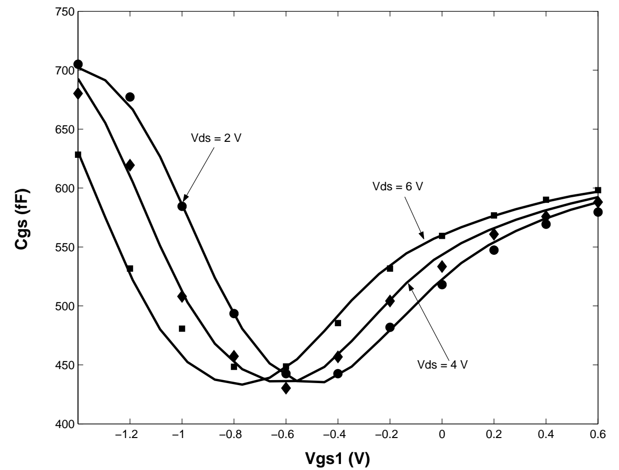

Fig. 3. Modeled (line) and extracted values (from three-port S-parameter measurements) of the gate-to-source capacitance, C_{gs} for V_{ds} = 2V, 4V, and 6V.

The dual-gate MESFET large-signal model is implemented in the Advanced Design Systems (ADS) simulator [13] with the help of Symbolically Defined Devices (SDD) modeling facility. For the large-signal dual-gate MESFET, a three-port

nonlinear model is used. To fully characterize a device in an SDD representation, currents and charges have to be defined at each device port. This includes linear and nonlinear components. Appropriate weighting factors {0 or 1} are used for DC or time derivative operators. After completely defining currents and charges at each port, the model is used as a plug-in component in higher level circuit designs. As an example, the generated neural network model for the transconductance (g_m), is exported as a C-language function.

The ADS SDD model requires port currents rather than conductances. The transconductance FET is related to the drain current by the relation:

$$g_m = \frac{\partial}{\partial V_{gs}} I_{ds}\left(V_{gs}, V_{ds}\right) \qquad (2)$$

Therefore, the drain current is obtained from g_m by integration of (2) as follows:

$$I_{ds} = \int_{V_{gs0}}^{V_{gs}} g_m(V_{gs}, V_{ds})\, dV_{gs} \qquad (3)$$

where V_{gs0} is the pinch off voltage. The integration of (3) is performed analytically using the *Maple* software package [14]. In addition, the ADS SDD large-signal model requires the charge values at each of its ports. Normally, charges are not directly available but capacitance values are. Charges can be obtained from the capacitance values by integration over the appropriate voltage values range. As an example, the gate-to-source charge is obtained from the gate-to-source nonlinear capacitance (and assuming that the capacitance $C_{gs}(V_{gs}, V_{ds})$ is a weak function of V_{ds}) as follows:

$$Q_{gs} = \int_{V_{gs0}}^{V_{gs}} C_{gs}(V_{gs}, V_{ds})\, dV_{gs} \qquad (4)$$

The nonlinear expression of the gate-to-source capacitance is given by a neural network nonlinear function. The integration in (4) is performed analytically using *Maple* software package.

4 Model Validation

The application used in model verification is a variable-gain nonlinear amplifier (Schematic Fig. 4, and layout, Fig. 5). It consists of six dual-gate MESFETs of various sizes connected in parallel. The sizes of the six dual-gate FETs are: 1x10 μm, 1x20 μm, 1x40 μm, 1x80 μm, 2x80 μm, 4x80 μm. The first digit refers to the number of device gates while the second refers to the gate width (W). All transistors have a gate length of 1 μm. The six terminals of the first gate are connected together. Similarly for the drains for the six transistors. Input power is connected to the first gate terminal (gate$_1$) while output power is taken on the common drain. The second gate of each transistor can be independently connected to a DC bias source. This gate controls whether or not the individual transistor is turned on. Setting the DC bias of this gate to approximately 2.0 V turns on the individual transistor, while connecting a DC voltage of -1.0 V or less to the same gate turns a given transistor off. The overall gain of this stage can then be controlled by the number of dual-gate FETs turned on.

For verification purposes, this variable-gain amplifier will be used as a constant gain amplifier with its gain set to a maximum. In other words, all the six transistors are turned on and therefore the output gain is at its maximum.

The measurement setup consists of an on-wafer amplifier stage, an on-wafer probing station, an input signal generator with variable power, a spectrum analyzer and DC power supplies

We used the HP 8662A synthesized signal generator and the Agilent 8565EC spectrum analyzer as the main components of the measurement setup. The bias conditions for the input/output power measurements are: gate$_1$ DC bias, V_{gs1} is set to -0.6 V, the gate$_2$ DC bias, V_{gs2} is set to 2.0 V, the DC drain bias, V_{ds} is set to 5.0 V. The input power is varied form -10.0 dBm till 15.0 dBm in steps of one dBm. The frequency of the input signal is set to 1.2 GHz. The spectrum analyzer is set to measure the fundamental and the higher harmonics of the output power. Measurements are recorded for the fundamental, the second, and the third harmonics. The harmonic balance simulation is setup with a variable input power source. Input power is varied from -10.00 dBm to 15.00 dBm. The frequency of the input power source (single tone) is set to 1.2 GHz. It is to be noted that the cascaded two single-gate FETs acting as the dual-gate FET model are connected through a resistor R_{12}. This resistor models the inter-gate resistance. The value of R_{12} is obtained from a previous work on a similar device [15]. DC bias voltages are also shown on the schematic and are: V_{gs1} = -0.6 V, V_{gs2} = 2.0 V, and V_{ds} = 5.0 V. The values match the bias conditions under which the experimental measurements are performed.

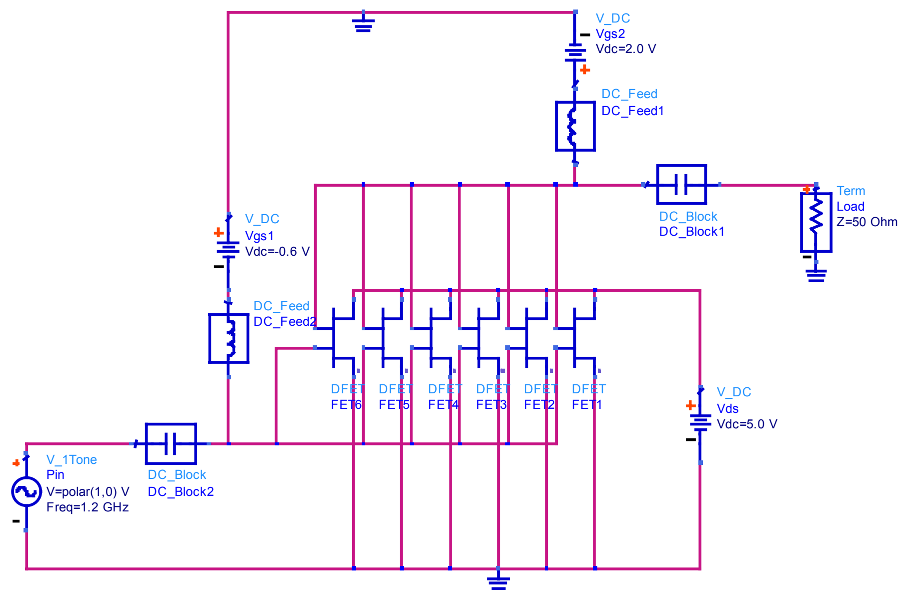

Fig. 4. The schematic of the nonlinear variable gain amplifier

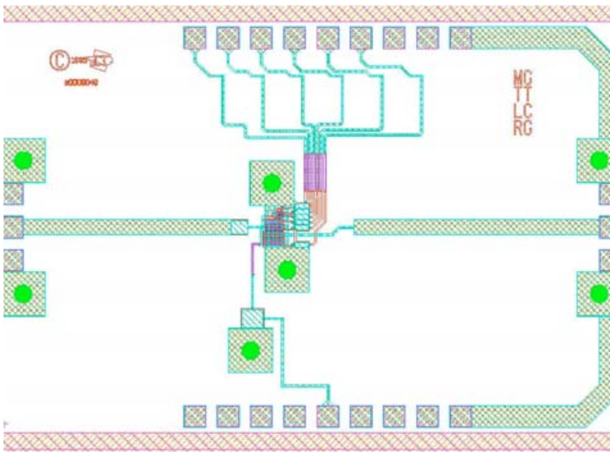

Fig. 5. The layout of the variable gain amplifier with the dual-gate MESFET.

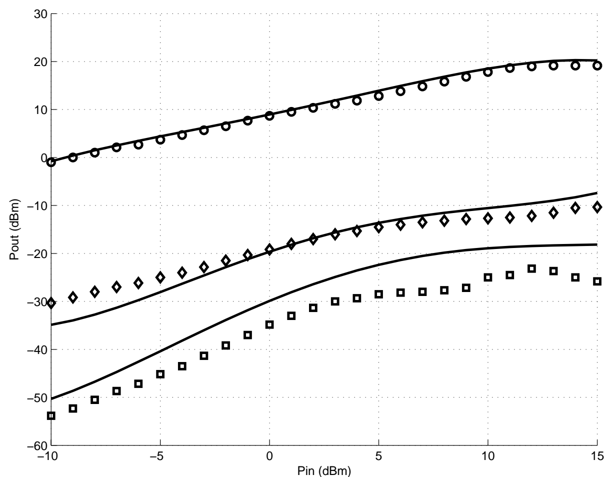

Fig. 6. The measured input/output power for the nonlinear amplifier stage for 1st harmonic (circle), 2nd harmonic (diamond), and 3rd harmonic (square).

Fig. 6 shows the measurements and the harmonic balance simulation of the input/output power transfer characteristics for the single stage dual-gate MESFET amplifier. The results of the first harmonic are in a very good agreement with the measurements. There are some discrepancies, however, between the measurements and simulations for the second and the harmonics. This can be attributed to some model simplifications and second order effects.

5 Conclusion

In this paper we presented an automated methodology for producing a complete large signal model for the dual-gate MESFET. The model is based on neural networks. It takes into account the nonlinearity of the transconductance as well as the junction and overlapping capacitances and output conductance. For the model to be of value to the design community, it is exported to the commercial circuit simulator, ADS. This is performed using the ADS symbolically defined devices (SDD) modeling facility. In order to verify the model correctness, a large-signal amplifier application based on the dual-gate MESFET is setup and measured. Also harmonic balance simulation is setup in ADS with similar conditions. The experimental and simulation results show good agreements for the first harmonic. However, for the second and third harmonic some discrepancies between the model and the measurements are observed. Intuitively, causes for some disagreements between the measurements and the simulations are attributed to some simplifying

assumption regarding the dual-gate MESFET. Inclusion of other lumped elements in the model could improve the accuracy but will significantly complicate the model extraction process and will affect the model usability.

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References:
[1] M. Abdeen and M.C.E. Yagoub, "Neural modeling of the large-signal drain current of the dual-gate MESFET with DC and pulsed I-V measurements", *IEEE Int. Symposium on Circuits and Systems*, Vancouver, Canada, 2004, pp. V_796-V_799.
[2] M. Ibrahim, B. Syrett, and J. Bennett, "Modeling the drain current of the dual-gate GaAs MESFET," *IEEE MTT-S Int. Symp.*, Philadelphia, PA, 2003, pp. 2113-2116.
[3] M. B. Jenner, "A large-signal compatible dual-gate MESFET dc model," *IEEE European Conf. on Circuit Theory and Design*, Stresa, Italy, 1999, pp. 888-891.
[4] F. Wang and Q. J. Zhang, "Knowledge-based neural models for microwave design," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2333-2343, 1997.
[5] F. Wang, V. K. Devabhaktuni, and Q. J. Zhang, "A hierarchical neural network approach to the development of a library of neural models for microwave design," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2391-2403, 1998.
[6] P. M. Watson and K. C. Gupta, "Design and optimization of CPW circuits using EM-ANN models for CPW components," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2515-2523, 1997.
[7] J. Xu, M. C. E. Yagoub, R. Ding, and Q. J. Zhang, "Neural-based dynamic modeling of nonlinear microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 2769-2780, 2002.
[8] Y. Fang, M. C. E. Yagoub, F.Wang, and Q. J. Zhang, "A new macromodeling approach for nonlinear microwave circuits based on recurrent neural networks," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2335-2344, 2000.
[9] T. Furutsuka, M. Ogawa, and N. Kawamura, "GaAs dual-gate MESFETs," *IEEE Trans. Electron Devices*, vol. 25, pp. 580-586. 1978.
[10] J. Scott and R.A. Minasian, "A simplified microwave model of the GaAs dual-gate MESFET", *IEEE Trans. Microwave Theory Tech*., vol. 32, pp. 243-248, 1984.
[11] M. Abdeen and M.C.E. Yagoub, "TopFinder: A new and efficient tool for topology construction and parameter extraction for RF/Microwave transistors," *Electronic Components and Technology Conf.*, New Orleans, LO, 2003, pp. 1541 -1545.
[12] *NeuroModeler Version 1.2*, Q.J. Zhang, Department of Electronics, Carleton University, Ottawa, ON, Canada.
[13] ADS user manual, "User defined models", May 2003.
[14] Maplesoft, Waterloo, Ontario Canada (www.maplesoft.com).
[15] M. Ibrahim, "Modeling of the dual-gate GaAs MESFET", *Ph.D. Dissertation*, Carleton University, Ottawa, Canada, 2003.