High Performance RF-Microwave Multilayer Integrated Components For Wireless Applications

YASAR AMIN, PROF. HANNU TENHUNEN, PROF.DR.HABIBULLAH JAMAL,
DR. LI-RONG ZHENG, XINZHONG DUO
Royal Institute of Technology, Stockholm, SWEDEN and
University of Engineering and Technology Taxila, PAKISTAN

Abstract: - Future high-performance wireless communication applications such as wireless local area networks (WLANs) around 5GHz require low power and high quality integrated transceiver solutions. The integration of RF front-end especially poses a great challenge to these applications as traditional system on chip (SOC) approach is quite inefficient. A system on package approach can address the problems in an optimum way. In this paper we present a comparison of different passive element fabrication choices. These passives are to be fabricated between different modules on an MCM-D substrate. Inductors and capacitors are compared on the bases of their Q-factors and SRF (self resonance frequency). RF receiver module for 5GHz wireless LAN applications is implemented using benzocyclobutene (BCB) as interlayer material.

Key-Words: - Low noise amplifier, bandpass filter, downconverter, MCM-D, RF front-end, system-on-chip, system-on-package, transceiver.

1 Introduction

For future wireless communication systems we see an important trend toward more flexible and wideband (multimedia) applications and toward higher carrier frequencies. Good examples of these trends are the upcoming standards for wideband wireless local area networks (WLANs) in the 5-6 GHz band. It is quite a challenging task to design their analog front-ends. Apart from high operating frequency critical aspects are the wide band width, large dynamic range and a good linearity.

For portable and battery powered applications, low power consumption as well as a high level of integration to reduce size and weight are essential. In current digital communication transceivers, the large number of discrete passive components mainly in the radio front-end is an important bottleneck for further integration. The new implementation paradigm called "system-on-a-package' (SoP) can increase the level of integration of these future wireless transceivers and at the same time reduce power consumption.

In Section 3, we discuss the prospects and limitations of a single-chip approach. In the Section 4, we present the single package approach, which uses a thin film MCM interconnection technology (MCM-D) to interconnect the different system subcomponents. A large number of components (passive) can be integrated using this approach that is required in traditional radios onto the MCM substrate. Starting from a printed wire board (PWB) radio design, a more compact MCM module could be derived by mounting different active components as bare die or even as packaged components on the MCM substrate by means of flip-chip interconnection technology.

2 Specifications of a 5GHZ WLAN

Standardization activities for wireless local area networks (WLAN) in the 5 GHz ISM band have been evolving for a few years already. The American IEEE and European ETSI organizations are finalizing their respective standards for the 5 GHz band: IEEE 802.11a [1] and HIPERLAN/2 [2]. These two standards define nearly identical systems, based on orthogonal frequency division multiplexing (OFDM) modulation. OFDM is a multicarrier modulation technique that efficiently manages intersymbol interference and multipath distortions, making it very suitable for indoor wireless communications. The standards foresee several data rates up to 54 Mbps, using different modulation schemes at different coding rates. The modulation schemes can be binary phase shift keying (BPSK), quadrature phase shift keying (QPSK) and quadrature amplitude modulation with 16 (16-QAM) and 64 points (64-QAM). The IEEE 802.11a standard defines three frequency bands that can be used. A first band extends from 5.15 to 5.25GHz, the second from 5.25 to 5.35 GHz and the

third from 5.725 to 5.825 GHz. HIPERLAN/2 specifies two bands: from 5.15 to 5.35 GHz and from 5.470 to 5.725GHz. Our design only considers the frequency range from 5.15 to 5.35 GHz, which is common to both standards. This band is divided into eight channels with a nominal spacing of 20 MHz. The IEEE 802.11a standard specifies further that the receiver should be able to receive a signal between -85 dBm and -30 dBm at the antenna and that the noise figure of the whole analog receiver chain should be less than 10 dB. Apart from that, the receiver must be able to withstand the effects of out-of-band blocking signals up to 0 dBm [3]. The design tool is Agilent ADS (Advanced Design System). ADS is a powerful and one of the most popular CAD tools in industry for wireless system design. The starting point for the presented SoP approach is a multichip module (MCM) technology. A substrate with low losses is required for RF applications. Here, a thin-film technology (MCM-D) with an Orosilicate glass substrate is used. This is a low-cost material with high resistivity and low microwave loss. The lithographic nature of a thin film technology guarantees lower component tolerances [4] in comparison with standard thick film or low temperature co-fired ceramic (LTCC) processes. The package substrate provides a good environment for integrated passive elements. Resistors, capacitors and inductors can be fabricated on the substrate with a thick-film or thin-film process. In principle, all passive subcircuits can be built on package substrates with connections to on-chip active subcircuits. The partition of what functions are on or off chip should be determined by the optimization of cost, size, and performance. Usually, the passive components and subcircuits on package substrates have higher quality factors than their on chip counterparts. However, full integration on a chip usually means lower cost and smaller size [5].

3 System-on-a-Chip (SOC) Integration of RF Transceivers: Feasible or Not?

Traditionally, radio front-ends have been based on the superheterodyne architecture that makes use of one or more IFs with image-reject filters on every IF. At the lowest IF, typically an analog bandpass filter with high quality factor (Q) is required for channel selection. The superheterodyne transceiver has a good performance but it is not suited for a high level of integration, mainly because of the different high-Q analog bandpass filters, which are typically implemented as discrete LC, ceramic or surface acoustic wave (SAW) filters. On the other hand, a high degree of integration is helpful to obtain high performance systems with small sizes and weight, in conjunction with low power consumption. At first sight it seems that a single chip solution is the best option that even combines the RF front-end with the digital signal processing (DSP) core of the transceiver. In this case the most economical technology will be the digital CMOS. During past years much research has been focused on this single-chip CMOS route for RF transceivers [6]-[7], and this has given several trends leading to more integrated transceivers.

3.1 Trends and Problems

Evolution of CMOS technologies allowing Si RF Design—In the majority of today's front-end implementations, most active components are realized in GaAs (e.g., low-noise amplifiers (LNA), power amplifiers (PA), mixers, antenna switches, etc.) and very often as individually packaged components. In commercial products, the use of CMOS technology is limited to the IF and baseband sections. In recent years, much research has been devoted toward CMOS integration of RF circuits [6]-[7]. But there are still several problems that could prevent single-chip integration of complete RF front-ends in CMOS in the future.

A number of front-end blocks are (and will most likely remain) impossible to integrate in CMOS, e.g., high-Q RF and IF bandpass filters or antenna switches. For some blocks, there is an important performance penalty associated with standard digital CMOS compared to a GaAs or Si (SiGe) bipolar implementation. Depending on the application specific requirements, some of these blocks will have to be kept off-chip and implemented in GaAs, such as very low-noise amplifiers [with noise figure (NF) around 1 dB] and power amplifier with an output power of several watts. Sometimes [8], [9] a power preamplifier is integrated on-chip, but the actual PA is off-chip. Another problem that may prevent the integration of PA is the interference of very large signal at the output of PA with that of the weak one in the receiver front-end. The maximum allowable supply voltage decreases with CMOS technology scaling. As a result the analog front-end blocks realized in deep submicron digital CMOS technologies have smaller headroom. This limits the dynamic range, which may not be allowable in future digital applications.

Mixed-signal Integration— The rationale behind the research in CMOS RF design is the perspective of future single-chip integration of the RF front-end

with the digital baseband processing circuits in deep submicron (standard digital) CMOS technologies. It would be fruitful to present some problems that could prevent single-chip integration of mixed analog-digital transceivers. In the single-chip solutions of mixed-signal front-ends, the signal-to-noise ratio (SNR) of the analog block can degrade due to coupling between different functional blocks, especially the coupling via the substrate and the power lines from the digital part to the analog blocks.

On-chip Inductors— In the past few years [10], [11], there has been a trend in silicon RF design to use on-chip inductors. Integrating inductors would allow eliminating a large part of discrete passives used in many commercial RF front-end implementations. On-chip inductors too have several disadvantages and problems. The quality factor (Q) of on-chip inductors is very low compared to discrete inductors. Unloaded Qs of on-chip inductors are typically not higher than five. By using several metal layers in parallel or by using thick metal layers, Qs of around ten will probably be feasible in the frequency range 5-6 GHz. By using even more advanced and costly technological solutions (low-k dielectrics, Cu metallization), Qs of about 20 are predicted in future deep submicron CMOS processes, but this seems to be an upper limit in the frequency range of interest for standard CMOS technologies [11]. High Qs are important in a number of RF blocks, because they are directly related to block performance and power consumption. For example, phase noise of a VCO is inversely proportional to the square of the Q of the LC tank [12] and directly proportional to the amplifier noise figure. The Q of the tank is limited by the component with the lowest Q, which is more often the inductor. Given that increasing the operating power can often reduce noise figure, we can say that power and inductor Q can be traded to achieve a given phase noise specification. High Qs are, e.g., also important to obtain low noise figure in an LNA [11].The area of inductor and of passive components in general in RF circuits is very large. For example, in the 2.4 GHz WLAN front-end described in [13], the passive components (mainly inductors) consume about 60% of the chip area. Since the cost per square millimeter of deep submicron silicon processes is increasing rapidly with technology scaling and the size of inductors does not scale, the cost of these integrated inductors will become more and more important in fully integrated RF front-ends.

New Architectures—Alternatives for the superheterodyne front-end architecture have been explored recently, to allow higher levels of front-end integration by eliminating high-Q discrete IF bandpass filters: zero-IF [14], [9], low-IF [8], wideband IF double conversion [15] architectures, etc. These architectures have a number of features in common, e.g., the use of quadrature (up-down) conversion and channel selection filtering at (near) baseband frequencies, which can be integrated in CMOS using analog or even digital signal processing. These new architectures also have some disadvantages and problems compared to the classical superheterodyne architectures.

The SNR performance of these architectures based on quadrature conversion is lower than for the traditional superheterodyne architectures. The mirror signal suppression is limited by the imperfect quadrature generation at RF frequencies and mismatches in the in-phase and quadrature (I/Q) signals to about 30-40 dB. However, for most digital telecom applications this limitation does not present a problem, and very often the receiver SNR is limited by other effects, e.g., phase noise, distortion, adjacent-channel interference, etc. At least one discrete RF bandpass filter in the receiver (a blocking filter) as well as in the transmitter (to limit out-of-band spurious emissions) is still required.

3.2 Solutions

Some of the problems stated above can probably be solved (at least partially) by further planned developments in deep submicron CMOS technologies or by going to specialized, non standard (expensive) technology options. Antenna switches can probably be implemented by using silicon-on-insulator (SOI) technologies. Very high performance, high frequency RF blocks could be implemented in silicon by going to SiGe BiCMOS technologies. The voltage scaling problem can be eliminated by using BiCMOS technologies, where the bipolar devices can typically stand higher supply voltages. Other solutions in CMOS technology are triple-well technology and low VT devices. The substrate coupling problem between analog and digital circuits could be alleviated by going to triple-well technology, deep trench isolation, SOI, etc., and finally, the use of thicker metal layers, Cu metallization or low-k dielectrics can increase the quality factor of on chip inductors.

4 An MCM-D Substrate as a Carrier

Deposited thin-film multilayer. An MCM-D substrate technology has been employed in this work. The MCM-D technology developed by GEC

Plessey Semiconductors has been described in detail elsewhere [16]. One of the constraints on the design of integrated RF systems is the availability of suitable and cost effective components. The system builder is also facing demand for ever greater functional density in RF products, particularly for portable products such as mobile phones and sub notebook computers [17]. MCM-D technology offers many of the necessary components and also gives advantages of size, repeatability and externally component count reduction. The MCM-D technology [Figure 1] allows the integration of different families of ICs together with integrated passive components to produce miniature radio modules and RF functions which offer considerable size and performance advantages over conventional discrete solutions [18], [19]. The benefits are further enhanced by the use of MCM-D passive components to produce structures such as filters which would normally consume significant space and cost in a conventional design [18]. MCM-D processes have been offering 4 to 10 fold reductions in the area of RF functions when compared to the surface mounted equivalent [20]. MCM-D technology as a solution for use in RF systems offers many significant advantages over more traditional technologies. In particular the size reductions and performance improvements possible allow product developers to meet more closely the requirements of the marketplace. The technology then eases many of the design problems in bringing RF systems into production [18].

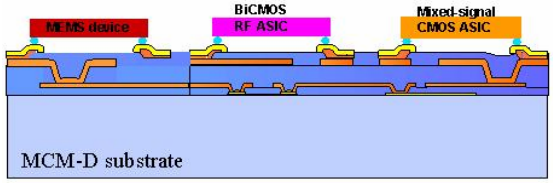

Figure 1. MCM-D Technology

5 Designs of Passive Components

Integration of passive elements in a package is the most important factor in chip-package co-design's success. Without this technology, chip and package designs are nearly independent. With the ability to integrate resistors, inductors, capacitors and distributed transmission-line elements, chip and package designs couple closely. Chip designers can then move critical passive elements that require high quality factors and large space off the chip. This improves circuit performance and potentially saves costs [5].

The conventional planar spiral inductor has been fabricated on a single layer. Increasing inductance has been obtained by increasing the number of turns laterally. As the area increases proportionally to the number of turns, Rs, Cs and Ls increase while Rp decreases. Therefore, this topology is expected to have both low Q and self-resonance frequency (SRF). One of the important factors of an inductor is the quality factor (Q). High Qs at the frequency range of interest can be obtained by designing multilayer inductors [21]. In this design both multilayer as well as single layer inductors has been designed.

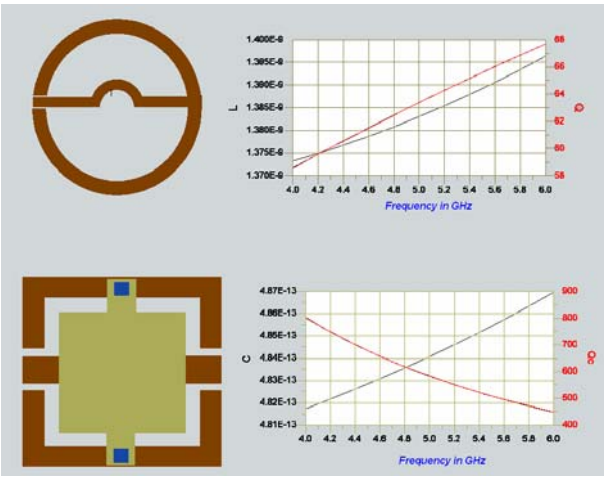

Figure 2. Layout and Q of Passives

Therefore, results for extremely compact 0.5 (Single Layer) and 1.5-turn (Multilayer) inductors having a line width of 90 µm and 40 µm respectively. For 0.5-turn inductor, the Q is 64 as shown in Figure 2 and the inductance, Leff, is 1.4 nH at 5.25 GHz and for 1.5-turn inductor, the Q is 31 and the inductance, Leff, is 3.0 nH at 5.25 GHz. Also, the thick Aluminum metallization in the packaging process made it possible to get a very high-Q. This has decreased the shunt parasitic capacitance and reduced the eddy current flowing in the ground plane, producing negative mutual inductance effect. As a result, higher Q and Leff have been achieved [22]. The inductors used for filter design have been designed on single layer because the metal layer 1 is only 0.5 µm thick whereas, the inductors used for Low noise amplifier have made use of both layers because high inductances as well as better Q were required at the same time. The inductors have been made in the metal 2 layer (3 µm thick Aluminum). The inductor values range between 0.3 to 3.6 nH, with a maximum quality factor Q up to 64 at 5.25 GHz. The frequency of maximum Q and the maximum value of Q itself can be exchanged.

Inductors with lower values have higher Q values, because they can be smaller (lower parasitic) or use wider metal tracks. An inductor with a larger inductance value using wider tracks would suffer a lower frequency of self-resonance due to higher parasitic capacitance. Therefore, inductors with lower inductance values can have higher Q-factors, given a certain technology and application (i.e., the required operation frequency).

6 Receiver Front-End Blocks

The presented integration demonstrator contains two bandpass filters, an LNA and a downconversion mixer. The prototype module is intended to demonstrate the concept of SoP. A lot of optimization work on the different blocks, especially on the LNA, is still possible.

An on-package integrated multilayer filter offers a more attractive implementation than on-chip and discrete filters [21]. There is possibility to improve the filter design by making multilayer inductors by having the freedom of equal thickness of metal layers. The size of the inductors influences much on the quality factor. The quality factor improves by increasing the conductor coil width, inner diameter. However, increase in inductance occurs by increasing the number of turns but at the same time if the inductor is drawn on one layer, this causes the decrease in quality factor which in turn increases the insertion loss of the filters. This problem can be solved by designing multilayer inductors explained. All components are matched for 50Ω, which is not necessarily an optimum, but is often a requirement when using of-the-shelf components or when measurement of the separate functions is mandatory. It consists of a single class A stage. The transistor is available as bare die and is mounted on the MCM-D substrate with the flip-chip technique, explained. All the passives are integrated in the MCM.

The low noise amplifier is built around a GaAs high electron mobility transistor [23]. Amplifier is designed to be unconditionally stable, which means that the amplifier is stable for every possible source and load impedance. The amplifier consumes 10 mA for a 2 V power supply [23]. The downconverter is a GaAs MMIC [9]. The device has a minimum specified gain of 12 dB. The complete receiver front-end layout design is shown in Figure 3 and has a measured conversion gain of 18 dB shown in Figure 4. The results are comparable with [21], in which copper metal is used whereas, in our design aluminum metal is used which is a cheaper solution. The whole structure measures 3275 µm by 5781 µm.

The conversion gain is with in the acceptable range, it can be further improved by making the filters with more improved performance i.e., with low insertion loss.

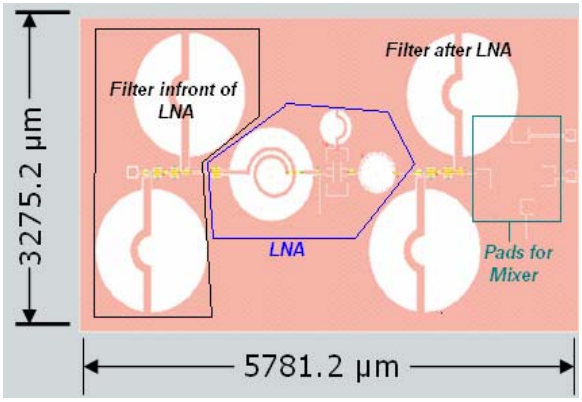

Figure 3. Receiver front-end layout

7 Conclusions

In this document, we have shown the advantages of SoP over single-chip solutions. Single-chip solutions do not provide complete system integration. A SoP approach using an MCM-D technology is a more complete solution that is compact and that is more flexible than a single-chip approach. Moreover, we have demonstrated that high-quality passive components can be embedded on an MCM-D substrate. These passives can be used together with mounted active components as well as for the design of integrated RF bandpass filters and matching networks. We have built prototype SoP-integrated RF modules of a receiver front-end with commercial bare-die components to demonstrate this concept. This receiver has a measured gain of 18 dB, making it suitable to serve as a part of a 5 GHz Wireless LAN system. A single-package approach is neither limited to one certain technology, nor to the availability or limits of commercial components, thus creating more degrees of freedom for design. Also the antenna is a candidate for future integration in the MCM-D module.

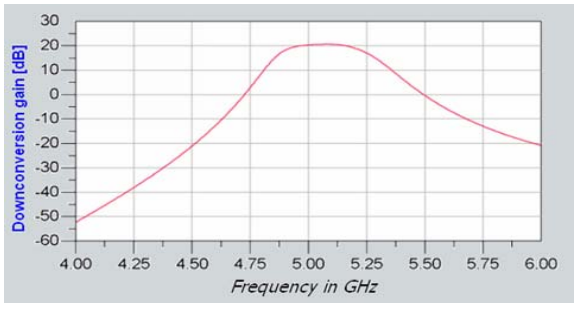

Figure 4. Downconversion Gain

References:

[1] Arnold, R.G., Faulkner, C.C., Pedder, D.J., *"MCM-D and direct module attach for RF applications"*, Multichip Modules and High Density Packaging, 1998. Proceedings 1998 7th International Conference on 15-17 Apr 1998 Page(s): 268 -272.

[2] Draft supplement to standard, part II: wireless LAN medium access control (MAC) and physical layer (PHY) specifications: High speed physical layer in the 5 GHz band, Tech. Rep. P802.11a/D7.0, July 1999.

[3] J.Laskar, *"System on package and system on chip trade-offs",* presented at the IEEE workshop on circuits and Systems for Wireless Communications and Networking, South Bend, IN, Aug.2001.

[4] J. Lasker, A. Sutono, C.-H. Lee, M.F. Davis, A. Obatoyinbo, K. Lim and M. Tentzeris, *"Development of integrated 3D radio front-end system-on-package (SOP)"*, in Proc. IEEE GaAs IC Symp., Baltimore, MD, Oct. 2001.

[5] G. Carchon, K. Vaesen, S. Brebels, W. De Raedt, E. Beyne, B. Nauwelaers, *"Multilayer thin-film MCM-D for the integration of high-performance RF and micrwave circuits",* IEEE Trans. Comp. Packag. Technol. vol. 24, pp.510-519, Sept. 2001.

[6] R. Tummala, V.K.Madisetti, *"System on chip or system on package?"*, IEEE Design & Test of Computers, Vol 16, pp 48-56, Apr-Jun 1999.

[7] K.L Tai, *"System-In-Package (SIP): challenges and opportunities"*, Design Automation Conference, 2000. Asia and south Pacific, 2000 pp 191-196.

[8] Sundaram, V., Liu, F., Dalmia, S., White, G.E., Tummala, R.R., *"Process integration for low-cost system on a package (SOP) substrate",* Electronic Components and Technology Conference, 2001. Proceedings 51st, 2001 Page(s): 535 -540.

[9] TriQuint Semiconductor Inc., Double balanced MMICmixerTGC1452.

[10] Jenshan Lin; *"Chip-package codesign for high-frequency circuits and systems",* Micro, IEEE, Volume:18Issue:4,Jul/Aug 1998 Page(s): 24 -32.

[11] Troster, G.; *"New Route In System Integration: Chip-Package Codesign",*Micro, IEEE, Volume: 18 Issue: 4 , Jul/Aug 1998 , Page(s): 7 -9.

[12] McWilliams, B., Demmin, J*., "Technical issues with multichip module packaging",* Telesystems Conference, 1992. NTC-92., National, 19-20 May 1992 .Page(s): 9/17 -9/24.

[13] R.G.Arnold, C.C.Faulkner & D.J.Pedder, *"Silicon MCM-D Technology for RF Integration",* proceedings of the 6th International Conference on Multichip Modules, Denver, Colorado, April 2-4 1997.

[14] Arnold, R.G., Faulkner, C.C., Pedder, D.J., *"Silicon MCM-D technology for RF integration"*, Multichip Modules, 1997, 6th International Conference on, 2-4 Apr1997 Page(s): 340 -344.

[15] K.Takashi, S.Fujita, T.Toshida, H.Sakai & M.Sagana, *"An Advanced mm wave flip chip IC integrating different kinds of active devices"*. 1996, Proc. IEE MTT-S Conference pages 1619-1622.

[16] Arnold, R.G., Faulkner, C.C., Pedder, D.J., *"MCM-D and direct module attach for RF applications",* Multichip Modules and High Density Packaging, 1998. Proceedings 1998 7th International Conference on 15-17 Apr 1998 Page(s): 268 -272.

[17] Stephen H. Hall, Garret W. Hall, James A. McCall, *"High Speed Digital System Design"*. Wiley-Interscience Publication.

[18] D. Wein, P. Anderson, J. Babiarz, J. Carter, N. Fulinara, M. Goetz, *"Microwave and Millimeter-Wave Packaging and Interconnection Methods for Single and Muliple Chip Modules",* IEEE GaAs IC Symposium, pp. 333-336, 1993.

[19] N. Ono, Y. Fuchida, J. Onomura, M. Amano, M. Sugiura, K. Yoshihara, E. Takagi, M. Konno, *"60-GHz-band Monolithic HEMT Amplifiers Using BCB Thin Film Layers on GaAs Substrates",* Asia- Pacific Microwave Conference, 1998.

[20] M. McNulty, J. Schnell, D. Nixon, *"Microwave Multichip Modules Using Low Cost Microwave Chip on Flex Packaging Technology",* International Conference on Multichip Modules and High Density Packaging, 1998.

[21] Diels, W.; Vaesen, K.; Wambacq, P.; Donnay, S.; De Raedt, W.; Engels, M.; Bolsens, I., *"Single-package integration of RF blocks for a 5 GHz WLAN application",* Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on],Volume:24Issue:3,Aug2001Page(s):384-391.

[22] Draft supplement to standard, part II: wireless LAN medium access control (MAC) and physical layer (PHY) specifications: High speed physical layer in the 5 GHz band, Tech. Rep. P802.11a/D7.0, July 1999.

[23] Monolithic Semiconductor S.A.S., High electron mobility transistor EC2612. [Online] Available: www.ums.com