I-V and C-V methods to extract Al/polysilicon Schottky diode parameters

FELLA BOULGAMH[1], AZEDDINE TELIA[2], MOHAMED REMRAM[2], ABDELBAKI DJOUAMBI[1]

(1) Centre Universitaire Larbi Ben M'hidi, Oum El-Bouaghi ,

(2) Département d'Electronique, Faculté des sciences de l'ingénieur,
Université Mentouri, Route Ain El-Bey, Constantine 25000

Abstract: Series resistance, ideality factors, saturation currents and doping concentrations have been determined using I-V and C-V techniques. However, the usual equations cannot fit some diodes, may be because they are too approximated or because other mechanisms are present. In this work we use two methods based on C-V and I-V measurements to extract Schottky diode parameters. These methods are very easy to use and give results with more precision even when characteristics behavior is far from ideal. The influence of the material (polysilicon) hase also been investigated.

Keywords: I-V curves; C-V curves; Schottky diodes; polysilicon.

1 Introduction

Microelectronics has been an engine for growth for the past five decades in nearly all technological fields. From a materials standpoint, it is largely based on single cristalline silicon. Furthermore, polysilicon has drawn considerable interest in some years ago due to its wide use in the fabrication of low cost terrestrial solar cells. The properties of polysilicon differ in important ways from those of single-crystal silicon due to the presence of grain boundaries [1,2]. These grain boundaries generally contain a high density of impurities and trapping centers which have significant effects on device performance [3].
In the other hand, the non uniformity of the grain size in polysilicon films lead to non uniform current flow and restricts detailes modeling of conduction in polysilicon [4]. Then, experimental characterizations are needed to understand and model polysilicon films.

All semiconductor devices and materials are characterized through the use of test structures. Metal-semiconductor contacts are the subject of considerable interest, and the capacitance-voltage (C-V) and current-voltage (I-V) as electrical characterization techniques are most commonly used to extract junction parameters.
For the C-V method it is important that C^{-2} versus V plots be linear and independent of frequency. For the I-V ones ln(I) versus V must have the same behavior. Indeed, deviations from linearity are commonly observed in polysilicon structures.

In the present work, we use and developp two iterative methods to find junction parameters based on C-V and I-V measurements.

2 Conventional I-V and C-V methods

2. 1 I-V method

The thermionic current-voltage relationship of a Schottky barrier diode, neglecting series and shunt resistance, is given by:

$$I = I_s[\exp(\alpha V)-1] \qquad (1)$$

where I_s is the saturation current, $\alpha=q/nKT$ with n the ideality factor and $KT/q = 25.10^{-3}$ V at T=300K.
When series resistances are considered the equetion (1) becomes [4]:

$$I = I_s [\exp(\alpha(V-R_sI))-1] \qquad (2)$$

The ideality factor n incorporates all unknown effects making the device non linear when greater to unity.
Data plotted as Log (I) versus V are linear when V>>KT/q.
In the conventional I-V method, the saturation current I_s is determined by an extrapolation of the Log (I) versus V curve to V = 0. The current axis intercept for the straight-line portion of this semilog plot at V = 0 is given by I_s.

The deviation of the Log(I)-V curve from linearity for high voltages is $\Delta V = IR_s$, allowing R_s to be determined according to $R_s = \Delta V/I$. When R_s and I_s are determined, we can easily obtain n value.

2. 2 C-V method

The capacitance-voltage (C-V) technique relies on the fact that the width of a reverse-biased space charge region of a semiconductor junction device depends on the applied voltage.
The capacitance per unit area of a Schottky diode is given by:

$$C/A = [(Nq\,\varepsilon) / (2(V_B - V)]^{1/2} \tag{3}$$

Where V_B is the barrier height, V the applied bias voltage, N the donor or acceptor density, ε the dielectric constant of semiconductor, q the magnitude of the electronic charge and A the contact area [5].
If one then plots the experimentally obtained values of $1/C^2$ versus bias voltage, N and V_B may be determined from the slope and the intercept on the abscissa, respectively.

In principle, I-V and C-V methods are quite simple; in practice, a number of complications may arise which make techniques more difficult to use. Some of these complications lead, in general, in a non-linear behavior of Log (I)-V and ($1/C^2$)-V plots and it becomes very hasardous to determine diode parameters with accuracy.

3 Iterative methods

3.1 Evaluating Current-Voltage (I-V) characteristics

Here, it will be shown how to determine diode parameters such as saturation current, ideality factor and series resistance from I-V characteristics of Schottky diodes or p-n junctions.
In this part, calculations are based on a method developped by A. Kaminski et al. [6, 7]. By writing the relation in Eq. (2) in its logarithmic form, it was demonstrated that

$$Y = \alpha(-R_s + X) \quad \text{for} \quad I \gg I_s \tag{4}$$

with $Y = \dfrac{\ln(I/I_0)}{I - I_0}$, $X = \dfrac{V - V_0}{I - I_0}$, $\alpha = \dfrac{q}{nKT}$ and (V_0, I_0) is a point of the I-V curve.
To get a better accuracy it consider a set of I_i - V_i data giving rise to a set of X-Y values, with i varying from 1 to N. We calculate X and Y values for $I_0 = I_{i0}$ and $I = I_{i0+1}$ up to $I = I_N$. This gives (n-1) pairs of X-Y data. We start again with $I_0 = I_{i0+1}$ and $I = I_{i0+2}$ up to I_N and get (n-2) additional X-Y data, and so on, up to $I_0 = I_{N-1}$.
Finally, we obtain n(n-1)/2 pairs of X-Y data that means more values for the linear regression. The linear regression of Eq. (2) gives α and R_s. At last, knowing R_s, the reverse saturation current is obtained by plotting ln I versus ($V-IR_s$).

3. 2 Evaluating Capacitance-Voltage (I-V) characteristics

Here we develop a new method based on the same principle of I-V method described above. This mehod concerns directly the usual measured C-V data.
We start from

$$\frac{1}{C^2} = \alpha V + \beta \tag{5}$$

with $\alpha = \dfrac{-2}{A^2 Nq\varepsilon}$ and $\beta = \dfrac{2V_B}{A^2 Nq\varepsilon}$

For a data pair defined by (V_0 , C_0) we have

$$\frac{1}{C_0^2} = \alpha V_0 + \beta \tag{6}$$

By subtracting Eqs. (5) and (6) we obtain

$$\frac{1}{C^2} - \frac{1}{C_0^2} = \alpha(V - V_0) \tag{7}$$

Taking $Z = \dfrac{1}{C^2} - \dfrac{1}{C_0^2}$ and $X = V - V_0$ we have a straight line

$$Z = \alpha X \tag{8}$$

We consider a set of C_i-V_i data giving rise to a set of Z-X values, with i varying from 1 to N, and we continue in the same way as I-V itterative method.
We determine the doping concentration N from the linear regression of Eq. (8) givingα. When this one is determined we can obtain β by fitting the relation in Eq. (5) by a linear function defined by the value of the slope α.

The advantage of this method is that when $1/C^2$-V curve present several linear parts with different slopes, it can inform about the range of V which give accurate values of the barrier height V_B.

4 Results

Test structures are Schottky diodes Al/polysilicon with an area of 1mm^2. Polysilicon wafers are P type elaborated by PHOTOWATT and doped Bore at 10^{17}cm^{-3}

We were interested to polysilicon because it presents, generally, a non linear behavior of its characteristics which let the evaluation of diode parameters very difficult.

4. 1 C-V results

Experimental C-V characteristics at 1 MHz show that the capacitance varies proportionally with $V^{1/3}$ as given in Fig.1. This behavior is also observed on polysilicon junctions by several authors [8].

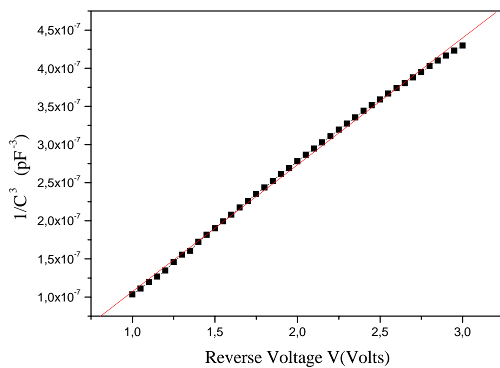

Fig.1. Characteristics 1/C^3 as a function of the reverse bias voltage.

From the slope, we find N = 7,18 10^{16} cm^{-3}.
A value of 7,5.10^{16} cm^{-3} is obtained from Z-X linear regression as given in Fig. 2. One can sea that the second value give more precision in the determination of N because it approaches the doping value 10^{17} cm^{-3} .

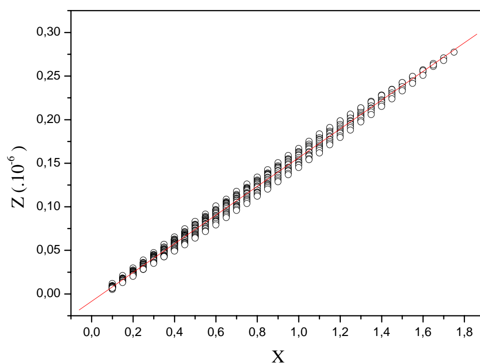

Fig. 2. Z-X characteristics.

4. 2 I-V results

In order to calculate saturation current I_s, ideality factor n and series resistance R_s we use the method presented above. An example of experimental I-V characteristic is given in Fig. 3 and one can see that ln(I)-V curve is not linear .
Then the conventional method becomes very difficult to use.

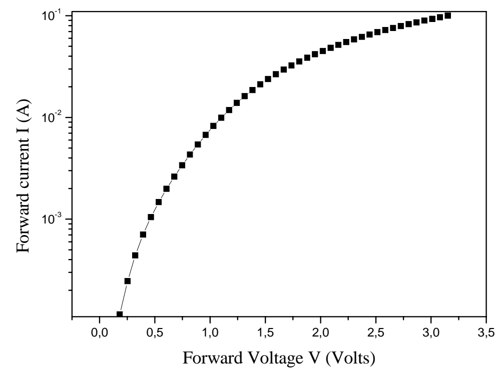

Fig. 3. Log (I) versus V plot for Al/polysilicon Schottky diode.

So we use Y-X plot to determine diode parameters. Linear regression in Fig. 4 gives an ideality factor n = 4.9 and a series resistance R_s = 530.54 Ω .

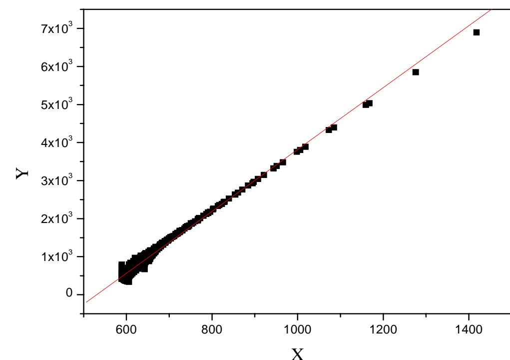

Fig. 4. Y-X characteristic.

By plotting ln (I) versus (V-R_sI) curve, as shown in Fig. 5, we find saturation current I_s equal to 5.84 mA.

The device presents high value of ideality factor. This can be explained by the presence of grain boundaries and therefore of traps. That give rise to different conduction processes like trap assisted tunneling and recombination [4,6] which affect the current.

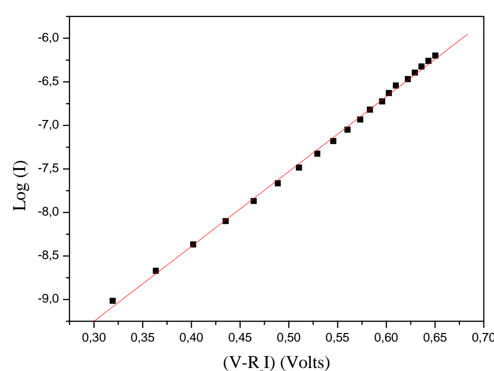

Fig. 5. Log (I) versus (V-R_sI) plot.

Values of saturation current I_s and series resistance R_s are physically acceptable [9].

5 Conclusion

This study was originated by the intention of determining Schottky diode parameters when $1/C^2$-V and ln(I)-V curves present a non linear behavior. That is the case of Al/polysilicon structures. Capacitance was find to be proportionnel to $V^{1/3}$ as for gradual doping profile. L(I)-V curves are nonlinear but X-Y ones are, allowing us to determine ideality factor, series resistance and saturation current.

We know that any damage at the interface affects the I-V behavior because defects may act as recombination centers or as intermediate states for trap-assisted tunnel currents. Either one of these mechanisms raises ideality factor which we find equal to 4,9.

References:

[1] J. Y. W. Seto, “ The electrical properties of polycristalline silicon films”, J. Appl. Phys. 46, December 1975, pp. 5247-5254.

[2] G. Baccarani, B. Ricco, and G. Spadini, “ Transport properties of polycristalline silcon films ”, J. Appl. Phys. 49, Novembre1978, pp. 5565-5570.

[3] D. P. Joshi and D. P. Bhatt, “ Theory of grain boundary recombination and carrier transport in polycristalline silicon under optical illumination”, IEEE Trans. On Electron Devices vol.37 N°1, January 1990.

[4] D. K. Schroder, “ Semiconductor material and device characterization ”, 2nd Edition, J. Wiley and sons, U.S.A., 1998.

[5] A. M. Goodman, “ Metal-semiconductor barrier height measurement by the differential capacitance method – one carrier system ”, J.Appl. Phys., vol 34 N°2, February 1963.

[6] A. Kaminski, J. J. Marchand and A. Laugier, “ I-V methods to extract junction parameters with special emphasis on low series resistance”, Solid State Electronics vol.43, 1999, pp.741-745.

[7] A. Kaminski, J. J. Marchand and A. Laugier, “ Non ideal I-V curves behavior of silicon solar cells ”, Solar Energy Materials and Solar Cells, vol. 51, 1998, pp. 221-231.

[8] M. Amrani, R. Menezla, H. Sehil, F. Raoult, H. Boudiaf, and Z. Benamara , “ Simulation of the high frequency C-V characteristics of lateral PN junctions on polysilicon films ”, Materials science and engineering B49, 1997, pp. 197-201.

[9] S. M. Sze, “ Physic of semiconductor devices ”, J. Wiley and sons, U.S.A., 1981.