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Thermal Model Conversion from Floating Point to Fixed Point – The Bridge between Theoretical Modelling and Practical Implementation

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Abstract: - This paper gives an approach to simulation model conversion from a Simulink® floating point operation to a programmable logic implementation with limited bit width and step time. A third order thermal model for IGBTs in a voltage source PWM inverter is converted to a fixed point model. Once the model is implemented into a PLD (Programmable Logic Device), the temperatures of the power switches can be observed in real time without direct measurement. As a test case parameters of a module in practical application are used.

Key-words: - Thermal, Model, Fixed, Power, Electronics

1 Introduction

Usually inverters and power modules are thermally dimensioned so that the power switches operate at the maximum allowable temperature when the inverter is at full load. The headroom in thermal dimensioning must be kept as small as possible in order to minimize manufacturing costs. However, the headroom could be further minimized with constant observation of the chip temperature.

The temperature of the chip can be either measured directly or calculated from power loss estimations. Usually the temperature is measured from the heatsink or from the baseplate, which obviously only gives long term - or average - temperature. In cyclid load or dynamic load conditions the temperature of the base plate follows the temperature of the chip with a time constant, namely thermal time constant. In the other hand, measuring the temperature directly from the chip is expensive and therefore not suitable for commercial applications [1].

The influences of the thermal time constants between the chip and the heatsink can be taken into account when deriving the temperature of the chip from power losses. This method also takes into account the differences in the thermal resistances between modules. Calculations can be done online with a microcontroller or a programmable logic [2]. An FPGA (Field Programmable Gate Array) type of PLD is the target in this study.

A basic third order thermal model [3-6] for simulating the temperature of a power switch has been presented in various conference records. It is based on power loss estimates, from which the temperature difference between the chip and the reference point is calculated. However, the model is not suitable for a programmable logic implementation without some changes. These changes include signal conversion from floating point format to fixed point format and the use of per unit values and fixed step time. Additionally, the look-up tables in the model must be defined so that the distance between two consecutive input value points is always two's exponent. This is demonstrated in chapter 3. All these changes add error to the model, but the accuracy of the original model can be kept with carefull design. The object of this research is to keep 5 % accuracy between the original model and the converted model in temperature calculations.

The original model is presented briefly in chapter 2. In chapter 3, the conversion procedure of the model is presented. Models are compared by simulations in chapter 4. Finally, some conclusions about the conversion are made in chapter 5.

The implementation itself and the verification of the original model are prospective studies. Results from those studies will be presented in future papers.

2 The Original Model

The original model calculates the temperature difference between the chip and the heatsink based on conduction and switching power losses in the chip. The output current and the heatsink temperatures are the only input variables in the model. The voltage over the switch in blocking state, the switching frequency and the gate resistance are given as parameters. In simulations these parameters can be changed if necessary. Thermal resistances and time constants are given as constants within the model, and they are dependent on the IGBT-module type. The power module used in this study is Semikron SKiiP 32nab12T1.

The switching losses are dependent on the output current, the gate resistance and the switching frequency, while the conduction losses are dependent on the output current, the voltage loss over the switch in conduction state and the chip temperature [7, 8]. The voltage loss over the switch is interpolated from a two-dimensional look-up table in which the current and the chip temperature are inputs. Another two-dimensional look-up table describes the switching energy as a function of output current and gate resistance. These tables are based on data given in the module datasheet. A block diagram of the original model is presented in Fig. 1 [2].

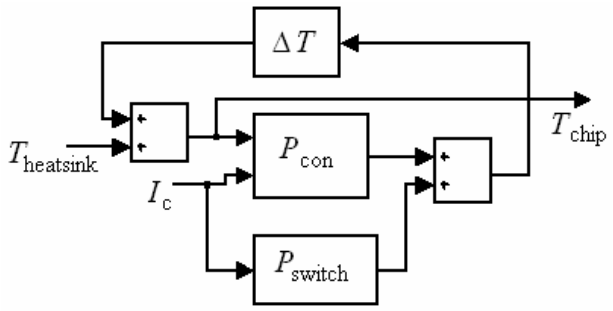

Fig.1. A block diagram of the original thermal model. The model consists of conduction power loss P_{con}, switching power loss P_{switch} and ΔT calculations [2].

The temperature difference ΔT between the chip and the reference point as a function of time can be calculated with:

$$\Delta T(t) = P(t) \cdot Z_{th}(t), \qquad (1)$$

where P(t) is the total power loss. Z_{th}(t) is the thermal impedance between the chip and the reference point as a function of time with a unity step input [4]:

$$Z_{th}(t) = R_{th}\left(1 - e^{-\frac{t}{\tau}}\right) \qquad (2)$$

where R_{th} is the thermal resistance and τ is the thermal time constant.

By transforming this to the Laplace domain and by dividing with a unity step function 1/s we get

$$Z_{th}(s) = \frac{R_{th}}{1 + s\tau_1}. \qquad (3)$$

This is used in forming the simulation model for the ΔT calculation in Simulink.

3 The Modified Model

The original thermal model must be changed so that it can be programmed with hardware description language to an FPGA. To do so, all the signals must be in fixed point format, all the values of every signal and parameter must be between zero and one, the look-up tables in the model must be changed so that the input values' distances are always two's exponent and the integrators in the ΔT calculation are discrete. The signals have a limited bit width in the fixed point format, i.e. they are quantized. Additionally, the sample time is fixed. The input signals of the modified model are discretized, converted into per unit format and quantized with so called AD-blocks. Such block is presented in Fig. 2.

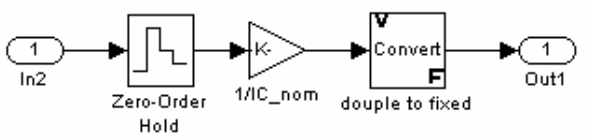

Fig. 2. An example of so called A/D-block, in which the input signals are discretized, converted into per unit format and quantized.

In this study the conduction power losses dependancy of the chip temperature was excluded to simplify the simulations. In the original model the conduction state voltage drop was given as a two-dimensional table. The temperature of the chip and the output current were inputs of the original table, but in the modified table the only input is the output current. The tables are valid with 25 °C temperature. The temperature dependancy will be included in future work with a similar procedure.

The integrators are discretized with forward Euler mapping. The integrator's response in z-domain is

$$\mathrm{H}(z) = \frac{Az^{-1}}{1 - Bz^{-1}}, \qquad (4)$$

where the coefficients A and B are dependent on the step time h, the thermal resistance R_t and it's corresponding thermal time constant τ:

$$A = \frac{h \cdot R_t}{\tau} \qquad (5)$$

$$B = 1 - \left(\frac{h}{\tau}\right). \qquad (6)$$

The integrator is damped because the coefficient B is always less than one.

The coefficients of the integrators are dependent on the step time h with equations (5) and (6); shorter the time the more resolution, i.e. bits, is required. However, in the FPGA implementation the usable bit width is limited. This leads in optimization problem with the step time. The step time must be shorter than the shortest thermal time constant, but long enough to achieve reasonable accuracy with limited bit width. The step time and the bit width are given as parameters in the model, so they can be easily changed for simulating purposes. Initial step time was decided to be 100 μs, which is two decades shorter than the shortest thermal time constant (10 ms). The optimal global bit width in the model is 16 with this step time, except for the integrators the bit width is 24. The accuracy is worse with fewer bits, but in the other hand extending the bit width from this value doesn't have significant effect on the accuracy.

The aim in the model conversion is to retain 5 % accuracy compared to the original model. The converted model is done using Simulink's Fixed Point Blockset, which ensures all the signals are in fixed point format. All input variables, parameters and constants are given in per unit (pu) format. That is all signals have a certain nominal value, which is usually the maximum value plus some additional scale. The additional scale ascertains that the values are in every case below one, even if extraordinary operation occurs in a practical application. The conduction power losses have different nominal values from the switching power losses. Also the actual ΔT calculation has a different nominal value. Because of this there is a scaling factor between power loss calculations and ΔT calculations, and also between the switching loss calculation and the summing of the losses. The modified model is presented in Fig. 3.

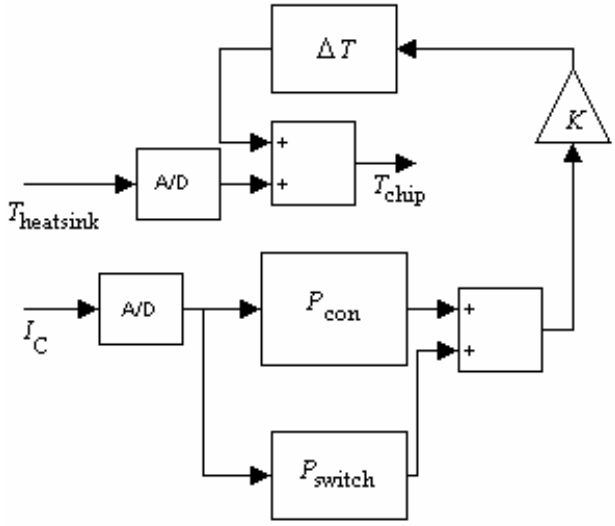

Fig. 3. The modified model. In comparison with the original model there are A/D-blocks in the input signals and a scaling factor K for switching from one nominal value to another.

There are three look-up tables in the model: IGBT conduction mode voltage drop vs. output current, IGBT switching energy vs. output current and vs. gate resistance. The tables must be modified so that the distance of two consecutive input value points is always two's exponent. The look-up table for the switching energy E_{switch} versus output current I_C is presented in Table 1 as an example. The current is an input and the switching energy is an output.

Table 1. The modified table of the IGBT switching energy E_{switch} versus output current I_C.

I_C [A]	I_C [pu.]	distance [pu.]	E_{switch} [mW]
0	0		0
		$1/2^1$	
88	1/2		25

Both the original and the modified table are plotted as a function of current in Fig. 4.

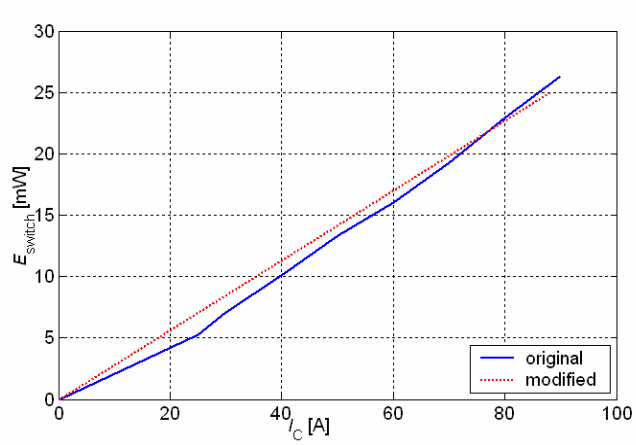

Fig. 4. The IGBT switching energy versus output current of the inverter. Solid line presents the original look-up table and dotted line presents the modified table.

As we can see from Fig. 4. the modified look-up table is inaccurate. This table needs adjustments and more data points, but it is used in simulations to determine how much of the error in the converted model comes from the look-up tables.

An improved version of the modified table is presented in Table 2 with more datapoints.

Table 2. An improved version of the modified table of the IGBT switching energy E_{switch} versus output current I_C.

I_C [A]	I_C [pu.]	distance [pu.]	E_{switch} [mW]
0	0		0
		$1/2^3$	
22	$1/2^3$		4,655
		$1/2^2$	
66	3/8		17,99

Both the original table and the improved version of the modified table are plotted in Fig. 5.

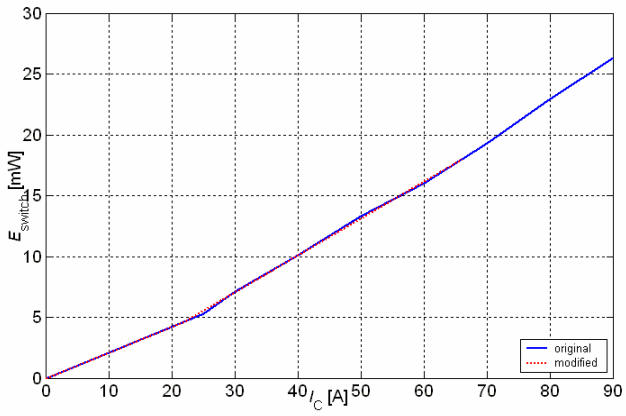

Fig.5. The IGBT switching energy versus output current of the inverter. Solid line presents the original look-up table, and dotted line presents the improved version of the modified table.

4 Simulation results

Simulations of the modified model were done using both versions of the modified look-up tables in order to find out how much of the error in the power loss calculation results from the look-up table error. The results of this simulation were compared against simulation results of the original model. In both models the temperature dependancy was omitted and the only input parameter was the output current. The current was sinusoidal with the amplitude proportional to the frequency of the current. The switching frequency was kept constant at 10 kHz. In table 3, the amplitude and the frequency of the current and the simulation results for the IGBT with both models are presented. First versions of the modified look-up tables were used in this simulation.

Table 3. Simulation results with the modified and the original thermal model. P_{sw} is the switching loss and P_{con} is the conduction state loss. First versions of the modified look-up tables were used.

		Modified		Original	
f [Hz]	I [A]	P_{sw} [W]	P_{con} [W]	P_{sw} [W]	P_{con} [W]
50	31	22,58	22,65	17,32	22,75
40	24,8	18,03	16,21	13,13	16,62
30	18,6	13,48	10,55	9,85	11,09
20	12,4	8,93	5,91	6,56	6,16
10	6,2	4,38	2,19	3,28	1,66
5	3,1	2,1	0,57	1,64	0,42

There is some difference in the simulated losses between the original model and the converted model. As an example the switching losses are presented as a function of frequency of the current in Fig. 6.

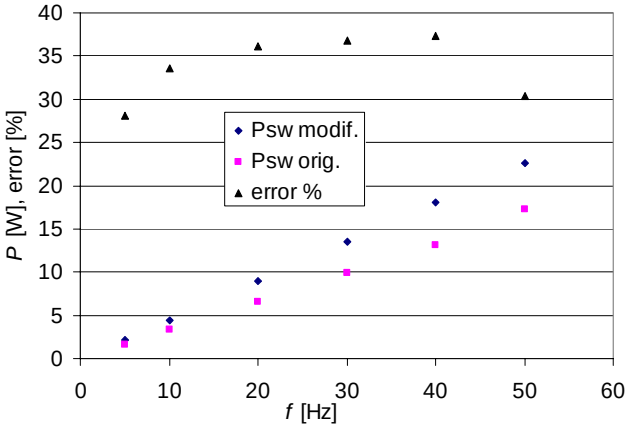

Fig. 6. Simulation results for the switching losses of the IGBT as a function of frequency of the current. The simulations are done with the original and the modified model. Black triangle reflects the error between models.

As can be seen in Fig. 6. the error between models is as much as 37 % with the first versions of the look-up tables. In table 4 the simulation results with improved versions of the modified tables are presented.

Table 4. Simulation results with the modified and the original thermal model. P_{sw} is the switching loss and P_{con} is the conduction state loss. Improved versions of the look-up tables were used.

		Modified		Original	
f [Hz]	I [A]	P_{sw} [W]	P_{con} [W]	P_{sw} [W]	P_{con} [W]
50	31	17,91	22,52	17,32	22,75
40	24,8	13,59	16,36	13,13	16,62
30	18,6	9,99	10,91	9,85	11,09
20	12,4	6,6	6,05	6,56	6,16
10	6,2	3,21	1,65	3,28	1,66
5	3,1	1,51	0,41	1,64	0,42

In this case the error is 7 % at maximum. Again, the switching power losses are presented as a function of frequency of the current in Fig. 7.

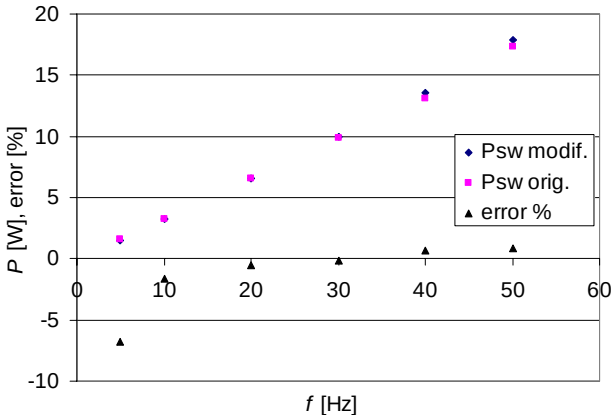

Fig. 7. Simulation results for the switching losses of the IGBT with the original and the modified model. Black triangle reflects the error between models. Improved versions of the look-up tables were used.

Also the total temperature difference ΔT between the chip and the reference point was simulated. A sinusoidal current step was fed to the model at instant 0 s. The amplitude of the current was 31 A and the frequency 50 Hz. The simulations were done with the original and the modified model. The improved versions of the modified look-up tables were used in the modified model. The results are presented in Fig.8.

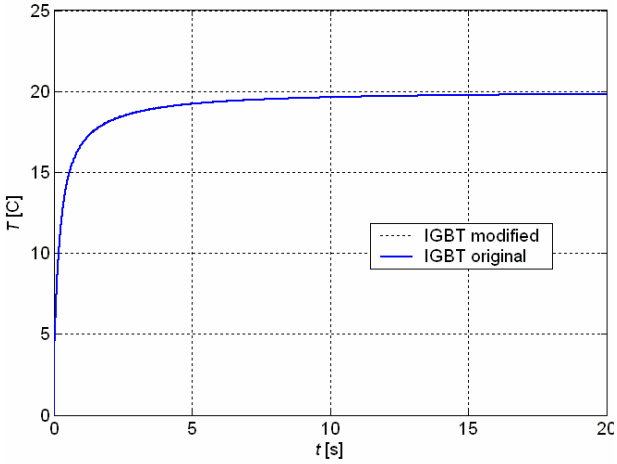

Fig.8. Simulated temperature of the IGBT when a current step is fed to the model. There is no visible difference between the original model (solid blue line) and the modified model (dotted black line).

There is almost no visible error in the IGBT temperature between the original and the modified model. The modified model gives a slightly smaller temperature rise than the original model, but the error is within specified limits (5%).

5 Conclusions

A procedure for model conversion from a Simulink® floating point operation to a programmable logic implementation with limited bit width and step time was presented in this paper. A thermal model for IGBT temperature simulations was converted and the simulation results were compared. Parameters used in the simulations were those of SKiiP 32nab12T1 power module.

It was shown with simulations that the modified model corresponds with the original model with 5 % accuracy. There is no sense to adjust the modified model anymore without verification of the original model. This will be done in future work and the results will be presented in future papers. Also the model implementation in the programmable logic will be done in future work. However, this study shows what is needed to turn from a theoretical modelling to a practical implementation.

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