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A Noise Rejection Deadbeat Control Technique for Active Power Filter

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Abstract: - Compared with power filter, active power filter has a lot of advantages and it is an efficient technique to eliminate or limit the harmonic pollution in power system. However, the control of active power filter is very complex, and the control of current loop is the key part. Traditional active power filter has direct control to instant current, which will bring noise into control and affect stability of the system. Deadbeat control is one of the feasible current control techniques since the DSP implementation of APF is concerned. This paper proposes a noise rejection dead-beat technique for active power filter, in which the resetting integrator is used as an input filter. This method is robust to parameter changes, sampling noise and periodic noise. It has been shown that it can be adopted to improve the performances of APF.

Key-Word: - Resetting integrator, Deadbeat control, Current control technique, Active power filter, Noise rejection, Sampling noise, Periodic noise.

1 Introduction

Compared with power filter, active power filter has a lot of advantages. APF can effectively restrain all of the harmonics including fractional harmonics, and can improve power factor by compensating some reactive power. Therefore, APF is an efficient technique to eliminate or limit the harmonic pollution in power system. However, the control of active power filter is very complex, and current control loop is a key element in the control structure of active power filtering systems.

Dead-beat control [1] has been accepted as a feasible current control as far as the DSP implementation of APF is concerned. The control rules of dead-beat control are deduced from the discrete model of the inverter stage. Though the simulation results for dead-beat control always seems quite promising, however, the practical realization of this control law is not that trivial. The control technique uses high gains on the errors measured at one sample to control the errors to zero ideally by the next sample. The high gains make the control very sensitive to any errors or noises in the measurement. Therefore, the input filters are commonly used to eliminate high-frequency noise and harmonic components due to modulation [2].

These filters, in fact, are not normally reckoned in the control algorithm. Therefore, the dynamic behavior of the current loop changes, which may bring the overall system instability, hence lower loop gains than the actual values are used to tradeoff between stability and performance. Similar problems also arise when there is a parameter mismatch between the modeled inverter inductance and the actual one [3].

Nowadays, trend of using resetting instigators is gaining recognition and as a witness, a number of papers have emerged in last decade. But, most of these papers have reported results regarding the nonlinear characteristics of resetting integrator [4] as a controller to generate duty ratio for PWM. Recently the results on noise immunity of linearly resetting integrator have also been described in some papers. Tung-Hai Chin, M. Nakano, and T. Hirayama in reference [5] use a resetting integrator to make accurate measurement of instantaneous values of voltage, current and power for power electronics circuits, and obtain good results in voltage and current measurement. K. Masoud and G. Ledwich in reference [6] examine the use of resetting integrator in the sampling to reduce the noise present in the samples, and combine with a high order filter to reduce the noise sensitivity of control of an inverter.

To demonstrate the results, deadbeat control with resetting integrator has been presented and applied to APF. The robustness of this controller to parameter uncertainties, random noise and periodic noise is studied and compared with conventional dead-beat control.

The organization of this paper is as follows. In the next section we will analysis the characteristics of resetting integrator. In section 3, deadbeat control with resetting integrator will be proposed and

compared with direct deadbeat control. In section 4, application of deadbeat control technique with resetting integrator in single-phase shunt active power filter has been presented with experimental results. Finally, section 5 concludes this paper.

2 Resetting Integrator

In resetting integrator the value of the integrator is reset to zero at the start of each cycle. Therefore, in resetting integrator no memory element will exist at the start of each cycle.

The frequency response of resetting integrator can derived easily and is given as follows:

$$G(j\omega) = \frac{1}{j\omega T}(1 - e^{-j\omega T}) \qquad (1)$$

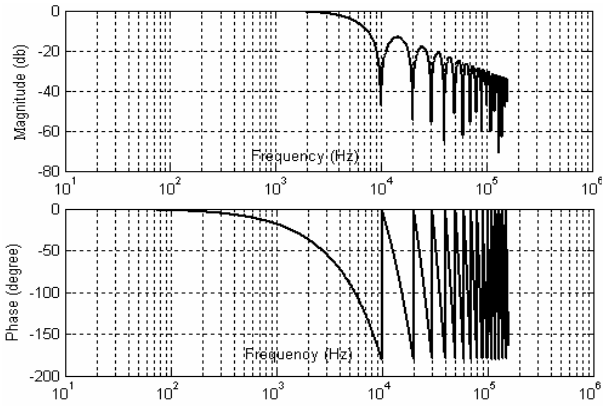


Fig. 1 Frequency response of resetting integrator

Fig. 1 shows the frequency response of resetting integrator. The magnitude response curve has been normalized to the output of systems response at zero hertz. Throughout this paper we will consider the value of T=100μs. It can be observed from these curves that, though resetting integrator has high rejection of the signals at the harmonics of switching frequency, the rejection for the signals lying in the frequency range between two harmonic frequencies is quite poor. For instance, in Fig. 1, the attenuation at 15 kHz is about 15db only, besides the roll off of the filter in almost 20db/decade. So this filter is not a very effective filter for random noise signal as has been reported in [5]. However in the presence of higher levels harmonic noise this filter is still an attractive choice. This feature becomes more essential if these noises are either periodic in nature or limited to the frequencies quite higher than switching frequency, hence resetting integrator can be quite useful in rejecting such signals.

3 Current Control Loop with Resetting Integrator

3.1 Power Stage Model

In this section, we will construct the discrete-time input continuous-time output model for PWM inverter power stage for deriving the current control law with resetting integrator. Unlike the output at the sampling instant, the average and the first harmonic current outputs of the power stage highly depend upon the modulation technique and there are several PWM techniques, such as leading edge modulation, trailing edge modulation, triangular modulation, etc. Trailing edge and leading edge only have nonlinear relationship from PWM input to the average output, while this relation is linear because of symmetry in the case of triangular modulation. Therefore, triangular wave modulated PWM is appreciated as far as the control of inverters is concerned.

Fig. 2 shows the circuit diagram of power stage of full bridge converter. The resistance of the filter inductor has been considered zero, and it has been assumed that the dc voltage and ac voltage is constant over a PWM period (quasi-static approach). Given the significant time-scale separation between the switching frequency and the source frequency, this assumption is well justified. Using triangular tracking as shown in Fig. 3, for the power stage of converter with a 2 level modulation we have following equation for the power stage in continuous time over one sampling period.

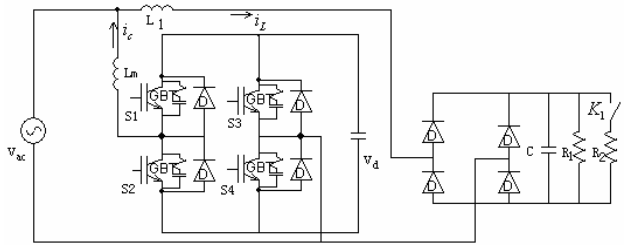


Fig. 2 Basic scheme of single phase APF

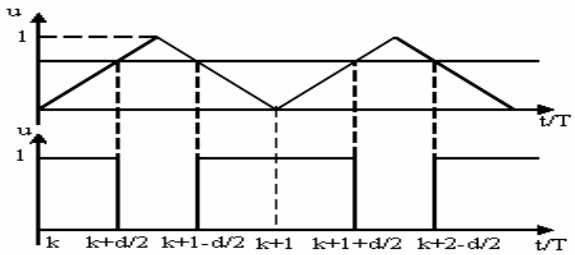


Fig. 3 Triangular tracking PWM

$$\frac{di_c}{dt} = \begin{cases} (v_d - v_{ac})/L_m & k < t/T < k + d/2 \\ -(v_d + v_{ac})/L_m & k + d/2 < t/T < k + 1 - d/2 \\ (v_d - v_{ac})/L_m & k + 1 - d/2 < t/T < k + 1 \end{cases} \qquad (2)$$

Where, i_c is the filter inductor current; v_d is the voltage of DC side; v_{ac} is the AC voltage of the connection point of APF to the system; L_m is the filter inductor; d is the duty ratio in one sample period.

The discrete time model of this system can readily

be obtain by integrating (2)over one period:

$$i_c(k+1) = i_c(k) + \frac{v_d T}{L_m}[2d(k)-1] - \frac{v_{ac}(k)T}{L_m} \quad (3)$$

The output of this system can be written in terms of average given as follows.

$$\bar{i}_c(k) = i_c(k) + \frac{2v_d(k)Td(k) - [v_d(k)+v_{ac}(k)]T}{2L_m} \quad (4)$$

3.2 Current Loop Control Using Resetting Integrator

Deadbeat control has been accepted as a feasible current control technique as far as the DSP implementation of APF is concerned. In order to track the reference current $i_c(k+1)$ is substituted by the reference signal $i_{ref}(k+1)$ in(3). Then, we can get the control law:

$$d(k+1) = \frac{[i_{ref}(k+1) - i_c(k)]L_m + [v_{ac}(k)+v_d]T}{2Tv_d} \quad (5)$$

This control law is further divided into two parts: reference current tracking and AC source rejection. After feed forward rejection of AC source, following is the control law for current tracking.

$$d(k) = \frac{L_m}{2Tv_d} err(k) \quad (6)$$

This control law forces the error to be zero at next sampling step. In general, the actual inductance of the filter inductor is known with some error. Therefore, we consider the actual inductance L_{mx} as follows,

$$L_{mx} = L_m(1-\Delta L) \quad (7)$$

Where, L_m is the nominal inductance of the inverter and ΔL is the normalized variation in L_m. In practical implementation of deadbeat control, there is an inherent delay produced by calculation. Therefore, a predictor to predict one step ahead is always used to compensate the delay.

The discrete transfer function of the close current loop is as following

$$G_{close}(Z) = \frac{1}{(1-\Delta L)Z^2 + \Delta L} \quad (8)$$

In most of the PWM application the average value of the output in each step is supposed to follow the reference signal rather than the output at the sampling instant, then the discrete transfer function of the close current loop can be written as follows.

$$G_{close}(Z) = \frac{0.5(Z+1)}{(1-\Delta L)Z^2 + \Delta L} \quad (9)$$

Since the average value of current is needed, resetting integrator can be used as a filter to get the value. Therefore, we will derive the deadbeat control law with resetting integrator as input filter. Computational delay will also be considered and compensated through the calculation. At the same time, we need to predict the peak current value of the next step. Therefore, we use a two steps predictor as follows:

$$i(k) = \bar{i}(k-2) + \frac{v_d T}{L_m} d(k-2) + \frac{v_d T}{L_m} 2d(k-1) \quad (10)$$

The discrete transfer function of the closed loop system is given below.

$$G_{close}(Z) = \frac{0.5Z(Z+1)}{(1-\Delta L)Z^3 + 0.5\Delta LZ + 0.5\Delta L} \quad (11)$$

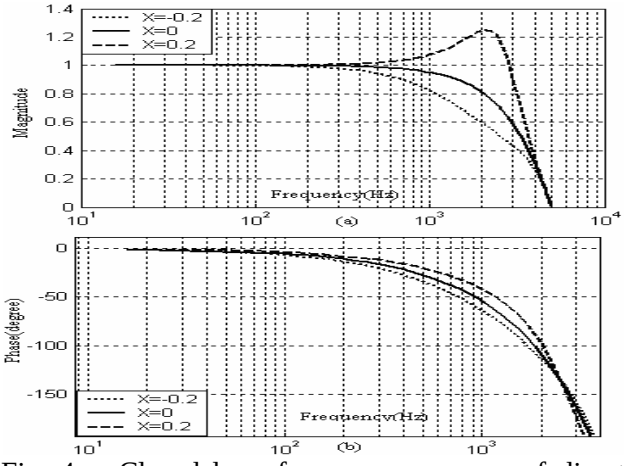


Fig. 4 Closed loop frequency response of direct deadbeat control with average current output

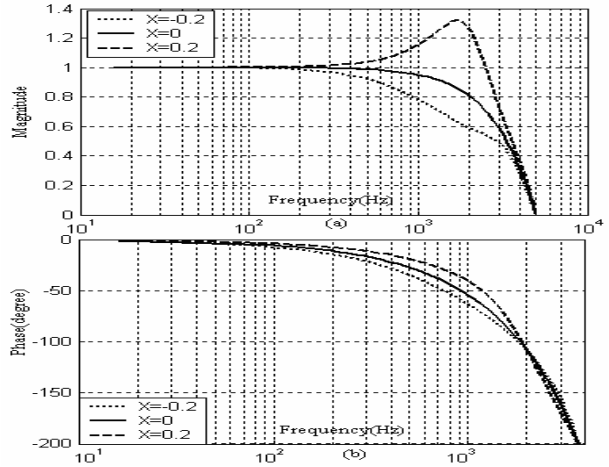


Fig. 5 Closed loop frequency response of deadbeat control with resetting integrator

3.3 Stability and Robustness Analysis

In this subsection we will present the robustness comparison of deadbeat control laws with variation in the inductance of the filter inductor in the power stage. To perform this analysis, the stability range with the variation of ΔL is estimated using Routh's stability criterion after transforming the closed-loop transfer function into appropriate form. It has been found that systems (9) and (11) show the same

stability range of 50% positive variation in ΔL and the system performances are almost the same (see Fig. 4 -Fig. 5). On the other hand, dead-beat control with resetting integrator is better in noise rejection because of the introduction of resetting integrator as input filter, which we will be proved by simulation in the next subsection.

3.4 Simulation Results

In this subsection we will present the simulation results for various control laws derived in last subsection. These simulation results are obtained by using Matlab Simulink software. The nominal value for power stage filter inductor (Fig. 2) is considered as 0.5mH. DC link voltage is taken as 450V and 220V RMS is considered on AC side. The basic setup for these simulation results is shown in Fig. 6. The reference input is set to a step of 100A to check the speed and overshoot of the closed loop systems. For studying the effect of noise, white noise source with 10 kHz high pass filter is added to the current output to simulate a signal with sampling noise. To study the effect of periodic noise, a 20 kHz, 50A peak-to-peak periodic signal is added at the feedback.

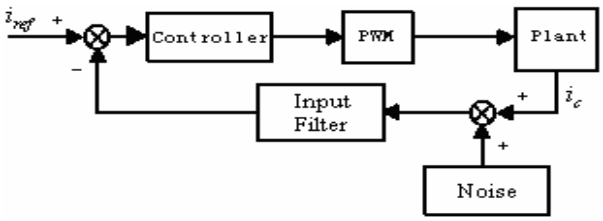


Fig. 6 The scheme of current control loop

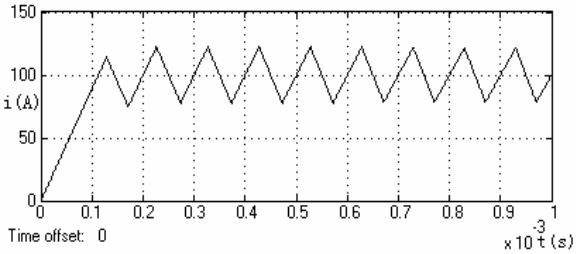


Fig. 7 Current response of dead-beat control

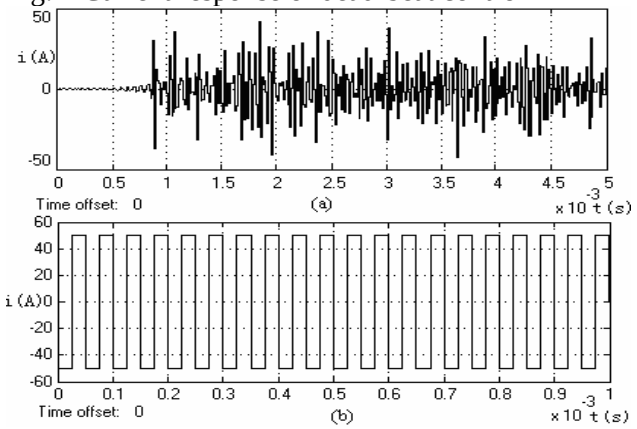


Fig. 8 Noise added to the current sampling (a. sampling noise, b. periodic noise)

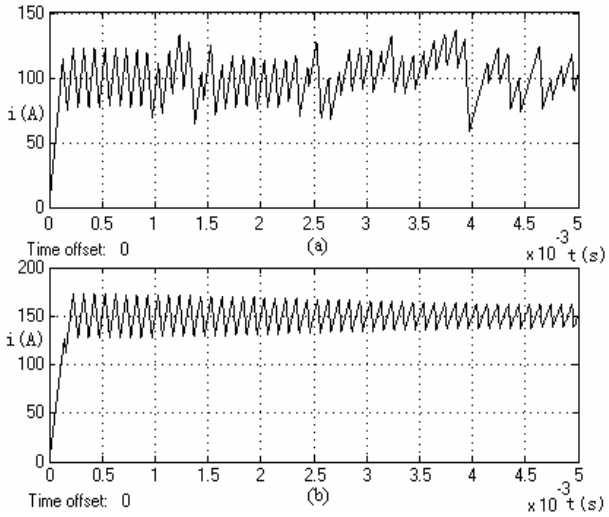


Fig. 9 Current response of direct deadbeat control with noise (a. sampling noise, b. periodic noise)

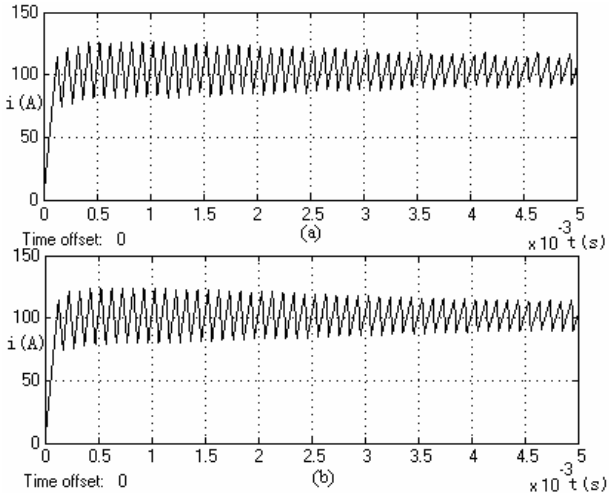


Fig. 10 Current response of dead-beat control using resetting integrator with noise (a. sampling noise, b. periodic noise)

First we present the results for direct dead-beat control. In the absence of white noise and at nominal value of main inductor (0.5mH), the deadbeat control performs quite satisfactory, as shown in Fig. 7. However in case of noisy signal (Fig. 8), the simulation results corresponding to this input are shown in Fig. 9. It can be observed that deadbeat control is highly sensitive to random noise and periodic noise.

Dead-beat control with resetting integrator is considered next. Once again, we consider the cases for random and periodic noises. The current output responses for deadbeat control with resetting integrator are shown in Fig. 10. The normal response of the system is exactly the same as deadbeat control without resetting integrator, as shown in Fig. 7. The system with resetting integrator shows less sensitivity to the noise. From simulation we conclude that this method is more robust than direct dead-beat control.

4 Applying Resetting Integrator to Shunt Single-phase APF

The basic scheme of the parallel single-phase active power filter is shown in Fig. 2. The typical distorting load, a single phase full-bridge diode rectifier load is considered. The control scheme is shown in Fig. 11.

The operation of a VSC-based single-phase APF using the deadbeat control technique with resetting integrator has been simulated in PSCAD/EMTDC [7]. The main parameters of the experimental system are presented in Table 1.

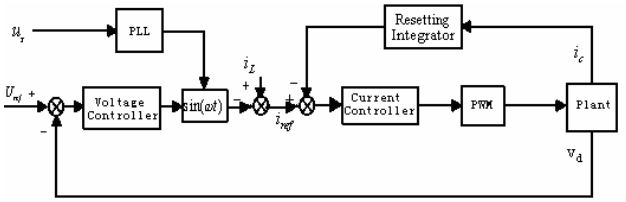


Fig. 11 Block diagram of overall control system for the active power filter

Table 1 Parameters of Experiment and Simulation

Name	Parameters
DC voltage set point	450V
Fundamental frequency	50Hz
Source voltage	220V
Fundamental load current	22A
Nominal filter inductance	0.5mH
Switching/sampling frequency	10kHz
DC capacitance	10000 μ F

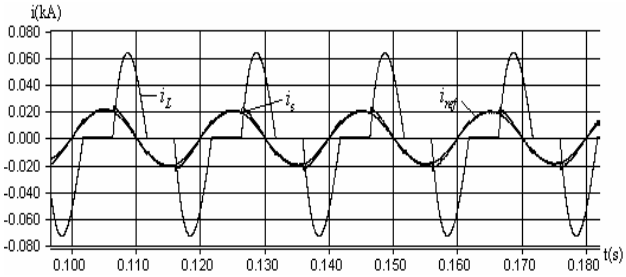


Fig. 12 The reference current, the source current and the load current while the load is fixed

Fig. 12 shows the reference current, the source current and the load current while the load is fixed. Fig. 13 shows the reference phase relationship of source voltage, fundamental current before compensation and after compensation. Fig. 13 presents that the fundamental current after compensation has the same phase as input voltage, which means that reactive power has been compensated by APF.

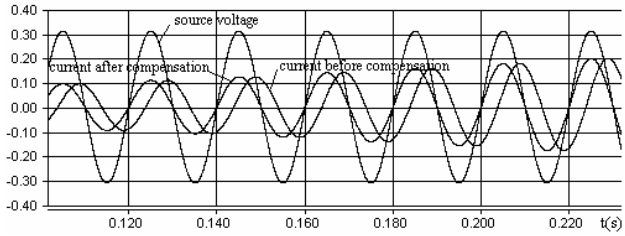


Fig. 13 The reference phase relationship of source voltage, fundamental current before compensation and after compensation

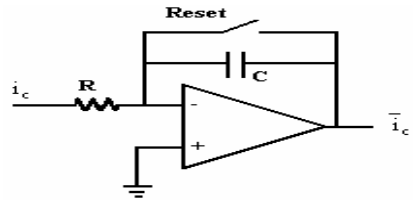


Fig. 14 The circuit of resetting integrator

Fig. 15 The dc link voltage (450V), the source current and the load current response

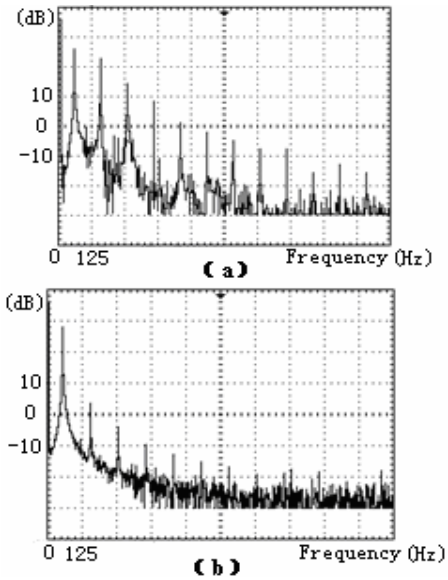


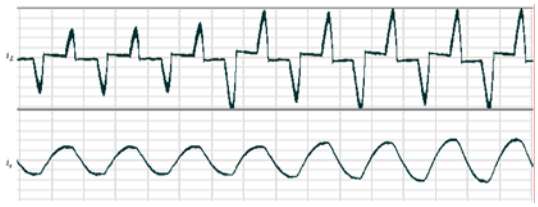
Fig. 16 The FFT results of load current (a) and source current (b)

The operation of an active power filter using the deadbeat control technique with resetting integrator has been experimentally tested on a single-phase prototype, shown in Fig. 2. The circuit of resetting integrator is shown in Fig. 14. The prototype connects in parallel to the AC 220V mains. The

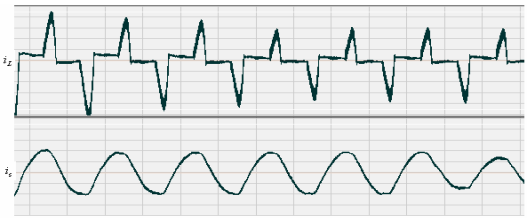
control method has been implemented on a digital signal processor (DSP) – based system using a TMS320F2812 DSP.

The system was designed to compensate the harmonic and reactive component of load current. The main parameters of the experimental setup are presented in Table 1. The nonlinear load is implemented by diode full-bridge rectifier. The capacitor of load is $8200\,\mu\mathrm{F}$, and R_1 is $15\,\Omega$. The sudden change of the load is implemented by the switch K_1 which controls the connection and disconnection of the resistor R_2.

When the switch K_1 is connected, the virtual value of the load current is about 22A. Fig. 15 shows the experimental waveforms of the load current and the source current of the active power filter system. The FFT result of load current is shown as Fig. 16(a), and the total harmonic current distortion (THD) of it is about 77%. The FFT result of source current is shown as Fig. 16(b), and the THD of it is about 7%.



(a)



(b)

Fig. 17 The load current and source current transient response while load increase (a) and decrease (b) suddenly(X: 10ms/div, Y: 10A/div)

Then we will test the situation when the load is suddenly changed. First disconnecting the switch K_1, the load current is about 12A. Then connecting the switch K_1, the load current is up to 22A suddenly. At last disconnecting the switch K_1, the load current is back to about 12A. Fig. 17(a) shows the load current and the source current when the load increases suddenly. Fig. 17(b) shows the inverse situation. From Fig. 17 we can see that the harmonics is compensated rapidly. The respond time of harmonic compensation is less than 0.2 ms, and the source current gets stable after about 30ms.

5 Conclusions

Based on the dynamic properties of resetting integrator, deadbeat control with resetting integrator has been proposed and analyzed. The simulation results show that the proposed control techniques is equally robust as direct deadbeat control and less sensitive to random noise and periodic noise in comparison to direct deadbeat control. The deadbeat control technique with resetting integrator is also applied for active power filter. The theoretical results have been verified by simulation and experiment.

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