

Computationally Efficient Simulation of Nonlinear Communication Circuits with Switches

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Abstract: - Implementation of a recent model of an internally or externally controlled ideal switch is described. General nonperiodical switching is considered. No limitations regarding the circuit structure and complexity are imposed. Simulation examples demonstrate computational efficiency.

Key-Words: - Electronics, simulation, switch, modeling, communication circuits.

1 Introduction

Electronic components (transistors, thyristors, and diodes) for convenience are often modeled as switches. Instances of such models may be found in switched capacitor (communication filters) or switched-current networks, switched power supplies, mixed signal circuits such as A/D converters [1] etc. The advantage of using ideal switches in circuit simulation is explained in [2]. To simplify, if nonideal models are used in a SPICE-like program, simulation of the resulting stiff system demands long simulation times. When switches are modeled as ideal, simulation for the switch transition is performed in one time instant, rather than as a step transition of voltages and currents. It saves simulation time without significant error in the simulation results. That will be demonstrated by an example in this paper.

Several approaches have been used for analysis of switched networks. Externally controlled switches and a restricted set of circuit elements are used in switched-capacitor (SC) networks [3, 4]. SC networks are a subset of periodically switched linear networks. Techniques to analyze such problems are described in [5] and [6], but such methods cannot be used for the circuits with internally controlled switches.

One group of methods used for the time-domain simulation of internally controlled switched networks is based on the state variable formulation. These are, however, difficult to implement in a general purpose electronic simulation program. A summary of this class of methods can be found in [7]. Recently in [8] additional results were reported suffering, however, the same deficiencies related to both possibility of implementation in general

purpose simulation program, and restriction to the set of circuit elements.

Algorithms for analysis of linear networks with internally controlled switches are described in [7] and [9]. The method in [9] enables simulation of linear systems where inconsistent initial conditions occur after switching. In networks with internally controlled switches, the Dirac impulses of voltage or current can cause changes of states of other switches in network. Algorithms that take this into consideration are described in [7] and [10]. It is shown that nonlinear storage elements (capacitors and inductors) must be represented by charges and fluxes.

New switch models were reported recently in [11]. These are, however, not efficient for implementation in systems with large number of switches commutated asynchronously.

We started our research in this field by recognizing the fact that circuits with switches, no matter how many of them are present in the circuit, and no matter what is the structure of the circuit and the nature of the rest of the elements, are nonlinear per se. Or, putting that in other words: there are no linear circuits if ideal switches are present. Nonlinear circuits are, in general, described by nonlinear equations that are unavoidably solved by iterative procedures. The switch is nonlinear as it can be, so that, the ideal switch model proposed recently [12, 13] is suitable for the time-domain simulation of networks containing externally and internally controlled switches. Our switch model is intended for use with standard SPICE-like simulator. Namely, the switch is considered as a circuit element and managed either during circuit description, or simulator's code writing, as any other element (resistor, diode etc.)

The main motivation for this research was the fact that the current versions of the switch model

implemented in SPICE are nonideal, with low R_{on} resistance and high R_{off} resistance [14]. When finite values of switched resistances are used, however, the eigenvalues in the system are extreme, and the simulation demands very long CPU times. Switch models with energy storage elements [15] can prevent such extreme eigenvalues and the simulation becomes somewhat faster.

The structure of the paper is as follows. Our nonlinear switch model is presented in Section 2. Section 3 handles inconsistent initial conditions. In Section 4, commonly used SPICE nonideal switch model is presented. The paper is concluded with a simulation example demonstrating computational efficiency of the presented ideal switch model in comparison to SPICE nonideal switch model.

2 Nonlinear Ideal Switch Model

2.1 Limitations of the Usual Ideal Switch Model

A closed switch, connected between nodes j and k is modeled as a zero-valued voltage source

$$v_j - v_k = 0 \quad (1)$$

If the switch is open, the model is equivalent to a zero-valued current source:

$$i = 0 \quad (2)$$

where i is the current through the switch flowing from the node j to the node k , as depicted in Fig. 1. Having in mind the graphical representation of (1) and (2) one readily concludes that the ideal switch is a nonlinear circuit element as it can be. Accordingly, independent of the algorithm applied for solution of the network equations related to circuits containing ideal switches, the response evaluation is performed iteratively. We here adopt the Newton/Raphson procedure that is applied in most circuit analysis programs, and our model is expressed in such a way to be easily applicable in this kind of programs. The rest of the discussion is related to equation formulation.

Modified nodal analysis (MNA) [16, 17], is well suited for automated formulation of the system of equations. For each component, a model stamp is developed. Since (1) is a voltage equation, and (2) is a current equation, two different stamps should be defined for the switch [18].

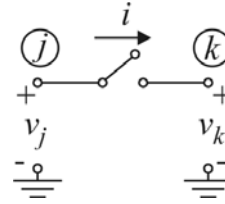


Fig.1: Ideal switch

It would seem that one could replace one stamp by another when the switch transition occurs. Unfortunately, this leads to numerical problems in a SPICE-type program, since the switch transition changes the network topology, and this is reflected in the change of the structure of the nonzero entries in the system matrix. If such models were implemented, a new reordering and pivoting in the matrix would be necessary after every switch transition.

2.2 Nonlinear Model of a Closed Switch

Our first concern is to define the switch model that would have the same structure of nonzero entries for both states [12, 13]. Let us first consider a closed switch. The problem here is that the zero entry appears on the main diagonal of the matrix. However, for circuit simulation (1) can be replaced by

$$(v_j - v_k) - r \cdot i = -r \cdot i^m \quad (3)$$

where r is a new model parameter with dimension of resistance. Superscript m denotes iteration number, and i^m denotes the value of the current obtained in the previous iteration. When convergence is reached, the current in $(m+1)$ th iteration equals that from m th iteration:

$$i = i^m \quad (4)$$

and one obtains the equation for the closed switch (1). We will use the simple circuit of Fig. 2(a) to illustrate this procedure. The iterative process of switch closing is depicted in Fig. 2(b) in i - v coordinate system. At the beginning the switch is open - that is at the point B in Fig. 2(b). When convergence is reached, the switch should be closed (point A). If the model given by (3) is used, transition from B to A is defined by iterative procedure through the intermediate solutions B', B'', B''' . These points are determined by the line A - B and another line, representing the switch model equation. Convergence is faster when lower values of r are used. Nevertheless, too low value of parameter r could lead to numerical problems. We have found the value of $10^{-5} \Omega$ enables fast convergence and is high enough to avoid numerical problems.

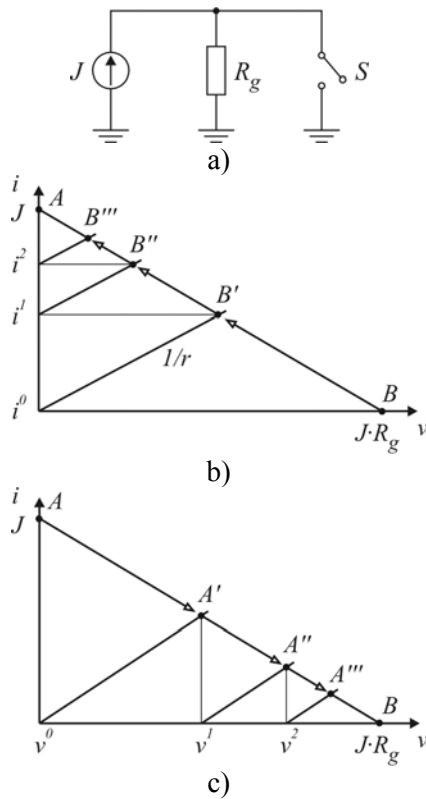


Fig. 2: a) Simple circuit with a switch; b) Iterative procedure of switch closing. The switch current in the m th iteration is i^m and $1/r$ is the slope of the line representing the switch model; c) Iterative procedure of switch opening. The switch voltage in the m th iteration is v^m and $1/R$ is the slope for the open switch.

2.3 Nonlinear Model of an Open Switch

For the open switch we introduce a new model

$$v_j - v_k - R \cdot i = v_j^m - v_k^m \quad (6)$$

where R is a model parameter with the dimension of resistance. When the convergence is reached, the voltages from $(m+1)$ th and m th iteration are equal

$$v_j = v_j^m, \quad v_k = v_k^m \quad (7)$$

and from (6) one obtains (2) which models the open switch.

The iterative procedure of switch opening is again illustrated using the circuit in Fig. 2(a). At the beginning the switch is closed, and the circuit solution is in position A . The transition from A to B goes through the points A' , A'' , A''' in Fig. 2(c). The convergence will be reached in smaller number of iterations if R is higher, but too high value could lead to numerical problems. We found the value of 10Ω convenient.

With our choice of r and R , the number of iterations necessary for convergence of nonlinear switched networks is not affected by our switch model being determined by other nonlinear devices in the network.

The stamps corresponding to the open and closed ideal switch can be found in [12, 13]. No zero main diagonal entries are generated and the structure of the nonzero entries in the stamp is the same for both switch states.

With the described model we have obtained switch transitions that change the network topology but not the structure of nonzero entries in the sparse matrix. Reordering of the matrix after switch transition is not necessary. The use of nonlinear switch model requires iteration even if the rest of the network is linear, but the convergence is reached quickly, while the algorithms for iterative solutions of nonlinear networks are built into any SPICE type program. When analyzing networks with other nonlinearities, our nonlinear switch model does not noticeably increase the number of iterations.

In the next section the most intriguing application of an ideal switch will be considered.

3 Inconsistent Initial Conditions

Inconsistent initial conditions can occur in networks with ideal switches. An example is given in Fig. 3. If the switch is in position 1, capacitor C_1 is charged to the voltage E , and C_2 has zero voltage. When switch transition occurs from 1 to 2, a Dirac impulse of current appears, and instantaneously equalizes the voltages.

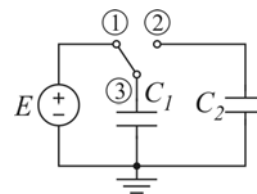


Fig. 3: Circuit with inconsistent initial conditions.

In [7, 9, 10] and [19], the problem of inconsistent initial conditions is resolved by special integration procedures. When our switch model is used, consistent network state after switch transition can be found as well. Fig. 4 shows the simulation results for the circuit in Fig. 3. The switching period is 4ms and the capacitor values are $C_1 = C_2 = 100$ nF. After the switch transition from 1 to 2 ($t = 2$ ms), some charge is instantaneously transferred through the switch, and the total amount of charge in the circuit is conserved. No special techniques are necessary for

finding consistent initial conditions after the switching.

With our model, the switching is not represented just as a replacement of one network topology by another. The switch transition is modeled through a number of iterations, where in every iteration both Kirchhoff laws are satisfied. The values of voltages and currents in the previous and new iteration are always connected by quasi-capacitor or quasi-inductor model. For that reason, a finite amount of charge is transferred from C_1 to C_2 in every iteration and charge conservation is maintained. In the dual problem, current through the inductor would be instantaneously changed, and our nonlinear ideal switch model conserves the flux in the network.

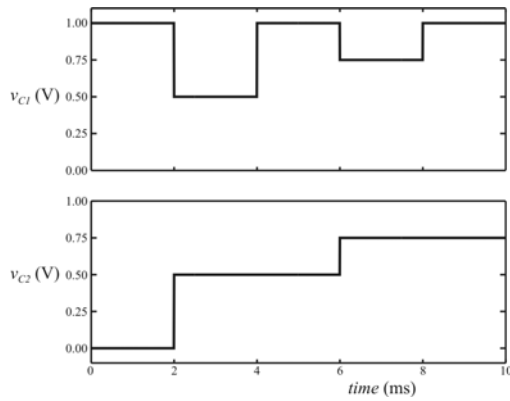


Fig. 4: Circuit with inconsistent initial conditions.

As discussed in [7] and [10], it is also important to take into account Dirac impulses that can occur at the instant of switching, which is also provided by our model [13].

4 SPICE Nonideal Switch Model [20]

SPICE does not allow for ideal switches. Accordingly, the voltage-controlled switch (Fig. 5.) is a special kind of voltage-controlled resistor. Model parameters are given in Table 1. The resistance between switch nodes (N_+ and N_-) depends on the voltage between the controlling nodes (N_{C+} and N_{C-}). The resistance varies continuously between the ON value (RON) and OFF value ($ROFF$). Resistance is calculated according to (8).

Name	Description	Units	Default
RON	“on” resistance	Ω	1.0
$ROFF$	“off” resistance	Ω	1E+6
VON	control voltage for “on” state	V	1.0
$VOFF$	control voltage for “off” state	V	0.0

Table 1: SPICE voltage controlled switch model parameters

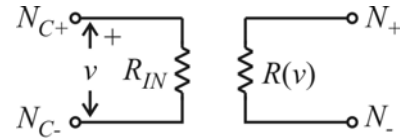


Fig. 5: SPICE voltage controlled switch model.

In the following equations:

- V_C voltage across control nodes
- L_m log-mean of resistor values $\ln(\sqrt{RON \cdot ROFF})$
- L_r log-ratio of resistor values $\ln(RON/ROFF)$
- V_m mean of control voltages $(VON + VOFF)/2$
- V_d difference of control voltages $VON - VOFF$

If $VON > VOFF$ the switch resistance R_S is

$$R_S = RON, \quad \text{for } V_C \geq VON$$

$$R_S = ROFF, \quad \text{for } V_C \leq VOFF$$

$$R_S = \exp\left(\frac{L_m + 3L_r(V_C - V_m)/(2V_d)}{-2L_r(V_C - V_m)^3/V_d^3}\right)$$

$$\text{for } VOFF < V_C < VON \quad (8)$$

Equations describing model for $VON < VOFF$ can be found in [20].

A resistance of $1/GMIN$ (GMIN is simulator parameter with default value of 10^{-12} S) is connected between controlling nodes to keep them from floating.

Making the ratio between ROFF and RON greater than 10^{12} is not recommended because of possible numerical problems. Similarly, it is not recommended to make the transition region too narrow. In the transition region the switch has gain. The narrower the region, the higher the gain and greater the potential for numerical problems.

A general property of this model may be stated as follows. Although very little time is required to evaluate switches, during transient analysis, simulator must step through the transition region with fine enough step size to get an accurate waveform. So, for many transitions, run times may be long from evaluating the other devices in the circuit as many times, as many iterations per time instant are needed.

5 Simulation Example

In order to exemplify the computational efficiency of the proposed ideal switch model, the circuit presented in Fig. 6 was simulated. This circuit presents the switched capacitor (SC) realization of the elliptic filter C05, $\theta = 42^\circ$, $p = 10\%$ [21]. Input signal presents sinusoidal signal with frequency

swept linearly with respect to the simulation time (the so called chirp signal). Envelope of the output signal obtained from a transient simulation actually presents the amplitude characteristic of the SC filter's transfer function. The simulation of this circuit was performed by the Alecsis simulator [22, 23]. Simulation results are presented in Fig. 7.

Apart from the ideal switch model, SPICE nonideal switch model was also implemented in Alecsis simulator. Table 2. gives the simulation run-times for the ideal and nonideal switch model used. It can be noted that the speed-up of 10.6 times was gained with the use of ideal switch model.

Operational amplifiers were modeled with input resistance of $10^6 \Omega$, output resistance of 10Ω and gain of 10^5 . Switches were controlled by the 500 kHz $\pm 1V$ clocks with $1\mu s$ edges. Parameters of the SPICE nonideal switch model used were: $RON=10^9 \Omega$, $ROFF=10\Omega$, $VON=0.5V$, $VOFF=-0.5V$. Default SPICE tolerances were used.

Simulation run-times [hh:mm:ss]	
Ideal switch	SPICE switch
00:23:00	04:05:01

Table 2: Simulation run-times for the SC filter (Fig. 6)

Note that no loss in the accuracy of the simulation results occurred. That was checked by comparison of the response of Fig. 7 with the original frequency domain response of the C05, $\theta = 42^\circ$, $p = 10\%$ Cauer filter.

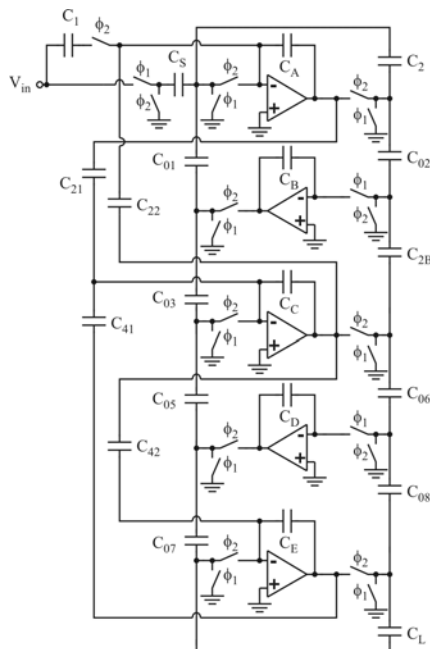


Fig. 6: Switched capacitor bilinear ladder realization of a fifth-order elliptic filter

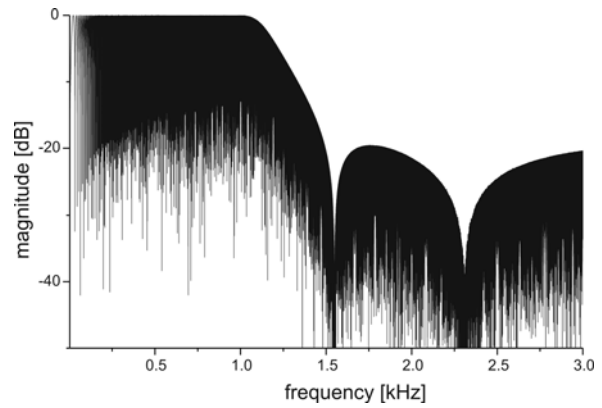


Fig. 7: Simulation results for SC filter presented in Fig. 6.

Speed-up gained with the use of ideal switch model will be explained using Fig. 8. This figure depicts time instants in which simulation results were obtained and number of system matrix factorisations needed for that solution. Since the circuit using SPICE nonideal switch is linear, there are no iterations, thus the number of factorisations is the number of time instants in which the circuit equations were solved before the solution that is within given tolerances was obtained (Fig. 8(a)) [17]. Ideal switch is nonlinear, but despite of that, it enables faster simulation because it requires less system matrix factorisations (iterations per time instant in this case), which is shown in Fig. 8(b).

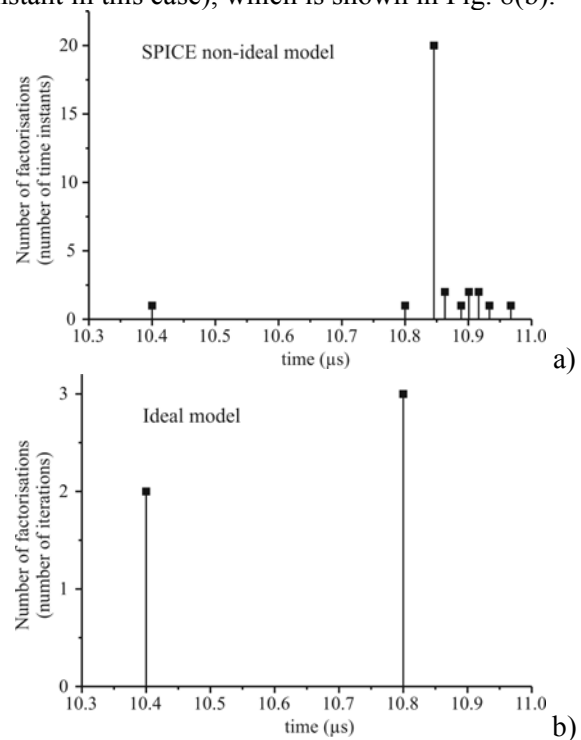


Fig. 8: Number of system matrix factorisations required for obtaining the simulation results for the circuit in Fig. 6. a) SPICE nonideal model used; b) Ideal model used.

4 Conclusion

Considering the fact that any circuit containing ideal switch is nonlinear, we developed model for the ideal switch that is applicable in a general-purpose time-domain circuit simulation program. The switch is considered as circuit element and used by routine as simple as any other circuit element. One of the important properties of the model is that it handles real situations such as managing the Dirac pulse that is encountered when switching real circuits. Here, a set of examples is presented expressing, to our opinion, the effectiveness of the model and its versatility.

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