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# Floorplanning with IR-drop consideration

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***Abstract:*** As technology advances, with supply voltage decrease and power density increase modern chips suffer more seriously IR-drop problem. In this paper IR-drop constraint is considered in floorplanning stage in order to solve problem in the early stages of physical design and shorten time to market. First a fast model with some extend of accuracy is proposed to quantify the IR-drop of a block. And then selection strategy in simulating annealing based on the model being introduced. The experiments show that the algorithm proposed in this paper can reduce the chip average IR-drop and maximum IR-drop effectively and only brings a little tradeoff in area.

***Key Words:*** VLSI IR-drop Floorplanning Simulating Annealing Wire-bond

## 1. Introduction

With the advance of VLSI manufacturing technology and market requirement, chips that integrate more functionality are operating at higher frequency and require higher current and more power. The lower supply voltage, higher power density and longer wire length deteriorate the IR-drop problem, which is due to large current passing large power network resistance. So IR-drop will be fast becoming one of dominant factors determining the chip frequency. Due to on-chip IR-drop, the actual voltage supply of standard cells on chip is less than the power-supply voltage, which results insufficient driving strength and finally lower chip frequency. Even the chip might not work normally for setup time or hold time violation, if care is not taken into clock tree delays caused by on-chip IR-drop. So in today's new interconnect-centric paradigm [1], new terms such as IR-drop, power and signal reliability have become as important, or more important, as chip area, which was a prime concern for previous technologies.

In this paper we address IR-drop problem in floorplanning stage. Floorplanning is the first stage in physical design. And the areas and relative positions of blocks are determined, and various constraints are also concerned in this stage. As a key stage floorplanning builds the framework for a feasible layout and can be used to verify the feasibility of a design. IR-drop problem has close connection with block positions and if the problem can be well solved in this early stage, it will reduce the design return time and shorten time to market.

In traditional floorplanning stage [2] chip area and wire length is optimized, but these factors are less critical in DSM era. We introduce IR-drop constraint in floorplanning to address to more and more serious timing and signal integrity problem

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caused by voltage drop. Because the exact analysis about on-chip IR-drop can only be performed after route power network. However it is unpleased to discover IR-drop violation in this late stage. So a fast and accurate model to calculate the IR-drop in early physical design stage is needed. In this paper we propose a feasible model to estimate the IR-drop of blocks in foorplan stage. With this model we propose our floorplanning appoarch based on simulating annealing algorithm. Finally the experimental results are encouraging. Through comparing with traditional floorplanner without IR-drop consideration, we obtain floorplans with significantly less maximum IR-drop and average IR-drop and with only a little area increase.

The rest of paper is organized as follows. Section 2 describes our fast IR-drop model and calculation of a floorplan IR-drop cost. Simulating annealing with IR-Drop constraint is introduced in Section 3 and the selection strategy is also described in this section. Section 5 shows our approach for floorplanning with IR-drop consideration. Finally experimental results and conclusion are stated in Section 5.

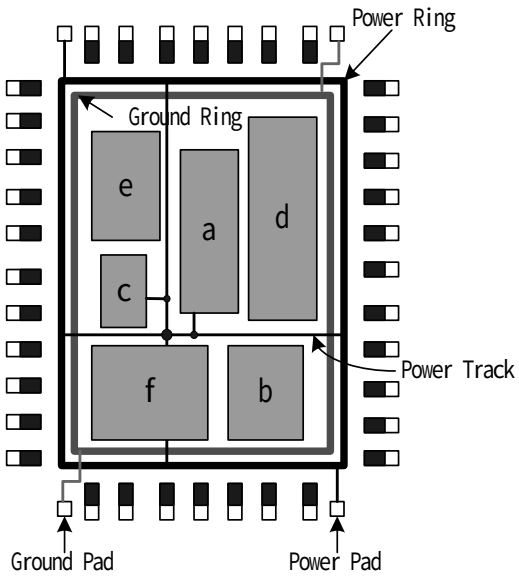



Fig.1. A wire-bond package chip with six blocks

## 2. IR-Drop Model

IR-drop is the voltage drop due to current passing through the resistance of the power distribution network. Sharp IR-drop will cause logic error because of insufficient supply of voltage. Since IR-drop has close relationship with blocks positions, we should consider the IR-drop constraint in floorplanning stage during VLSI physical design. In floorplanning stage the unit block can be a CPU core, DSP core, memory core and so on. After floorplanning the maximum IR-drop value of every block should be within its IR-drop margin by specification. For size of problem we need a fast and accurate model to quantify the IR-drop values of blocks.

For the chip with wire-bond package, there is power/ground ring surrounding the chip (Fig. 1) [3]. This power/ground ring is connected to the on-chip power network, which distributes power across whole chip. The ring is made by wide transfer line in order to reduce the voltage drop along it. Hence, IR-drop is negligible within the power/ground ring, resulting in the constant voltage boundary condition [3]. And For simplification we assume that IR-drop is only caused by resistance of inner power network is for wire-bond package.

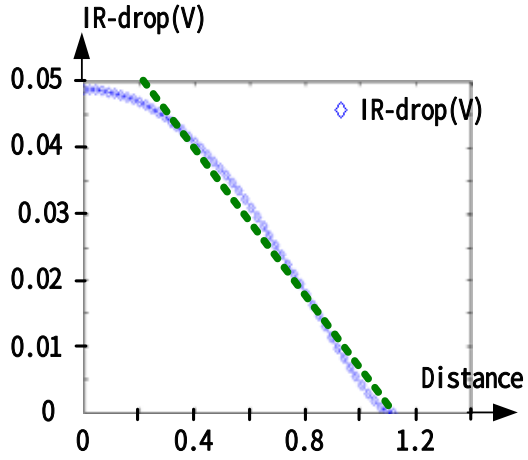



Fig.2. Y-coordinate is IR-drop and X-coordinate is the distance betweer observed point and maximal IR-drop point.

Previously, several IR-drop models have been introduced [3-5]. In [3] a simple and accurate model is introduced for wire-bond package as follows.

$$V_{IR}(x,y)=\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}E_{mn}\sin(\frac{m\pi}{a}x)\sin(\frac{n\pi}{b}y) \quad Eq.1$$

Where $V_{IR}(x,y)$ is the IR-drop of a point at $(x,y)$ on the chip, $a$ is the height of the chip and $b$ is the width, and $E_{mn}$ is a coefficient which depends on the current distribution across the chip. For a uniform current distribution, the maximum voltage drop is at the center of the chip [3].

$$V_{IR\max}(x,y) = V_{IR}(x=\frac{a}{2}, y=\frac{b}{2}) \quad Eq.2$$

If the IR-drop is calculated by using Eq.1 directly, the spending will be too large to be accepted. It is the bottleneck of the algorithm. This paper extends the application of Eq.1. The distance between the observed point $(x,y)$ and the maximum IR-drop point is used to quantify the IR-drop of point $(x,y)$. The experimental results in Fig.2 shows that the actual IR-drop of point $(x,y)$ is mostly linear with the distance between the point and the maximum IR-drop point on the chip. Hence, a possible IR-drop cost function can be written as follows.

$$Cost_{IR} = \sum_i^n d_i \quad where\ d_i = d_{\max} - d'_i \quad Eq.3$$

Where $n$ is the number of block, $d_{max}$ is the maximal distance between a point on the chip and maximal IR-drop point and $d'_i$ is the distance between block i's center point and maximal IR-drop point. Such cost function is simply, but the impact of coefficient of $E_{mn}$ is not considered. Furthermore in practice margins for IR-drop of blocks are different. Some blocks run at high frequency $f_i$, which demand a strict timing relation. A little IR-drop for these blocks will cause chip malfunction. So a weight $w_i$ variable is introduced in IR-drop cost function in order to reduce the IR-drop for the "needy" block. $w_i$ has direct proportion with frequency $f_i$ ( $f_i \uparrow \rightarrow w_i \uparrow$ ). Now the cost function is as follows.

$$Cost_{IR} = \sum_i w_i d_i \quad Eq.4$$

For block with high frequency consumes high power $p_i$ and has high power density $\rho_i$, $w_i$ can be calculated as follows.

$$w_i = \frac{\rho_i}{\sum_i \rho_i}, \quad \rho_i = \frac{p_i}{a_i} \quad Eq.5$$

Where $\rho_i$ is power density, $p_i$ is the power, $a_i$ is the area.

## 3. Simulating Annealing With IR-drop Constraint

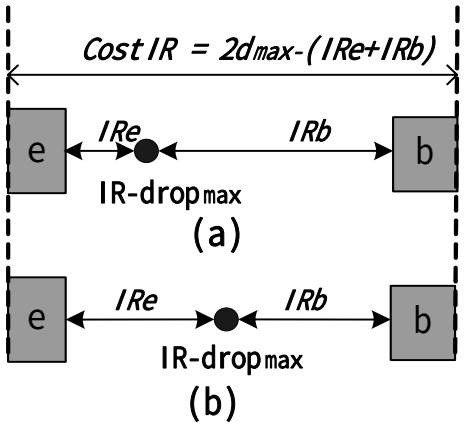



Fig.3. Even IR-drop distribution

Floorplanning with IR-drop consideration can be described as follows: Given N blocks $b_1 \ldots b_n$, where a set $b_i = \{a_i, p_i\}, 1 \le i \le n$, $a_i$ is the block area, $p_i$ is the block power, find a feasible solution such that IR-drop and chip area is optimized maximally.

During simulating annealing process the move probability is controlled when optimizing IR-drop. If the IR-drop of a block is large, the selection probability for it is large. And meanwhile the selection probability is also large for a block with small IR-drop. This means blocks with large IR-drop or small IR-drop are more probably selected for move during simulating annealing. Such selection strategy will produce more even IR-drop distribution as shown in Fig.3.

The contribution to IR-drop cost function is same for both situations in Fig.3 (a) and Fig.3 (b). However situation in Fig.3 (b) is preferred, because more even IR-drop distribution is produced than

situation in Fig.3 (a) and block e in Fig.3 (a) may suffer from logic error for large IR-drop. In practice the goal is to confirm every block of chip satisfies its IR-drop constraint and the whole chip functions normally.

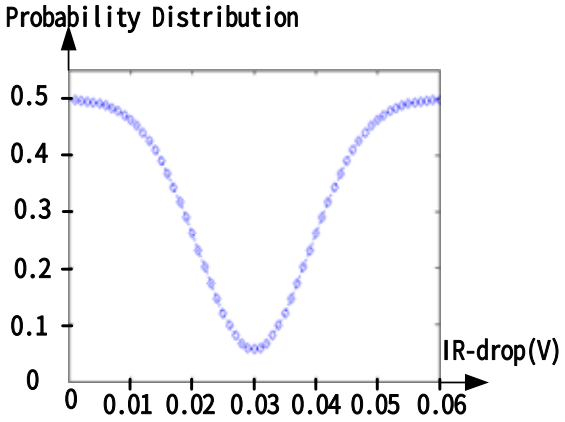


Fig.4. Selection distribution

Accordingly the selection probability distribution as shown in Fig.4 is adopted, where X-coordinate denotes IR-drop and Y-coordinate denotes the probability of certain IR-drop. The selection process is as shown in Table 1:

Table1. Selection Strategy

1. Calculate every block's IR-drop ($IR_i$);
2. Calculate the average IR-drop ($IR_{avg} = \frac{\sum_{i=0}^{N-1} IR_i}{N}$);
3. Calculate the absolute difference between $IR_{avg}$ and $IR_i$ ($Abs_i = |IR_i - IR_{avg}|$);
4. Sort the $Abs_i$ ($0 \le i \le N-1$) in set *Ary* by descending order.
5. Generate a random number *Rnd* between [0, N-1] which meets norm distribution.
6. Select the block chosen by *Ary[Rnd]* for move.

## 4.Floorplanning With IR-drop Consideration

Our flooplanning algorithm with IR-drop consideration is based on the H. Murata, et al [7] floorplan representation approach. Accordingly in our algorithm a legal floor plan is represented by a sequence pair (SP). In this paper instead of optimizing chip area or chip area and wire length in traditional floorplanning algorithm, we propose to perform IR-drop planning with respect to current foorplan be considered and in result to obtain a much better floorplan with less IR-drop constraint violation in following physical design stages.
For the cost function, we use the following equation.

$$Cost = \alpha Area + \beta WireLen + \lambda CostIR \quad Eq.6$$

Where *Area* is the total chip area, *WireLen* is the total chip wire length and *CostIR* is the cost value of total chip IR-drop that can be calculated by before mentioned approach in section 2. The coefficients $\alpha$, $\beta$ and $\lambda$ are weighting parameters of chip area, chip wire length and IR-drop cost respectively. Users due to the importance of the optimization terms can change these coefficients.

## 5. Experiment

We have tested our approach on some MCNC building blocks benchmarks. All experiments were carried out on 2.8G-pentium-IV processor. For benchmarks without enough information on current or voltage, we randomly generate it on the basis of benchmarks with this information. In our all experiments, we only optimize total chip area and IR-drop. So the wire length weighting parameter is zero. And we set IR-drop and area weighting parameters as 0.3 and 0.7 respectively.

Talbe2-4 show the comparison results between results obtained by our approach and results obtained

by a traditional floorplanner without IR-drop consideration. In these tables, $IR_{max}$ row shows the maximal IR-drop, $IR_{ave}$ row is the average IR-drop and *Area* row is the area. The row Δ shows the improving degree that is our result subtracted from traditional floorplanner result then divided by tradional result. We can see that our approach effectively reduces maximal IR-drop and average IR-drop of a floorplan and bring a little area increase. For ami33 benchmark that contains 33 blocks, we get 81.6% maximal IR-drop decrease, 36.5% average IR-drop decrease and only 6.5% area increase. For ami49 benchmark that contains 49 blocks, we get 93.1% maximal IR-drop decrease, 56.6% average IR-drop decrease and only 5.7% area increase. For some benchmark Xerox than only contains 10 blocks, we also get some improvement in maximal IR-drop and average IR-drop with a little area increase.

In Fig. 5 shows IR-drop distributions of floorplan obtained by our approach and traditional approach without IR-drop consideration. Where the darker blocks are suffered from more serious IR-drop than other blocks. We can see the floorplan by our floorplanner has more even IR-drop distribution and less dark IR-drop blocks than floorplan obtained by a traditional floorplanner.

In conclusion, we have proposed an approach to consider IR-drop constraint in floorplanning stage. With a fast and accurate IR-drop model and certain selection strategy, our algorithm can get encouraging results quickly. With slight area increase, we obtain large reduction on maximal and average IR-drop of a floorplan.

Table 2. Ami33

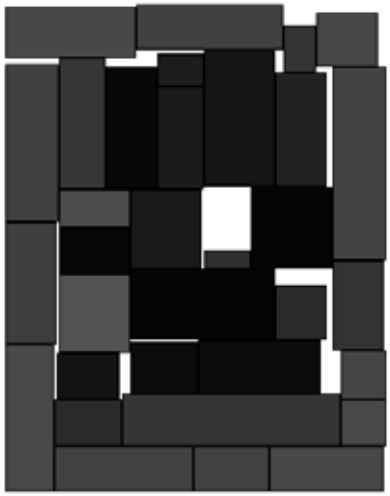
| | $IR_{max}$ | Δ % | $IR_{ave}$ | Δ % | *Area* | Δ % |
|---|---|---|---|---|---|---|
| Ours | 3.13 | -81.6 | 1.55 | -36.5 | 1.31 | 6.5 |
| Trad. | 17.04 | | 2.44 | | 1.23 | |

Table 3. Ami49

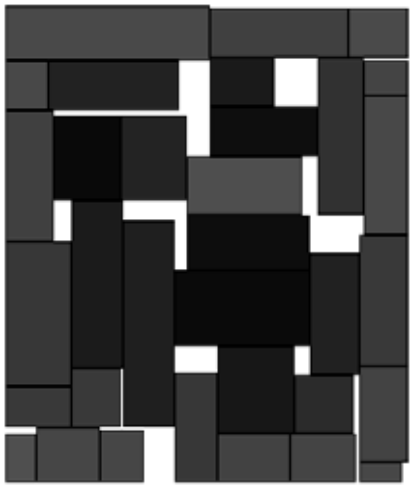
| | $IR_{max}$ | Δ % | $IR_{ave}$ | Δ % | *Area* | Δ % |
|---|---|---|---|---|---|---|
| Ours | 4.76 | -93.1 | 2.36 | -56.5 | 39.75 | 5.7 |
| Trad. | 69.36 | | 5.43 | | 37.61 | |

Table 4. Xerox

| | $IR_{max}$ | Δ % | $IR_{ave}$ | Δ % | *Area* | Δ % |
|---|---|---|---|---|---|---|
| Ours | 2.81 | -16.1 | 0.97 | -2.1 | 21.48 | 2.9 |
| Trad. | 3.35 | | 0.95 | | 20.87 | |



(a) Ami33 result by traditional floorplanner



(b) Ami33 result by ours

Fig. 5. Aim33 floorplan obtained by traditional floorplanner and ours. Dark color blocks suffering from large IR-drop.

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