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Numerical Simulation of Random Dopant Fluctuation in Sub-65 nm Metal-Oxide-Semiconductor Field Effect Transistors

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Abstract: - As the gate length of MOSFET devices shrinks down below 100 nm, the fluctuation of major devices parameter, namely, threshold voltage (V_{TH}), subthreshold swing, drain current (I_D) and subthreshold leakage current due to influences of processes variations becomes a serious problem. Random dopant fluctuation is one of the problems. In this work, we numerically examine the fluctuation effects of random dopant on the threshold voltage and drain current variation in deep sub-micron semiconductor devices. In the numerical simulation of the threshold voltage variation, the drift-diffusion and density gradient models are considered to describe transport phenomena with quantum effects of devices. Random dopant induces drain current and threshold voltage lowering. The fluctuation of device characteristics caused by random dopant cannot be neglected. From the results, the thin channel of DG-MOSFET might prevent V_{TH} fluctuation caused by random dopant effects. Also, comparison of two- and three-dimensional simulation is presented. Three-dimensional simulation must be considered while simulating semiconductor devices in sub-50 nm regime so as to obtain a reliable result. From the fabrication point of view, we concluded that the random dopant fluctuation of device characteristics could be controlled in the design of DG-MOSFET with thin channel thickness.

Key-Words: - random dopant fluctuation, double-gate MOSFET, nanoscale device, drift-diffusion model, density-gradient method, three-dimensional simulation.

1 Introduction

Short channel effects, subthreshold slope, current-voltage characteristics and quantum effects, are the most interesting topics in the recent years while semiconductor devices are scaled into deep sub-micron dimensions [1-5]. Among the characteristics of devices, the threshold voltage (V_{TH}) and the drain current (I_D) are the two crucial one, which determine the operation of a device. The former one corresponds to the onset of inversion channel build-up, which means the starting of the devices operation. Threshold voltage not only determines the operation characteristics of metal-oxide-semiconductor field-effect transistor (MOSFET) but also judge the function of designed circuit. The later one, which is the drain current of a device, is the flow of electrons from the source to the drain is controlled by the voltage applied to the gate. Drain current determines the signal presented by the devices. As the scale of integrated circuit moving form VLSI to ULSI, large current is necessary to reduce the RC delay.

Nowadays, the dimension of semiconductor devices, such as MOSFETs is in the regime of nanometer. The fluctuation of major devices parameter, namely, V_{TH}, subthreshold swing, I_D and subthreshold leakage current due to influences of processes variations becomes a serious problem [6]. Random dopant fluctuation is one of the problems [6-10]. Therefore, as scaling size of devices and developing of new transistor architecture, the random dopant fluctuation may be required to avoid so as improving the device integration. Computer-aided design (CAD) for semiconductors [11-24]

provides software driven approach to explore influence of process variations on characteristics of devices. Also, computer-aided simulation needs much less time than experimental tests. Therefore, the random dopant influence on operating characteristics of devices is studied by numerical simulation in this work. With the continuous decrease of device dimensions, narrow width effect, which is neglected in two-dimensional simulation, must be considered. That is, three-dimensional simulation should be taken into account while a nanoscale device is simulating. However, three-dimensional simulation of semiconductor devices involves sophisticated computation and complicate physical model problem. Hence, a decoupled and iterative method is presented for three-dimensional simulation of nanoscale semiconductor devices. The influence of random dopant fluctuation on V_{TH} and I_D for single-gate (MOSFET), silicon-on-insulator (SOI) and double-gate MOSFET (DG-MOSFET) with different channel lengths (L_G) and silicon film thickness (T_{si}) are investigated numerically. The remaining content of this study is given as follows. Sec. 2 briefly explains the simulation models and the computational method. Sec. 3 shows the simulation results and discussion. Sec. 4 draws the conclusion.

2 Quantum Transport Models

According to related studies, quantum effects must be considered in simulation for semiconductor devices, which channel length are smaller than 0.1 μ m. Theoretically speaking, the Schrödinger equation coupled with classical model is the most accurate way to solve the carrier concentration, but it is not suitable for engineering applications. This is not only because it is computationally expensive but also because it is difficult to model the multi-dimensional cases. Quantum correction models are developed as the alternatives of the Schrödinger equation. This kind of models produce a similar results to quantum mechanically calculated one but require only about the same computation cost as that of the classical calculation. Among quantum correction models, the density-gradient model is considered a better approximation than that of the Hänsch, van Dort model, and MLDA models [11-24]. Therefore, the drift-diffusion and density gradient models are considered to describe transport phenomena with quantum effects of devices. The three governing equations of drift-diffusion model are listed as follows.

$$\nabla\varepsilon\cdot\nabla\phi = -q\left(p - n + N_D - N_A\right), \tag{1}$$

$$q\frac{\partial n}{\partial t} - \nabla\cdot\mathbf{J_n} = -qR, \tag{2}$$

$$q\frac{\partial p}{\partial t} + \nabla\cdot\mathbf{J_p} = -qR, \tag{3}$$

where ε is the electrical permittivity, q is the elementary electronic charge, n and p are the electron and hole densities, and N_D and N_A are the number of ionized donors and acceptors, respectively. $\mathbf{J}_n = -qn\mu_n\nabla\phi_n$ and $\mathbf{J}_p = -qp\mu_p\nabla\phi_p$ are the electron and hole current densities. μ_n and μ_p are the electron and hole mobility, and ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials, respectively. $\phi_n = -\nabla\phi - \nabla n\left(kT/\mu_n\right)$ and $\phi_p = -\nabla\phi + \nabla p\left(kT/\mu_n\right)$. R is the generation-recombination term.

Density-gradient theory is a generalization of the standard drift-diffusion transport description of electrons and holes in a semiconductor that incorporates lowest-order quantum effects. This is achieved by making the equations of state of the electron and hole gases depend not only on the gas densities but also on the gradients of their densities. The density-gradient model presented by Ancona [14-16] is an approximation approach to the quantum mechanical correction of the macroscopic electron transport equation. It is a macroscopic (continuum) approach to the quantum confinement problem. In the early 1980s, Ancona and his coworkers generalized the equation of state of the electron gas to include density-gradient dependence. Later it was extended to describe the quantum-mechanical behavior of electrons exhibited in strong inversion layers. Recently, Ancona and his research team made further progress on this physically based approach and pointed out that the density-gradient approximation is an effective fool for engineering-oriented analyses of electronic devices in which quantum confinement and tunneling phenomena are significant [16]. According to DG method, an additional potential Λ is introduced into the classical density formula, which reads: $n = N_C\exp\left(\left(E_F - E_C - \Lambda\right)/k_BT\right)$, where N_C is the

conduction band density of states, E_C is the conduction band energy, and E_F is the electron Fermi energy.Different approximation of Λ is employed to obtained the adjust potential [14-16, 19-20, 23]. In this study, Λ is given as

$$\Lambda = \frac{\gamma\hbar^2\beta}{12m}\left[\nabla^2(\phi+\Lambda)-\frac{\beta}{2}(\nabla\phi+\nabla\Lambda)^2\right]. \quad (4)$$

where γ and β are factors. In equilibrium, $n \propto \exp[-\beta(\phi+\Lambda)]$. Therefore, the drift-diffusion and density-gradient systematic equations are Eqs. (1), (2), (3) and (4). According to box discretization [25-29], each PDE is discretized as

$$\sum_{j\neq i}\sigma_{ij}\cdot\varepsilon(\phi_i-\phi_j)+\Omega_i\cdot(p_i-n_i+N_{Ai}-N_{Di})=0, \quad (5)$$

$$\sum_{j\neq i}\sigma_{ij}\cdot\mu_n(n_i B(\phi_i-\phi_j)-n_j B(\phi_j-\phi_i))+\Omega_i\cdot\left(R_i+\frac{\partial n_i}{\partial t}\right)=0, \quad (6)$$

$$\sum_{j\neq i}\sigma_{ij}\cdot\mu_p(p_j B(\phi_j-\phi_i)-p_i B(\phi_i-\phi_j))+\Omega_i\cdot\left(R_i+\frac{\partial p_i}{\partial t}\right)=0, \quad (7)$$

$$\Omega_i\Lambda_i=\frac{\gamma\hbar^2}{6m_i}\sum_j\sigma_{ij}\left(1-\exp\left[\frac{\phi_i+\Lambda_i}{2k_BT}-\frac{\phi_j+\Lambda_j}{2k_BT}\right]\right), \quad (8)$$

where $\sigma_{ij}=d_{ij}/l_{ij}$ in two-dimensional space and $\sigma_{ij}=D_{ij}/l_{ij}$ in three-dimensional space. l_{ij} is the distance between *i* and *j*. In two-dimensional space, Ω_i is the area of the box face between *i* and *j*. Ω_i is the volume of the box face between *i* and *j* in three-dimensional space. After the systematic equation is discretized in spatial domain, the Backward Euler method is employed to time matching. The discrete scheme is solved by finite difference method. Then, the solving procedure is described briefly as follows:

Step 1. Choose the stop criteria, mesh, output variables and simulated devices.

Step 2. Solve the Poisson equation until it converges.

Step 3. After the Poisson equation is convergent, density-gradient equation is solved by substituting the classical potential obtained by the last step into it.

Step 4. Solve the continuity equations iteratively by substituting the solutions obtained by the last two steps into them.

Step 5. Check the whole system converges or not.

Step 6. If the whole system converges, then stop computing.

Step 7 Otherwise, go back to Step 2 and go through Steps 2~6, until the whole system equations converge.

After the drain current is obtained, the threshold voltage is determined. The definition of threshold voltage employed in this study is the Gm maximum method. The method firstly find out the gate voltage at the maximum of Gm, then make a tangent line of the drain current – gate voltage (I_D-V_G) curve at the gate voltage. Finally, extrapolated intercept of the tangent line to the V_G-axis; the extrapolation is defined as V_{TH}.

3 Simulated Results and Discussion

Firstly, the necessity of three-dimensinal simulation is discussed. Simulation of Double-gate metal-oxide-semiconductor field effect transistor (DG-MOSFET) is considered as an example. The simulated scenario is given as follows: the channel length is equal to 40, 50 and 60 nm; the uniform channel doping is 1×10^{18} cm^{-3} by boron; source and drain are doped by arsenic uniformly with a concentration 1×10^{20} cm^{-3}; the oxide thickness is 2, 3, 4 nm and the thickness of silicon film is 10, 20 and 40 nm. The simulated device is shown in Fig.1. Furthermore, the channel widths simulated are 10, 20, 40 nm and 1 μm. The drain voltage and the gate voltage are given as 1.0 V. In traditional single-gate MOSFET, channel formed at the interface between oxide and silicon while V_G is larger than V_{TH}. Therefore, current transports just like a surface flow in the channel. However, the result of 3D simulation shows a different phenomenon, i.e., current flow concentrates at the corner of silicon fin. The interesting results obtained by three-dimensional simulation give us an insight into the operational characteristics of semiconductor devices so as to

improve the performance of devices of design new structures.

Figure 1 illustrates the I_D - V_G curves with(3D)/without(2D) considering channel width effects. The curves show the different results due to different channel width. According to the curves, current density increases as channel width decreases. In order to compare the discrepancies of I_D between the different channel widths, ΔI_D is defined as

$$\Delta I_D=(I_{D\_W}-I_{D\_40})/I_{D\_40}*100\%. \quad (9)$$

I_{D}_W is the drain current density of W = 10 and 20 nm, where I_{D}_10 and I_{D}_20 denote drain current density of W = 10 and 20nm, respectively. I_{D}_40 is drain current density of W = 40nm. From Fig.2, as the difference of channel width becomes larger; the discrepancy of drain current density becomes larger. As the result, a 10 nm decrease of channel width might induce a 20 % increase of drain current density. Therefore, channel width effects must be considered while a nanoscale semiconductor device is simulated, i.e., a three-dimensional simulation is necessary.

Another important variable of semiconductor devices is threshold voltage (V_{TH}), which determines the turn-on/turn-off characteristics. Since the shapes of I_D-V_G curves of different channel width are different, the V_{TH} is different. In two-dimensional simulation, $V_{TH} \fallingdotseq 0.2$ V, which is not high enough for a reliable device. On the other hand, $V_{TH} \fallingdotseq 0.4$ V, which presents a good turn-on/turn-off characteristics, in three-dimensional simulation. Therefore, if we draw a conclusion from the result of two-dimensional simulation, we may consider the design of device is failed.

In addition, different T_{ox}, T_{si} and L_G of DG-MOSFET are simulated in two- and three-dimensional space to examine the results and illustrated in Figs. 3, 4 and 5, respectively. According to the figures, as T_{ox} and L_G decrease, I_D increases. Performance of devices is improved with shrinking of their scales. Although I_D decreases with T_{si} decreases, the SCE (the decrease of the device V_{TH} as the channel length) is controlled by thin T_{si}. From Fig. 4, if T_{si} is thick, the device is failed because of low V_{TH}. Consequently, while T_{ox}, W and L_G are scaling down, T_{si} must shrink with an adequate ratio to obtain the optimal design of devices. Furthermore, results of 2D simulation are overestimated. The reason might bring about considering the width of channel. Because when the width is considered, the scattering of electron and hole increase.

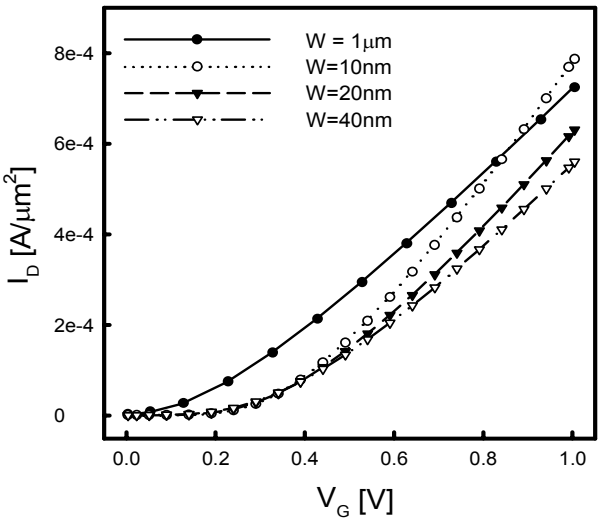


Figure 1. Simulated I_D-V_G curves of DG-MOSFETs with different width.

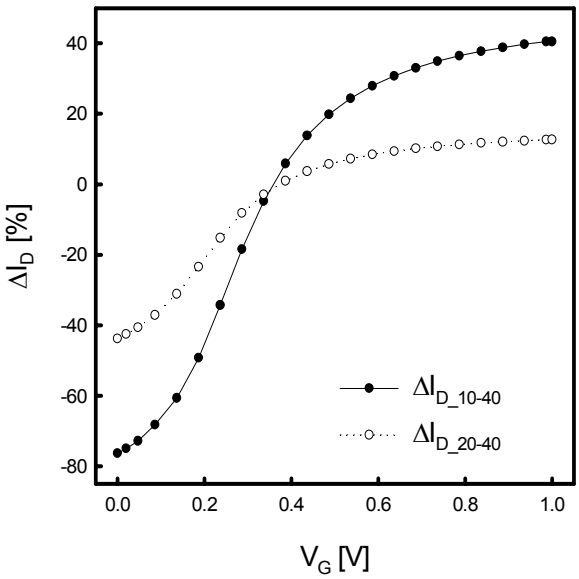


Figure 2. Discrepancies of drain current density between different channel widths, where W = 40 nm is considered as the comparing base. (L_G= 40 nm, T_{ox} =3 nm, T_{si} =10 nm)

Next, we examine the fluctuation effects of random dopant on the threshold voltage and drain current variation in single-gate MOSFET, SOI and DG-MOSFETs, which are illustrated in Fig. 6. In the numerical studies, the simulated oxide thickness (T_{ox}) is 3 nm, channel length (L_G) are 35, 40 and 50

nm, Si film thickness (T_{si}) are 10 and 20 nm and source/drain doping concentration is 1×10^{20} cm^{-3}. The uniform channel doping concentration (N_A) is 1×10^{18} cm^{-3}. Random number is generated from 0.01 to 50 uniformly and the cases are simulated by ISE-DESSIS ver. 10.0. Figures 7~9 illustrate simulated results of I_D-V_G curves for MOSFETS, SOI and DG-MOSFET with uniform and random dopant concentration. Figures 10 compares drain current of three kinds of devices with L_G = 35. V_{TH} fluctuation for devices with different L_G and T_{si} are shown in Fig. 11.

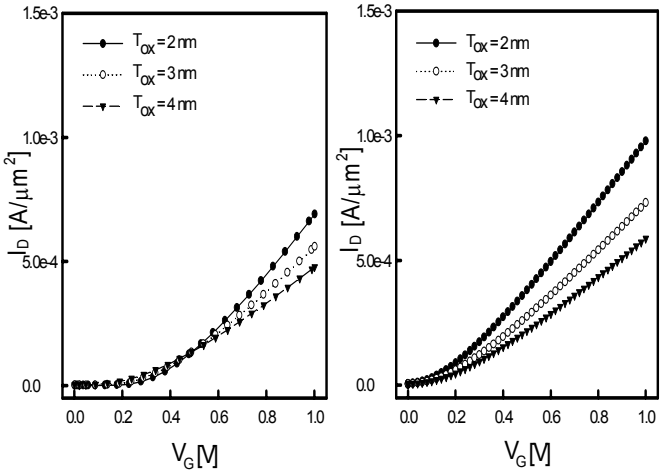


Figure 3. Simulated I_D-V_G curves of DG-MOSFETs with Tox = 2, 3 and 4 nm by (a) 3D and (b) 2D simulation. (L_G= 40 nm, W = 40 nm, T_{si} =10 nm)

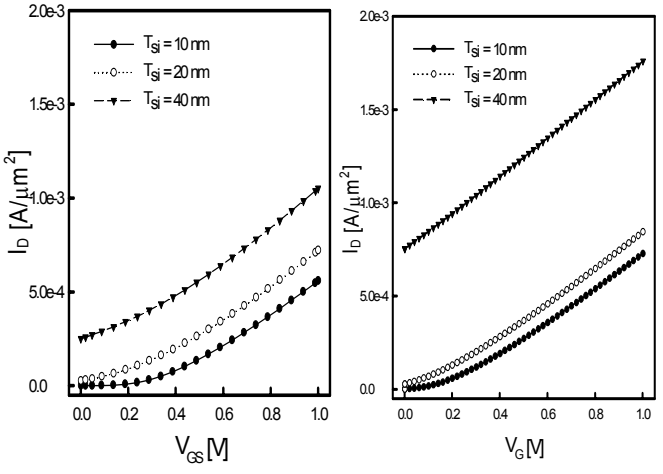


Figure 4. Simulated I_D-V_G curves of DG-MOSFETs with T_{si} = 10, 20 and 40 nm by (a) 3D and (b) 2D simulation. (L_G= 40 nm, W = 40 nm, T_{ox} = 3 nm)

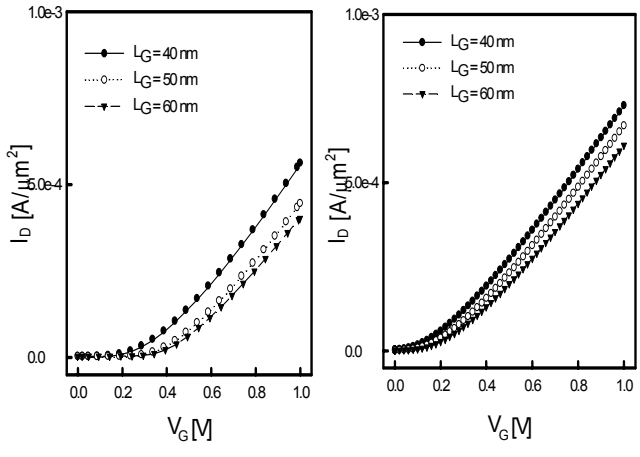


Figure 5. Simulated I_D-V_G curves of DG-MOSFETs with L_G = 40, 50 and 60 nm by (a) 3D and (b) 2D simulation. (T_{ox} = 3 nm, W = 40 nm, T_{si} = 10 nm)

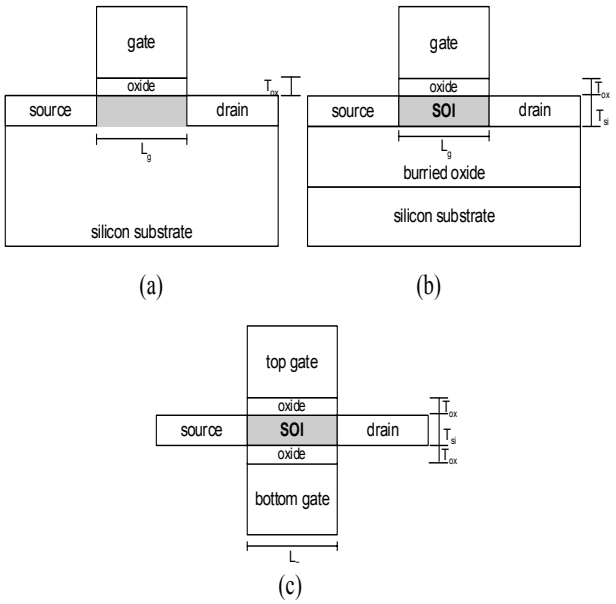


Figure 6. Simulated devices (a) single-gate MOSFET; (b) SOI and (c) double-gate MOSFET, the gray region is the random dopant region.

Figures 7~9 report the I_D-V_G curves of devices with uniform and random dopant (UD and RD). From the figures, random dopant induces drain current lowering and threshold voltage enlarging. The reductions of I_D of devices are given as follows. MOSFET is about 10%. SOI with T_{si} = 10 nm is about 9%~12% and SOI with T_{si} = 20nm is about 7%~11%. DG-MOSFET with T_{si} = 10 nm is about 3%~5% and DG-MOSFET with T_{si} = 20 nm is about

2%~5%. While channel length is longer, the variation caused by random dopant becomes larger. The smallest influence of random dopant, which is 2%~5%, is the DG-MOSFET with T_{ox}=3nm, T_{si}=10nm, L_G=35nm. I_D reduction rate caused by random dopant of single-gate MOSFET almost keeps in the same percentage in all size of devices. Among MOSFET, SOI and DG-MOSFET, the influence of random dopant fluctuation on DG-MOSFET is the smallest, especially in a thin channel thickness device.

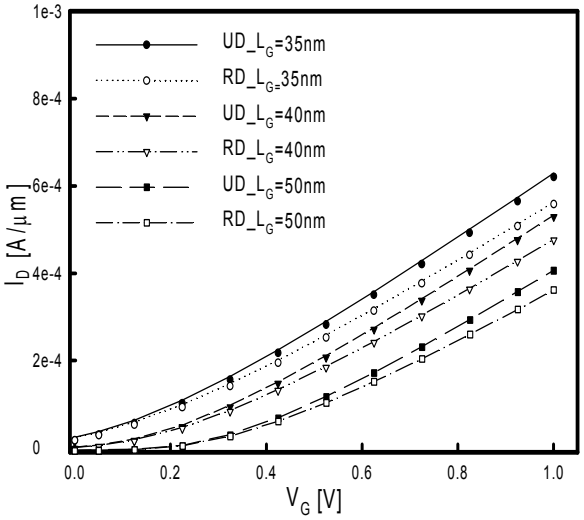
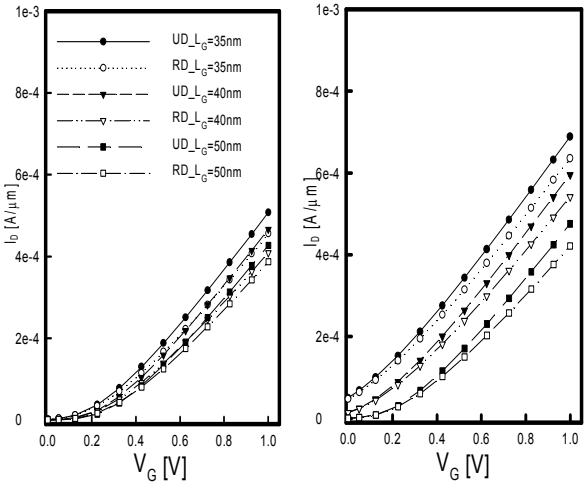
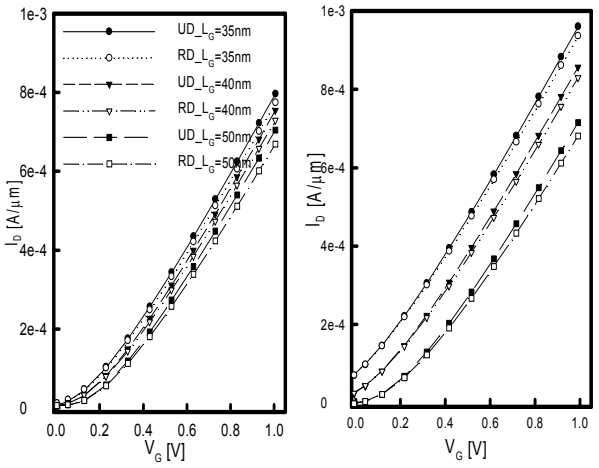


Figure 7. Simulated uniform and random dopant ID-V_G curves for MOSFETs with T_{ox}=3nm, N_a=10^{18} cm^{-3}, L_G=50nm for V_G = 1.0V, V_D=1.0V.



(a) (b)

Figure 8. Simulated uniform and random dopant I_D-V_G curves for SOI with T_{ox}=3nm, Na=10^{18} cm^{-3}, L_G=50nm, V_G = 1.0V, V_D=1.0V for (a) T_{si}=10nm and (b) T_{si}=20nm.



(a) (b)

Figure 9. Simulated uniform and random dopant I_D-V_G curves for DG-MOSFETs with T_{ox}=3nm, N_a=10^{18} cm^{-3}, L_G=50nm, V_G = 1.0V, V_D=1.0V for (a) T_{si}=10nm and (b) T_{si}=20nm.

From Fig.10, DG-MOSFET with T_{si} = 10 nm presents the best performance of all because the I_D is the largest and the I_D-V_G curve presents an acceptable V_{TH}. I_D of the SOI with T_{si} = 10 nm is as small as it of MOSFET. However, V_{TH} of the MOSFET is the largest one, which means that the MOSFET presents the worst performance among the simulated devices. That is, the MOSFET needs a large applied voltage to turn on, but induces a small drain current. SOI and DG-MOSFET present better operational properties than MOSFET does. For both SOI and DG-MOSFET, if T_{si} is thicker, I_D becomes larger and V_{TH} becomes smaller. On the other hand, if T_{si} becomes thinner, I_D becomes smaller and V_{TH} is larger. According to Figs. 10 and 11, we find that I_D becomes larger, but V_{TH} becomes smaller while L_G becomes smaller. V_{TH} drops because of the short channel effects. As L_G = 35 nm, I_D of SOI with T_{si} = 10 nm becomes the smallest one. Since V_{TH} of the MOSFET and DG-MOSFET and SOI with T_{si} = 20 nm are too small so that they cannot present good on/off operation in a circuit. Besides, V_{TH} of them varies largely, which is impossible to be used in a designed circuit. Among the devices, DG-MOSFET and SOI with thin channel thickness are promising for CMOS technology at channel length below 50 nm. The results agree with our previous results [24], that is, V_{TH} can be controlled by the channel thickness of DG-MOSFET and SOI devices.

Threshold voltage variation with channel length and dopant fluctuation is illustrated in Fig. 11. Since random dopant induces drain current lowering,

threshold voltage enlarges when random dopant is considered. The increment of V_{TH} caused by random dopant is about 0.01 V for SOI and MOSFET. V_{TH} variation of DG-MOSFET is only about 0.005 V. We may draw a brief conclusion herein, i.e., the operational properties of DG-MOSFET with a thin channel thickness are not sensitive to random dopant effects.

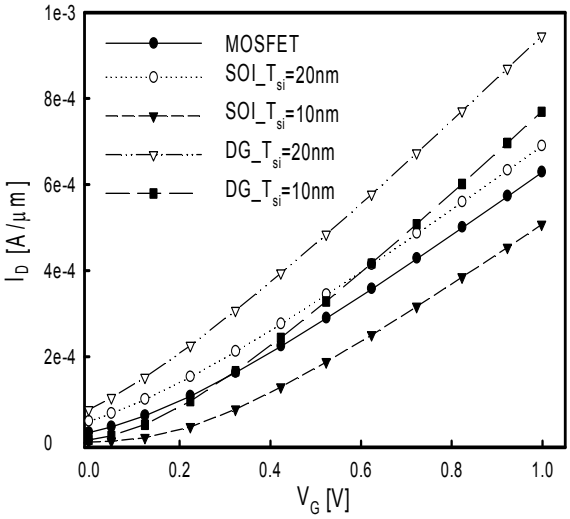


Figure 10. Simulated I_D-V_G curves for devices with T_{ox}=3nm, N_a=10^{18} cm^{-3}, L_G=35nm for V_G = 1.0V, V_D=1.0V.

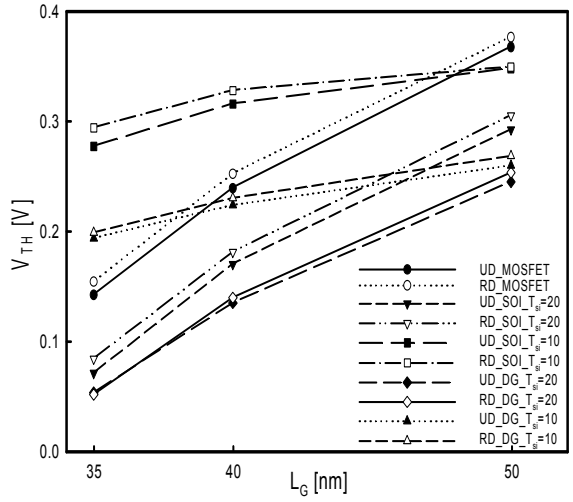
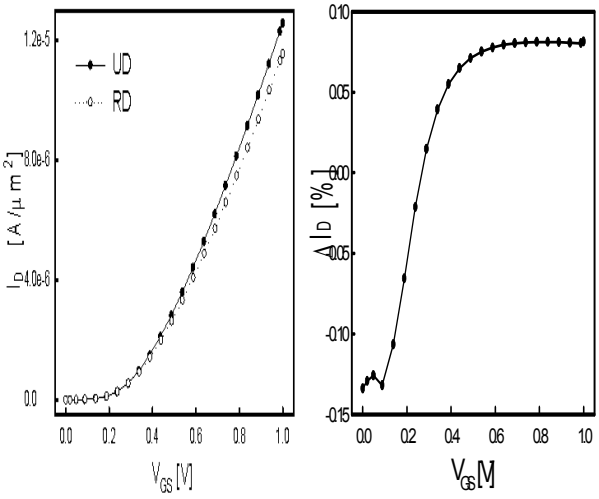


Figure 11. V_{TH} curves for devices with uniform and random dopant concentration for V_G = 1.0V, V_D=1.0V.

Figures 12 report the I_D-V_G curves of devices for uniform and random dopant (UD and RD). ΔI_D is given by ($I_{D\text{-}UD}$ - $I_{D\text{-}RD}$ / $I_{D\text{-}UD}$). Random dopant induces drain current lowering. I_D varies largely in the subthreshold region. As the dopant distribution is becomes more random, the fluctuation of drain current becomes more large. In the uniformly doped case, V_{TH} = 0.32 V. On the other hand, V_{TH} = 0.30 V in the random doped case. The difference is small enough to be neglected. According to our previous results, the results may cause by the simulated devices is thin enough to eliminate the fluctuation caused by random doping effects. DG-MOSFET is promising for CMOS technology at channel length below 50 nm. The results agree with the previous results, that is, V_{TH} can be controlled by the channel thickness of DG-MOSFET.



(a) (b)

Figure 12. (a) Simulated I_D-V_G curves and (b) difference of simulated I_D of uniformly and random dopant DG-MOSFETs.

4 Conclusions

We have performed an investigation of I_D and V_{TH} variation with random dopant for single-gate MOSFET, SOI and double-gate MOSFET. Since three-dimensional simulation takes lots of computing time, the numerical comparison of devices is studied in two-dimensional space. In the subthreshold region, I_D varies largely, which may confuse the signal in a circuit. Random dopant effects should be considered while designing and simulating of semiconductor devices to make the solution close to the real situation. Generally, a 5%~12% fluctuation of drain current exists. Among the three kinds of devices, SOI and DG-MOSFET with thin channel thickness are promising for CMOS technology at channel length below 50 nm. In this study, the simulated single-gate MOSFET is not with optimal designs of channel doping profile.

A device with optimal channel engineering may present a better performance. In addition, the DG-MOSFET with a thin channel thickness is not sensitive to random dopant effects as MOSFET. Furthermore, the DG-MOSFET provides a large I_D. From the fabrication point of view, the unavoidable variation of manufacturing process may induce the fluctuation of device properties in deep sub-micron regime. DG-MOSFET may provide a solution for the difficult position. In addition, deep sub-micron double-gate MOSFETs are simulated in two- and three-dimensional space. According to the results, V_{TH} is underestimated and I_D is overestimated by two-dimensional simulation. Therefore, three-dimensional computation is necessary for simulation of deep sub-micron devices.

Acknowledgement

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