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Modelling, Analysis, Simulation and Experimental Results Regarding a New Boost Converter Topology

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Abstract: - A novel BOOST-type converter is introduced. This converter can be extended to operate as a capacitor-diode multiplier, offering simpler structure and control, higher efficiency, increased reliability, and reduced size and cost compared to a push-pull multiplier. Isolation between input and output can be easily achieved. Other useful extension of the new converter provides continuous or ripple-free output current. Theoretical considerations are confirmed by simulation and experimental results.

Key-Words: - Switching dc-dc converters, converter synthesis, voltage multipliers, simulation.

1 Introduction

It is known that in high-voltage/low current applications such as TV-CRT's, electrostatic systems, lasers, X-ray systems or ion pumps, a capacitor-diode voltage multiplier is preferable to a transformer with large turns ratio and diodes with enormous breakdown voltages [1], [2]. The novel single-stage high voltage converter proposed in the paper is suitable to drive voltage multipliers. Isolation can be easily obtained with the possibility of coupling all the magnetics.

The converter topology is derived and analyzed in Section 2. Extensions related to power factor correction (PFC), quadrupler and multiple stage multipliers and continuous output current are presented in Section 3. The theoretical concepts are verified by simulation and experiments in Section 4, while Section 5 is devoted to conclusions.

2 The new Boost converter topology

The technique based on rotating switching cells [3] is employed for deriving the new BOOST topology. Namely, assuming the input source and the load share a common terminal, as Fig. 1 presents, a three-terminal switching cell is connected between the terminals *g*, *l* and *c* in all the six possible ways and for each combination switch synthesis is then performed [4]. The basic cell used here is drawn in Fig. 2. Switches S_1 and S_3 are synchronously driven, while $\overline{S}_2$ is driven complementary to S_1 and S_3. This is denoted by the negation sign accompanying it and this convention will be used all over the paper.

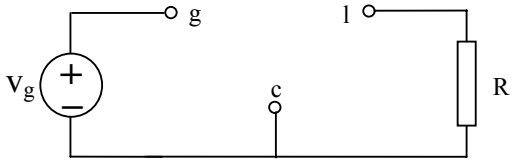

Fig. 1. The supply voltage and the load sharing the same ground terminal.

The duty cycle *D* is defined to correspond to switch S_1. The new converter topology corresponds to the

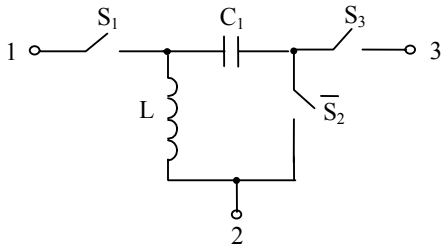

Fig. 2. The basic switching cell.

connection $1 \to g, 2 \to c, 3 \to l$ and after switch implementation the resulting structure is that shown in Fig. 3. As can be seen, indexes in the switching semiconductors follow the notations is Fig. 2.

It is interesting to note that the new converter resembles with a ZETA converter with the output inductor replaced by diode D_3. The cost for this replacement is the loss of continuous output current. The new converter can also be viewed as a classical BUCK-BOOST structure with the positions of the capacitor and diode exchanged and adding another diode and output capacitor. Assuming ideal

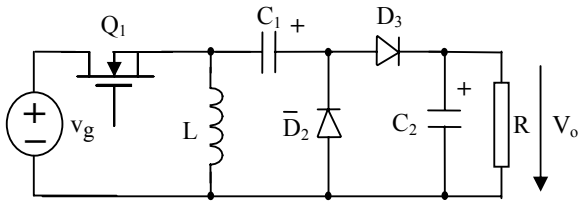

Fig. 3. The new BOOST converter topology.

components and continuous conduction mode (CCM) operation, during the first topological state when Q_1 and D_3 are on and $\overline{D}_2$ is off, the input voltage is applied across the inductor, while capacitor C_1 voltage equals the difference between the output and the input voltage. Assuming $C_2 >> C_1$, then the output voltage remains practically unchanged and only C_1 is discharged to the voltage difference mentioned above. In the second topological state, with Q_1 and D_3 off and $\overline{D}_2$ on, capacitor C_1 voltage is opposite applied across the inductor. Volt-second balance over L provides:

$$DV_g + (1-D)(-V_{C_1}) = 0 \tag{1}$$

On the other side, if C_1 is large enough, it is insignificantly charged by the inductor current in the second topological state and therefore it can be assumed that capacitor C_1 voltage equals $V_o - V_g$ with a high degree of approximation. Substituting V_{C_1} with $V_o - V_g$ in (1), the static conversion ratio can be easily found to be:

$$M = \frac{V_o}{V_g} = \frac{1}{1-D} \tag{2}$$

At this point two aspects should be stressed. First, the output voltage is the same polarity compared to the input voltage, similar to a classical BOOST converter. The second is related to current spikes occurring through Q_1 and D_3. This is because during the second topological state the inductor current is charging C_1 slightly higher than the difference $V_o - V_g$. When Q_1 and D_3 are on at the beginning of the next switching cycle, C_1 is discharging through Q_1 and D_2 to the difference between the C_2 voltage and the input voltage. As no other element is present is the discharging loop, the current is limited only by the Q_1 and D_2 on resistances, by the esr's of the capacitors or other parasitics.

As two passive switches are present in the converter, theoretically discontinuous conduction mode (DCM) can be related to any of the diodes. However, only D_2 can induce DCM operation, as D_3 is used only to provide a current path for discharging C_1, as mentioned earlier. It can be demonstrated in a classical manner that the DCM conversion ratio is:

$$M = \frac{V_o}{V_g} = \frac{1+\sqrt{1+\frac{4D^2}{k}}}{2} \tag{3}$$

with the parameter k given by:

$$k = \frac{2Lf_S}{R} \tag{4}$$

The converter is DCM operating as soon as:

$$k < D(1-D)^2 \tag{5}$$

3 Extensions and applications of the new Boost converter topology

The first application, which is straightforward, is the possibility to use the DCM operated converter in PFC applications. One can easily see that the input part of the converter is similar to that of the BUCK-BOOST converter. Therefore, similar to the BUCK-BOOST converter in DCM, it behaves as an "automatic" or "natural" current shaper [5]. Keeping in mind that v_g is now the output of a full wave uncontrolled rectifier fed by the sinusoidal voltage, then the averaged input current, $\bar{i}_g$, is given by:

$$\bar{i}_g = \frac{v_g}{R_e} \tag{6}$$

where

$$R_e = \frac{2Lf_S}{D^2} \tag{7}$$

Relationship (7) shows that $\bar{i}_g$ is proportional to v_g, so a good power factor corrector can be obtained. Obviously, in order to remove the high frequency components of the chopped input current, a simple LC filter is necessary at the input.

Similar to the ZETA or ĆUK converter, isolation can be achieved splitting the internal capacitor into two series and inserting an ac transformer between the capacitors, as shown in Fig. 4. Note that all the

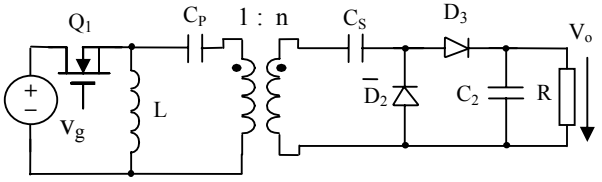

Fig. 4. Isolated version of the new BOOST converter.

magnetics, that is the inductor and the transformer, can be coupled on a single core. It can be easily proved that in this case the static conversion ratio is given by:

$$M = \frac{V_o}{V_g} = n\frac{1}{1-D} \tag{8}$$

The third extension is a capacitor-voltage multiplier, as the structure of the output part is suitable to this kind of application [6]. As shown in Fig. 5, by adding a capacitor and a diode, a quadrupler version of the BOOST converter can be easily obtained. The conversion ratio is equal to:

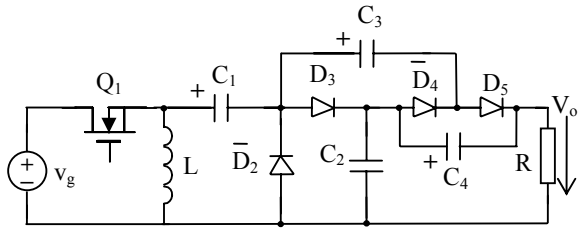

Fig. 5. A capacitor-diode quadrupler extension of the new BOOST converter.

$$M = \frac{V_o}{V_g} = \frac{2}{1-D} \tag{9}$$

Generally, for a *k*-stage multiplier the conversion ratio is:

$$M = \frac{V_o}{V_g} = \frac{k}{1-D} \tag{10}$$

considering that one stage consists of two diodes and two capacitors (hence the new converter is a *k*=1 multiplier). In the voltage multiplier the voltage stress on each switch and capacitor is reduced. For instance, for *k*=2 all switch voltage stresses are equal to $\frac{V_o}{2}$, that obviously is half of the switch stresses in a classical BOOST converter fed by the same input voltage and delivering the same output voltage as the quadrupler. Unfortunately, all the diodes are in series with the output at dc and therefore the conduction losses caused by the forward voltage drop of the diodes are increasing. In addition, output voltage ripple and output resistance are rapidly increasing with *k*. As a consequence, the minimum possible number of stages should be used in order to avoid losses and output voltage ripple.

The new converter can be modified in order to provide continuous (unchopped) output current, as shown in Fig. 6. This is the third extension we shall examine. The converter can be viewed to result from a ZETA converter inserting a voltage doubler before the output inductor.

The two inductors are in a loop with C_1, C_3, and C_4, which appear as short circuits at the switching frequency and its harmonics. Consequently L_1 and L_2 are effectively in parallel and have identical voltage waveforms. Hence they can be coupled [7]

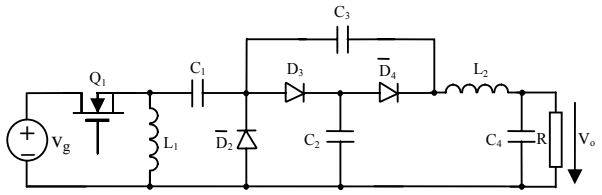

Fig. 6. An extension of the new BOOST converter with continuous output current.

to reduce size and provide ripple-steering feature. Of course a ripple-free output current is more desirable than a ripple-free current through L_1. Therefore L_2 has to be greater than L_1. However, these modifications affect the conversion ratio that is different from the original new converter. As one can easily derive, the conversion ratio is:

$$M = \frac{V_o}{V_g} = \frac{1+D}{1-D} \tag{11}$$

An important advantage is that, compared to the ZETA converter, this extension operates at lower duty cycles for the same conversion ratio. Equating the conversion ration in both cases and denoting by D_N and D_{ZETA} the corresponding duty cycles it results that:

$$D_N = 2D_{ZETA} - 1 \tag{12}$$

Using (12) it is clear that $D_N < D_{ZETA}$ as long as $D_{ZETA} \neq 1$, which is a trivial situation.

Also the voltage stress on the semiconductor switches is lower in this extension. One can easily calculate that:

$$V_{Q_1 off} = V_{D_1 off} = V_{D_2 off} = V_{D_3 off} = \\ = \frac{V_g}{1-D_N} = \frac{V_g}{2(1-D_{ZETA})} \tag{13}$$

Now it is clear that the semiconductor voltage stresses are half of those in the ZETA converter. Theoretically, a capacitor-diode multiplier with more stages (such as a quadrupler) could be inserted to replace the doubler. However in this case more losses will be introduced as mentioned in the analysis of the quadrupler extension.

4 Simulation and experimental results

All simulations were performed using the CASPOC package (Simulation Research) [8]. First the new BOOST converter in Fig. 3 was simulated. Converter parameters were:

$$V_g = 10V;\ L = 450\mu H;\ C_1 = 10\mu F;\quad C_2 = 100\mu F;$$
$$R = 50\Omega;\ f_S = 50kHz;\ D = 0.6$$

The main waveforms are presented in Fig. 7. The enormous current spikes through Q_1 and D_1 are caused by the ideal (without parasitic resistances) circuit elements assumed. I can be seen that the output voltage stays close to 25 V, as expected. The value slightly lower than 25 V is caused by the significant voltage ripple on C_1, as the simulation revealed. A new simulation with a greater value for C_1 solved the problem, fixing the voltage very close to 25 V, namely 24.93 V.

Then the quadrupler extension similar to that in Fig. 5 was investigated for the same load resistance and supply voltage. C_3 and C_4 were 100μF capacitors. Simulation showed that the expected 80V output voltage was not reached, the value being slightly lower. The explanation comes again when capacitor C_1 voltage is examined and a larger voltage ripple is observed. This is due to the fact that, with a voltage doubler, the load "seen" from C_1 is higher compared to the converter without capacitor-diode quadrupler extension. This leads to a larger ripple on C_1 voltage, which makes its average value to deviate more from the theoretical value. This error is "amplified" by the multiplier stage, thus determining the output error voltage. The solution is of course again a greater value for C_1.

Finally, the converter with continuous output current was simulated, the results being presented in Fig. 8 in the situation with coupled inductors in order for the output current to be ripple-free. Converter parameters were:

$$V_g = 20V;\ L_1 = 200\mu H;\ L_2 = 450\mu H;\ C_1 = 47\mu F;$$
$$C_2 = C_3 = C_4 = 100\mu F;\ R = 40\Omega;$$
$$f_s = 50kHz;\ D = 0.6$$

The coupling coefficient was $k = \sqrt{\frac{L_2}{L_1}} = 0.667$. It can be seen that the output current is essentially ripple-free, while the ripple in the current through L_1 is present, being increased compared to the situation without coupling.

Hence all simulations confirmed the theoretical expectations and the feasibility of the new structures.

In order to verify the theoretical predictions the new BOOST converter, with the schematic given in Fig. 3, was breadboarded. The component values were the following:

$$V_g = 12V;\ L = 480\mu H;\ C_1 = C_2 = 220\mu F;$$
$$esr_{C_1} = esr_{C2} = 0.55\Omega;\ R = 75\Omega;$$
$$f_s = 50kHz;\ D = 0.4$$

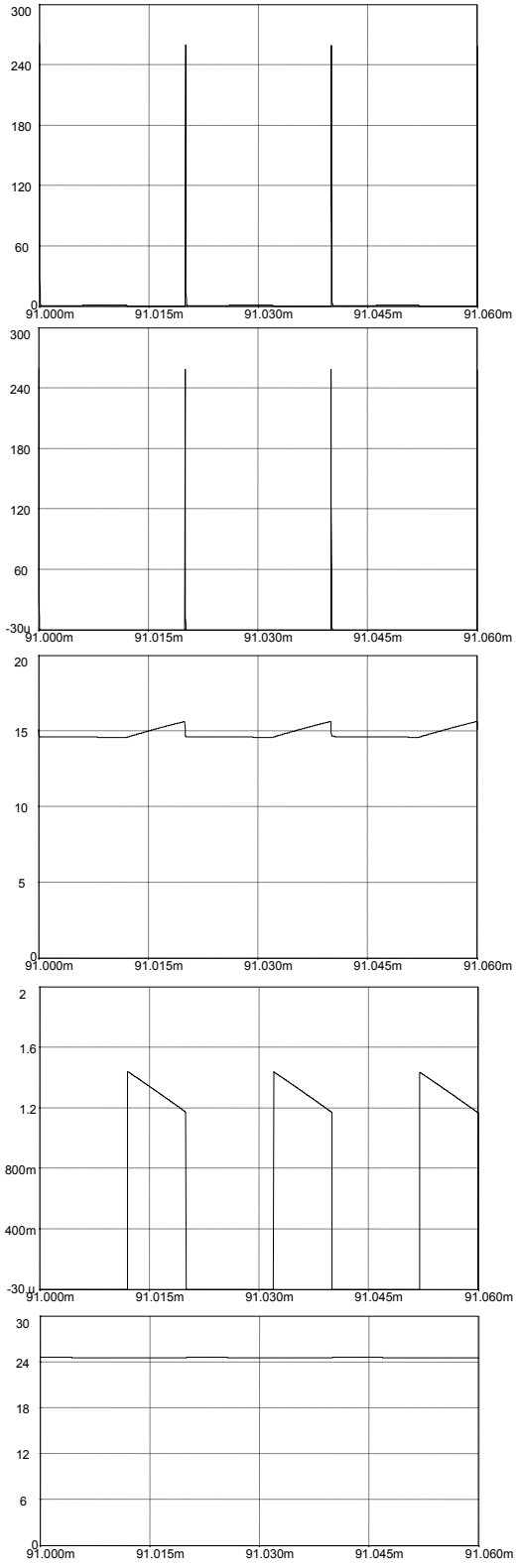

Fig. 7. Transistor current, diode D_3 current, capacitor C_1 voltage, diode $\overline{D}_2$ current and output voltage (this up to down order) in the new BOOST converter topology.

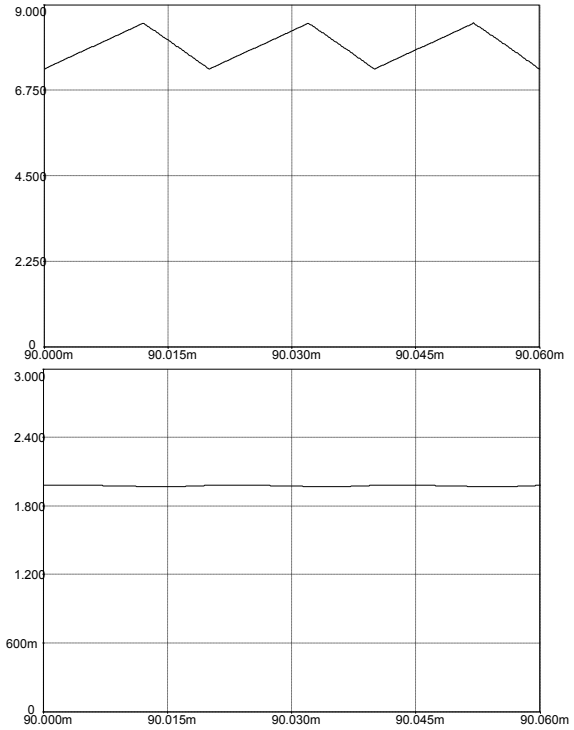

Fig. 8. Inductor L_1 current (up), and output (inductor L_2) current (down) in the new BOOST converter with coupled inductors exhibiting continuous output current.

Switch Q_1 was an IRFPCC50 (International Rectifier) HEXFET Power MOSFET transistor and diodes D_3 and $\overline{D}_2$ were of type HFA15TB60 (International Rectifier) ultra-fast diodes.

The waveforms measured in the experiment are shown in Fig. 9. The agreement between the theoretical predictions, simulated results and measured waveforms is excellent. Then the static conversion ratio was measured as a function of the duty cycle. The results are represented in Fig. 10 together with the theoretical (ideal) characteristic. In Fig. 11 the output characteristic is shown resulting in a 2.4 Ω average output resistance and thus denoting good load regulation even in open loop operation..

Converter efficiency was also measured as a function of the duty cycle. The results are presented in Fig. 12, good efficiency being achieved over the entire duty cycle range. The average efficiency was found to be 87.6%.

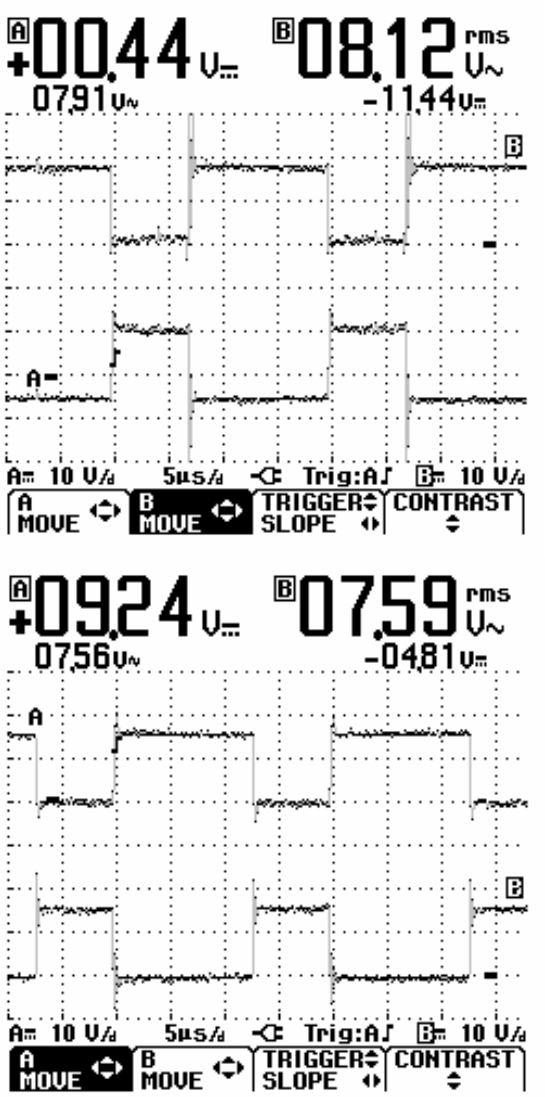

Fig. 9. Transistor drain to source voltage, inductor voltage, diode D_3 voltage, and diode $\overline{D}_2$ voltage (this up to down order) in the experiment with the new BOOST converter topology.

5 Conclusion

A novel three-switch BOOST-type converter is developed. In the new converter isolation is possible in a similar way and with the same advantages as in the ĆUK or ZETA converters. The energy transfer internal capacitor, which has a floating position, provides significant benefits. Thus it can be used to drive capacitor-diode multiplier structures, as a solution for high voltage applications.

Compared to the common PWM multiplier using a BUCK converter followed by a push-pull multiplier, the new converter has the advantage of using only one active switch instead of three active switches. As a consequence, decreased losses and lower cost are achieved and a much simpler control system can be used.

Compared to the classical BOOST structure the new BOOST converter can operate with high power factors even for output voltages slightly higher that

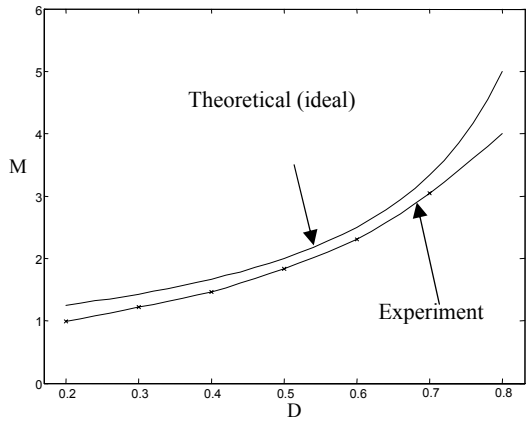

Fig. 10. Experimental and theoretical conversion ratio as a function of the duty cycle.

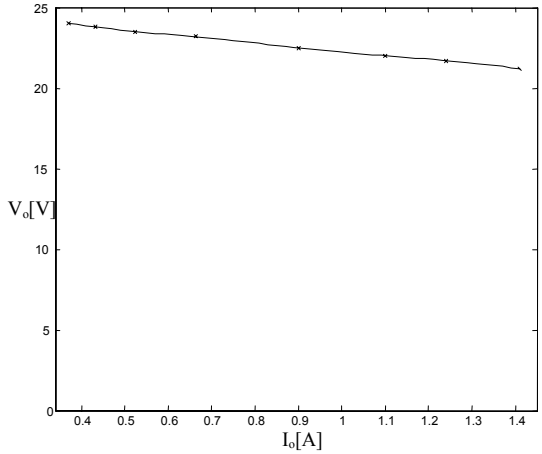

Fig. 11. Load regulation at constant input voltage (output resistance).

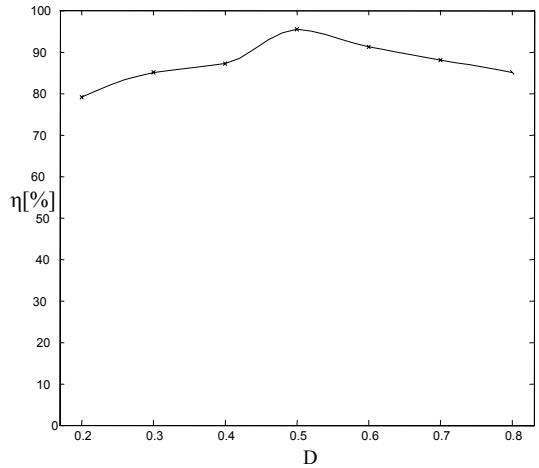

Fig. 12. Efficiency versus duty cycle in the new BOOST converter.

the amplitude of the input voltage, which in the case of a classical BOOST converter is not possible. In fact, the new converter is a perfect "automatic" current shaper.

The voltage multiplier extension of the converter has the benefit that the voltage stress on each switch, diode or capacitor is reduced compared to a classical BOOST converter fed by the same input voltage and delivering the same output voltage. For instance, for k=2 all voltage stresses in the quadrupler are half of the switch voltage stresses in a classical BOOST. Because fast diodes with enormous reverse voltage ratings are hard to find, reduction of the diode ratings decreases the reverse-recovery current in each diode.

Another extension of the new converter exhibits ripple-free output current while preserving its boosting capability. Operation with ripple-free output current has the benefit of reduced size. Moreover, an important advantage of this extension is that all semiconductor (transistor and diodes) voltage stresses are half of those in a ZETA converter operating at the same conversion ratio.

Experimental results all agree well with the theoretical and simulated predictions.

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