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Nonlinear Behavior Modeling of Charge-Pump Based Frequency Synthesizers

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Abstract: A nonlinear behavior model of a charge-pump based frequency synthesizer is implemented and verified against a transistor level implementation in a mixed circuit simulator. The presented behavior model is shown to be drastically faster while still giving an accurate prediction of the acquisition process. The model reliance is assured by identifying and implementing the nonlinear characteristics of each sub-circuit. The challenges of ensuring proper frequency generation even in the presence of process and temperature variations is circumvented by the presented model's reduction in computational cost.

Key–Words: Frequency synthesizer, Behavior model, Nonlinear, Control, Simulation, Computational cost

1 Introduction

The feature sizes of standard available CMOS devices in production are in the range of nanometer and are expected to further decrease over the years to come. This technology scaling further increases the challenges in system and chip design, due to the higher level of integration and increased system complexity. As a consequence unacceptable large computational cost are becoming an increasing problem for the industry. To reduce this impact simplified behavior models can be used to replace the more complex SPICE-level circuit models.

Predicting the frequency synthesizer (FS) feedback loop behavior with traditional transient analysis in a SPICE environment is a time consuming process. This since the input reference frequency (f_{ref}) typically is in the range of MHz, while the voltage-controlled oscillator (VCO) output frequency (f_{osc}) resides within the GHz region. Consequently, small time steps are required to resolve f_{osc}, while the acquisition process time generally is several orders of magnitude longer. FS are, thus, particulary prone to computational cost making behavior modeling an especially attractive method to describe the FS behavior.

This work presents an event-driven modeling technique for charge-pump based FS, as depicted in Fig. 1. A dramatic reduction in computational cost is presented and is achieved by utilization of the phase-frequency detector (PFD) inherent memory functionality. In general there is a trade-off between computational cost and model reliance. Here this trade-off is relaxed by identifying and implementing the crucial nonlinearites of the FS sub-designs into the model. As a consequence, the proposed behavior model gives both an accurate and fast solution of the FS dynamic behavior.

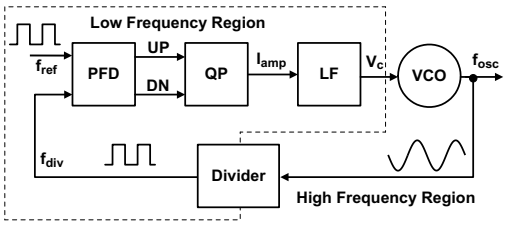

Figure 1: Block schematic over a charge-pump based frequency synthesizer.

2 Nonlinear Behavior Model

The dynamic behavior of a FS can be characterized by several nonlinear time-varying equations. A convenient way of finding such equations is to utilize state-space variables [1], [2], [3]. The system illustrated in Fig. 1 can represented in the phase-domain as illustrated in Fig. 2. In general phase-domain models are utilized to predict in-lock properties of the FS after it is linearized [1], [4], [5]. In this work the phase-domain model is not linearized and it is, therefore, not assumed that the synthesizer is near a locked condition or that it is only exposed to small phase differences between the input signals.

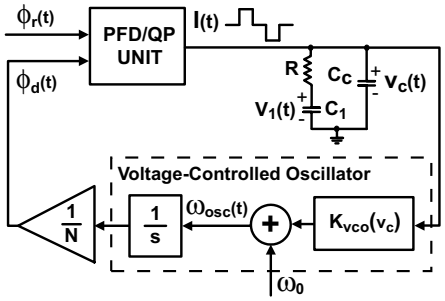

Figure 2: State-space model for the frequency synthesizer.

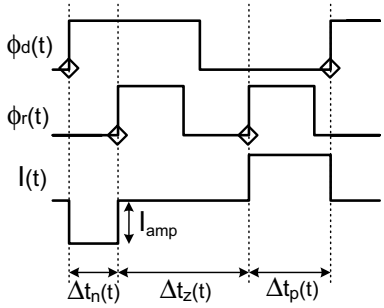

Figure 3: A graphical representation of $\Delta t_{\mathrm{z,p,n}}(t)$.

The proposed behavior model is based on the work presented in [3], but has here been expanded to include crucial nonlinear effects in the FS together with a second-order loop filter (LF). The state-space model as presented in Fig. 2 consists of four variables which describes the system.

- $I(t)$ [dimensionless], which represents the three possible output states of the PFD/QP unit (+1, 0, -1).
- $v_c(t)$ [V], is the output voltage from the loop filter, which in turn controls the output frequency of the VCO.
- $\phi_d(t)$ [rad], is the the divided VCO output signal phase.
- $\omega_{\mathrm{osc}}(t)$ [rad/s], is the VCO output frequency.

$v_c(t)$ and $\phi_d(t)$ are commonly utilized as state-space variables in many presented analyzes [2], [5]. New in this work is the introduction of $I(t)$ and $\omega_{\mathrm{osc}}(t)$. $\omega_{\mathrm{osc}}(t)$ is necessary to fully describe the nonlinear characteristics of the VCO gain ($K_{\mathrm{vco}}(v_c)$), as will be discussed later in this section. $I(t)$ represents the three possible output states of the PFD/QP unit, which captures its memory functionality and are defined as:

$+1$: As long as the PFD/QP is present in this state it delivers charge to the LF increasing its output voltage.

0 : This state represents the high-impedance output where the PFD/QP neither delivers nor drains the LF of charges.

-1 : As long as the PFD/QP is present in this state it drains the LF of charges decreasing its output voltage.

The tristate PFD only reacts to positive transitions in the input signal, see $\Diamond$ in Fig. 3. Thus, generating a state machine with three states [6], within each of these states the system acts as a linear system [3]. The presented behavior model derives the time spent ($\Delta t_{\mathrm{z,p,n}}(t)$) in each of the PFD/QP unit is output states. This is graphically depicted in Fig. 3 where both $I(t)$ and the corresponding $\Delta t_{\mathrm{z,p,n}}(t)$ are shown. It is clear both from Fig. 3 and [3] that only $\Delta t_n(t)$ in the -1 state is independent of the loop parameters. To derive $\Delta t_z(t)$ and $\Delta t_p(t)$ in the 0 and $+1$ states, each sub-circuit in the FS must be investigated.

1) PFD/QP Unit: Although it is efficient in terms of state-space variables to combine the PFD and the QP into one unit, the nonlinearites of the PFD and the QP are best studied separately since they originate from different phenomena.

In the derivation of the proposed state-space model it has not been assumed that the PFD has an ideal linear detection range of $\pm 2\pi$, an otherwise common assumption [1],[2], [4],[5]. However, the actual linear detection range of a nonideal PFD is deteriorated by the reset time of the PFD [6]. In [3] it is shown that the reduced linear detection range deteriorates the acquisition process of the synthesizer by introducing additional cycle slips.

The QP ability to deliver output current is affected by the present voltage value in the LF. This may be further understood if one considers that a typical output stage of a QP consist of a pMOS stacked on top of an nMOS [7]. For such systems it is easy to show that the drain voltage of the transistors in the output stage are equal to the present value of the LF output voltage. Figure 4 shows how the output current from the QP (I_{amp}) is affected by the present voltage value in the LF. It is evident that the transistors in the QP output stage will work in the triode region for large portions of the available $v_c(t)$ and that this phenomena should be included into the model. As also illustrated in Fig. 4 a deliberate large mismatch between the delivering and the draining current sources have been implemented into the model to verify that it works well even under these conditions.

2) Loop Filter: The LF plays an important roll in the appearance of the frequency response of the

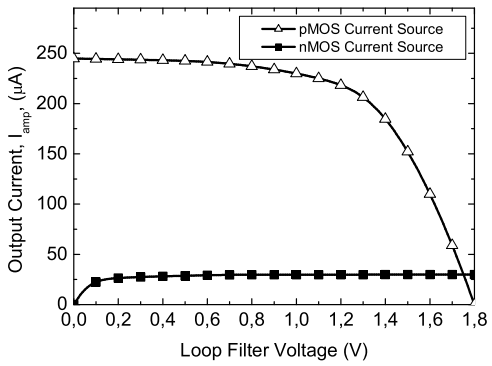

Figure 4: The amplitude of the output current from the charge-pump.

FS, since it mainly sets the bandwidth of the feedback loop. An easy way of illustrating the models concept is to consider a first-order LF as explained in [3]. Here, however, the more practical case of a second-order LF is investigated. The output voltage of the LF is updated once in each state of the PFD/QP unit. This is depicted in Fig. 5 where the LF voltages are depicted as the PFD/QP unit cycles between the 0 and $+1$ states. The LF voltages are updated according to the following equations:

$$\begin{aligned} v_c(t) &= \frac{K}{a}\Big[v_1(0)C_1\big(1-e^{-at}\big) \\ &\quad +I(t)I_{\text{amp}}\big(t+B_2(1-e^{-at})\big) \\ &\quad +v_c(0)C_c\big(1+B_2ae^{-at}\big)\Big], \end{aligned} \tag{1}$$

$$\begin{aligned} v_1(t) &= \frac{K}{a}\Big[v_1(0)C_1\big(1+B_3ae^{-at}\big) \\ &\quad +I(t)I_{\text{amp}}\big(t-\frac{1}{a}(1-e^{-at})\big) \\ &\quad +v_c(0)C_c\big(1-e^{-at}\big)\Big], \end{aligned} \tag{2}$$

where

$$\begin{aligned} a &= \frac{C_1+C_c}{C_1C_cR}, \quad K = \frac{1}{C_1C_cR}, \\ B_2 &= \frac{RC_1^2}{C_1+C_c}, \quad B_3 = \frac{RC_c^2}{C_1+C_c}. \end{aligned} \tag{3}$$

The LF also suffers from several nonidealties. The main nonlinearity is that the output voltage is generally limited by the supply and ground voltages. These limitations are included into the model to accurately predict the FS behavior. Other contributors such as current leakage as well as active solutions are beyond the scope of this study.

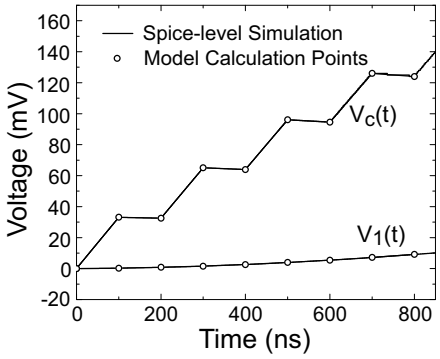

Figure 5: Typical variations in the loop filter voltages.

3) The VCO Gain: Once the variation in the LF voltages are known it is possible to derive how the VCO output deviates from its free-running frequency, ω_0. In general the VCO gain is modelled as a constant value through the tuning range of the VCO. Figure 6 illustrates a typical output frequency of a VCO as a function of the control voltage. It is evident that modeling the gain as a constant is a crude approximation and that its nonlinear behavior should be included into the model. Due to the VCO's nonlinear characteristics it is not possible to describe the output frequency as a linear combination of $v_c(t)$. Instead an integration of the frequency variation is required:

$$\omega_{\text{osc}}(t+\Delta t) = \omega_0 + K_{\text{vco}}(v_c)\int_t^{t+\Delta t} v_c(\tau)d\tau, \tag{4}$$

where K_{vco} is given in [rad/Vs] and the range Δt depends on the present state of $I(t)$. The effects of the integration preformed in (4) will be made clear as the divided phase is investigated below.

Division Factor N: The divider is modelled as an attenuation factor of N and, thus, divides the VCO output frequency into the same frequency range as the

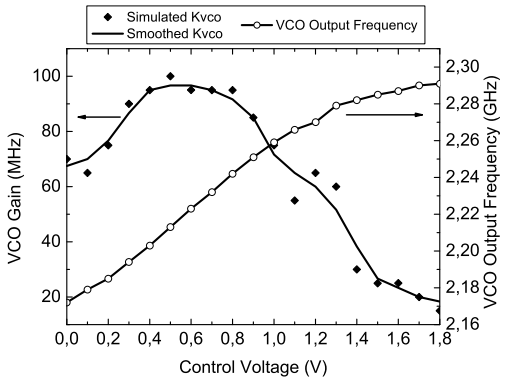

Figure 6: VCO output frequency and gain as functions of the control voltage.

reference signal:

$$\phi_d(t+\Delta t) = \frac{1}{N}\int_t^{t+\Delta t}\left(\omega_0 + K_{\text{vco}}(v_c)\int_t^{t+\Delta t} v_c(\tau)d\tau\right)d\tau. \quad (5)$$

The time spent in each state of $I(t)$ is acquired, by identifying the amount of phase that is needed to reach a positive transition in the $\phi_d(t)$ signal and solving (5) with respect of $\Delta t_{\text{z,p,n}}(t)$. Due to the extra integration introduced by the nonlinear $K_{\text{vco}}(v_c)$ in (4), it is difficult to find a symbolic solution for the different $\Delta t_{\text{z,p,n}}(t)$ as presented in [3]. Instead numerical solutions are utilized to find the correct amount of time spent in the state.

3 Benefits of the Proposed Model

The presented model gives the opportunity to overcome challenges in FS design related to computational cost. By utilizing the model it is possible to vary parameters related to both process and temperature variations, and still preform effective estimations of the FS acquisition behavior. The reduction in computational cost becomes possible through clever usage of the presented state-space variable $I(t)$. In spite of the fact that the entire system is nonlinear, it is clear from Fig. 3 that it may be divided into piecewise linear regions within each $\Delta t_{\text{z,p,n}}(t)$ slot. This fact greatly simplifies the derivation of the state-space equations, since each update $(t+\Delta t_{\text{z,p,n}}(t))$ may be considered linear. Unfortunately, however $\Delta t_{\text{z,p,n}}(t)$ is not uniform for the tristate PFD, which prevents traditional discrete transformations techniques.

To give a better understanding of the large number of verifications that needs to be performed to ensure proper operation, consider that in general on-chip passive components in standard available technologies vary with 10–20% of their nominal value. This affects the LF cut-off frequencies which, consequently, alters the bandwidth of the synthesizer. It is also in general difficult to predict the varactor characteristics in a VCO due to process variations and changes in its bias conditions. This reflects into an uncertain $K_{\text{vco}}(v_c)$, which may alter the loop gain as well as the maximum available output frequency of the synthesizer.

Performing simulations for all combinations of the above given cases becomes extremely time consuming and is generally not applicable utilizing SPICE-level circuit simulators. As a case study consider a FS targeted for the 2.4GHz frequency band. To capture the output frequency a resolution of approximately 5ps is required. To simulate 50μs will, consequently, require 10^6 time steps. In each of these time steps the SPICE-level simulator will need to solve the voltage and current values for every node in the design. With a rough estimate of the number of nodes being equal to 150 in a FS the simulator will need to solve at least $1.5{\cdot}10^9$ equations per scenario, assuming that only one equation is required to find the correct solution. As a comparison to the above given example, the presented state-space behavior model covers the same time range of 50μs with only $\sim$500 time points. It also only has about 20 equations to solve for each time point, which dramatically reduces the total number of equations to roughly 10^4 per scenario, a significant reduction in the number of required calculations. This example stresses the large benefit in utilizing fast behavior models as a complement to the traditional SPICE-level simulations.

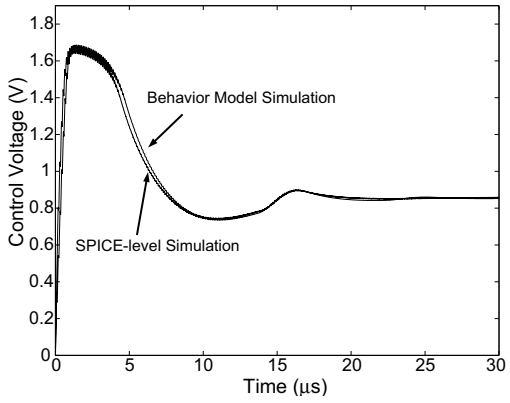

Figure 7: Comparison between a SPICE-level model and the proposed behavior model.

4 Simulation Results

The presented behavior model has been implemented in Matlab, with the nonlinearites described in the previous sections to keep an acceptable reliability for the FS dynamic behavior. The model has been verified against a transistor level implementation of a FS in a standard 0.35μm CMOS process, which has been simulated in the Cadence SpectreRF environment.

The result of these simulations are depicted in Fig. 7 where a very good agreement between the SPICE-level and the proposed behavior model is seen. Note, that the control voltage is depicted in Fig. 7–9 for easy verification against the implementation, the lock frequency has also been investigated and shows as good accuracy as presented in Fig. 7. To illustrate the impact of different variations in the FS behavior consider the simple case where the initial phase error (ϕ_e) between the input signals to the PFD ($\phi_d(t)$ and $\phi_r(t)$) varies. The result of such an experiment is illustrated in Fig. 8, where it is evident that both the transient response as well as the settling time of the FS

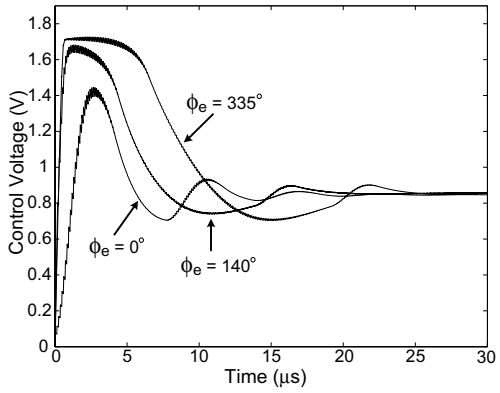

Figure 8: Transient response for different initial phase errors.

is noticeably affected. Figure 9 illustrates the effects of variations in the gain of the VCO. It's obvious that even small variations will cause noticeable difference in the transient behavior in the synthesizer.

The three above given results are only a few examples of what may be investigated with the proposed behavior model. It's possible to perform a large variety of initial conditions and parameter variations for the charge-pump based frequency synthesizer. The proposed model is able to perform this within minutes while for a traditional circuit level simulator the same job would take weeks.

5 Conclusion

This article has presented a behavior model and briefly highlighted its benefits as a complement to SPICE-level circuit models. A state-space model for charge-pump based frequency synthesizers is proposed. By utilization of the model the computational cost of the acquisition process may be drastically reduced. The model reliance is achieved by characterizing the main crucial nonlinearites and implementing their behavior into the model. The main advantages of the proposed model are that the functionality and performance of the synthesizer may be quickly analyzed for a large variety of parameters when there are process and temperature variations present.

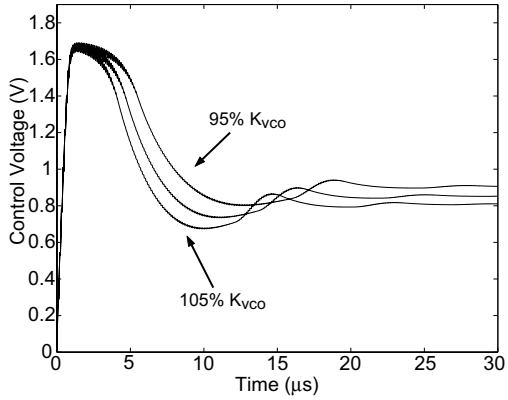

Figure 9: Transient response for variations in the VCO gain.

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