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Low-Power Adaptive Bias/Clock Generator Using 0.18μm CMOS Technology for Multi-Core Continuous Voltage and Frequency Scaling

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Abstract— **This paper presents a continuous voltage and frequency scaling approach achieving lower transition (both energy and time) overheads implied by changing voltage levels, at a very low power dissipation and silicon area cost for multi-processor systems with imposed time constraints. Design and implementation of a very low power, low phase noise, wide tuning range oscillator, and a very high-efficiency adaptive bias regulator block is proposed for battery operated equipment. The proposed design allows implementation of an adaptive bias/clock generator operating at 1 Volt supply voltage. Implemented in 0.18μm CMOS technology, operating at 50MHz to 250MHz, the proposed clock generator (based on voltage controlled ring oscillator, VCO) has a tuning range of almost 50%. At 125MHz, the phase noise of the VCO is -98dBc/Hz @1MHz offset from the carrier. Adaptive bias generator, implemented in same process has an efficiency of 96.5%. The silicon area of the designed adaptive bias/clock generator block is 35μm by 95μm, consuming very low power, 0.41mW.**

I. Introduction

Continued technology scaling over the last three decades has helped to dramatically increase both the embedded functionality per chip area and the operating (clock) frequency. The functionality increase, combined with the diversification of system components and the advances of VLSI design techniques have eventually led to System-on-Chip (SoC) and Network-on-Chip (NoC) concepts with increasing complexity. Application demands and the continuous trend towards mobile, distributed systems have also made battery-powered portable electronic systems very popular and virtually ubiquitous. Nowadays such systems are widely used in many applications, such as mobile computing, information appliances as well as various industrial, medical and military applications. Unfortunately, the battery capacity has improved very slowly (a factor of 2 to 4 over last 30 years), while the systems became more complex and could incorporate more and more functionality over the same time frame. Thus, reducing energy consumption and extending battery lifespan have become a critical aspect of designing battery-powered systems. In addition, the cost of providing power (and associated cooling) has resulted in significant interest in power reduction even in non-portable applications which have access to a permanent power source [9]. Thus, power dissipation and power/performance trade-offs have emerged as major factors in determining the weight, the size and the life-time (autonomy) of portable devices. Managing power dissipation at the system level with dedicated power management units and/or algorithms can decrease energy requirements considerably and thus maximize battery life-time for portable components. Therefore, the power/energy management problem in large scale systems must be attacked both at the system level by means of global power management and optimization techniques, and at the transistor/circuit level by means of innovative structures to limit power dissipation [3], [7], [10].

In this paper, we present a very low power adaptive bias/clock generator that would be uniquely suitable for global energy management of multi-core systems. The proposed module is implemented in 0.18μm CMOS technology, is capable of producing clock frequencies in a wide range between 50MHz to 250MHz, operating at 1V supply voltage. The power dissipation is 410μW, which qualifies the proposed solution for power management of multi-core systems.

II. Power Management in Multi-Core Systems

The ultimate power management goal in portable systems is to reduce "system-level" or global energy consumption, rather than concentrating on local minimization. Recently published system-level dynamic power management (DPM) techniques decrease the energy consumption by selectively placing idle components into discrete lower power states. Recent work on energy optimization includes dynamic voltage scaling (DVS), which refers to varying the operation speed of a processor by changing the clock frequency along with the supply voltage in a discrete manner, and power management, which refers to the use of power-down modes when a processor is idle to reduce power consumption.

In modern SoC / NoC designs integrating both analog and digital functions, continuous DVS approach becomes

much more challenging when considering dynamically providing voltage-frequency couples to each core [4]. This approach requires a dedicated supply voltage - clock generator couple for each core in the system. For on chip clock generation one solution is to create one phase-locked loop (PLL) clock generator running at a high frequency that can be further integer divided down to obtain all desired frequencies. The disadvantage of this scheme is high power consumption and stringent jitter requirements on the PLL [2]. Another method is to have dedicated PLL for each clock domain, but this solution is very costly in terms of power and silicon area. On the other hand using dedicated DC/DC convertors in order to supply each desired voltage level to all system components is not efficient at all in terms of power, silicon area and necessary external components for high efficiency [1]. Dedicated supply voltage regulators operated from a single (or multiple) DC/DC convertor(s) is a promising solution to this problem further increasing power efficiency while reducing associated cost in all terms.

III. Motivational Example

To demonstrate the utility of multi-core dynamic global energy management, consider the following motivational example (Figure 1). Here, each processing element is required to transmit data packets to the next element at a rate that is determined by the operation workload and the buffer capacity. The energy consumed by each core can be expressed as in 1: Where N is number of operations, N_g number of gates, k, K_3 and K_4 are technology related constants, C_L and C_r are the switching load and the rail stray capacitances respectively.

$$E_{core} = N * C_L * V_{ddcore}^2 + \frac{N * k * N_g * V_{ddcore}^2 * K_3 * e^{K_4 * V_{ddcore}}}{V_{ddcore} - V_{th}} + \frac{1}{2} * C_r * \mid V_{ddcore}^2 - V_{th}^2 \mid \quad (1)$$

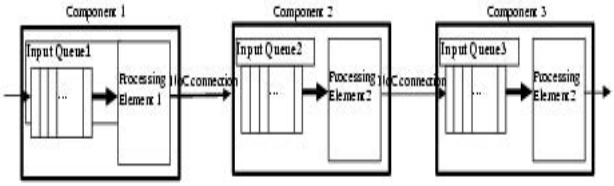

Fig. 1. The simple 3 core system used in the motivational example.

It can be shown that for each set of N_i (i=1,2,3), there is a global optimum in terms of energy consumed by the whole system 2. This optimum point corresponds to a specific clock frequency and supply voltage that must be provided to each core, and adjusted according to the changing workload conditions. To ensure the feasibility of the proposed solution, the silicon area and the power dissipation of each adaptive bias/clock generator must be kept as small as possible.

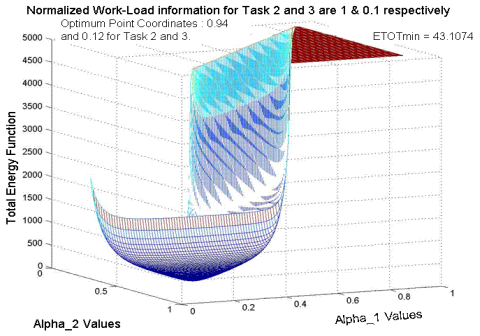

Fig. 2. Normalized system energy consumption for N_1=1, N_2=100 and N_3=0.1 respectively, showing the global energy minimum.

IV. Circuit Implementation

The circuit schematic of the proposed adaptive bias regulator is shown in Figure 3. The adaptive bias OTA (Operational Transconductance Amplifier) is designed to be used as a low power voltage buffer with high slew rate (SR) capability [5]. The design is made so that the amplifier regulates its own bias current depending on the input signal, further lowering power consumption. If no signal is applied the amplifier operates at a very low current and only when a signal is applied (a disturbance occurred on virtual ground) the current in the amplifier increases, resulting a high drive capability. The amplifier is realized in two symmetric parts where in each input stage the current of one branch is directly fed back to the tail current source. Due to the positive feedback used in the scheme, stability in such amplifiers could be a problem. Thus the current feedback ratio should be kept less than 2 in order to overcome such potential problems. The amplifier combines a very low stand-by power dissipation with a high driving capability. Nearly the whole supply current is used to charge/discharge the load so that the designed amplifier has a high efficiency. The efficiency of the regulator under typical simulation conditions is 97.1% with a settling time less than 50ns, driving 20pF of load.

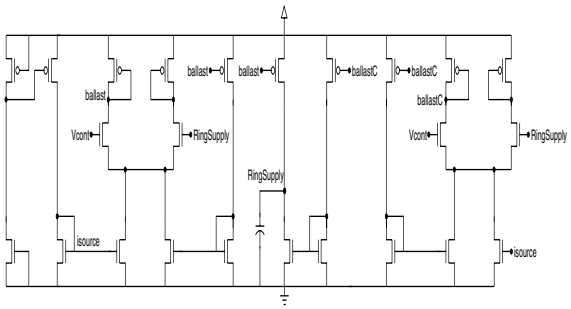

Fig. 3. Designed adaptive bias regulator. (The VCO consisting of 7 single ended stages is omitted.)

Figure 4 shows the simulated operation of the proposed low voltage VCO while the control voltage is swept between 0.5V and 0.85V. It can be seen that the output voltage (i.e. the supply voltage of the ring oscillator)

follows the control voltage with a small offset that does not exceed ΔV_{max} = 30mV at V_{cont} = 0.8V. Typical power consumption of the designed regulator-oscillator remains below 0.41mW at typical simulation corner (typical model parameters, 1V supply voltage at 25°C).

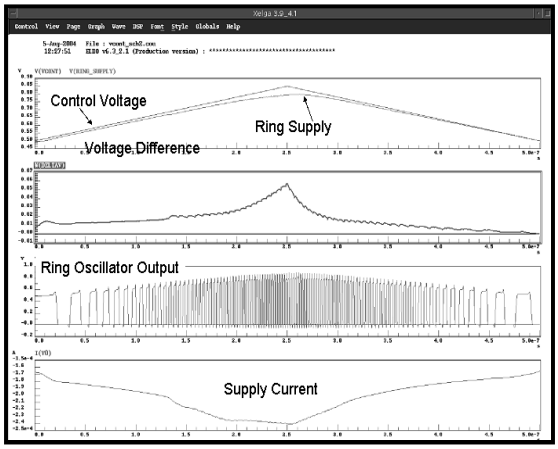

Fig. 4. Simulated input-output wave forms of designed regulator circuit, where the control voltage swept between 0.5V and 0.85V.

In order to provide a complete solution of supply voltage-operation frequency couple we also implemented a 7-stage single ended voltage controlled oscillator (VCO). The supply voltage of the ring oscillator is controlled by the output voltage of the bias regulator, hence directly mimicking the supply voltage - gate delay (maximum achievable frequency) relation given by f_{max}=$[\frac{k*(V_{dd}-V_{th})^{\alpha}}{V-dd}]$. We decided to implement a single ended oscillator due to the fact that a single-ended ring oscillators have a better phase noise at given power dissipation than their differential counterparts. For an N stage oscillator, phase noise of a properly designed differential ring oscillator is approximately N$[\frac{1+V}{I_{tail}R_L}]$ times larger than the phase noise of a single-ended oscillator with same number of stages, power consumption and oscillation (center) frequency. We decided to design a single-ended voltage controlled ring oscillator with 7 stages. The supply voltage of the designed oscillator is controlled via an Adaptive Bias Regulator to adjust the oscillation frequency, which helps to increase efficiency and provides a wide tuning range at very low supply voltage levels (1V). In Figure 5, the oscillation frequency of the VCO is seen as a function of the control voltage. The tuning range of designed VCO occupies 50MHz - 200MHz frequency range for 0.6V and 0.8V control voltage respectively. The gain of the VCO is 0.68GHz/V. Besides the high tuning range the linearity of the designed VCO remains within ±5% limits. Fundamental frequency of 125MHz at typical simulation corner changes from 91.07MHz for 185.64MHz for worst-case process corner to best-case. Temperature and supply stability were also checked. Frequency pushing of VCO is 65.5MHz/V and temperature drift is less than 255kHz/°C. The phase noise of the designed oscillator at 1MHz offset is -98.2dBc/Hz.

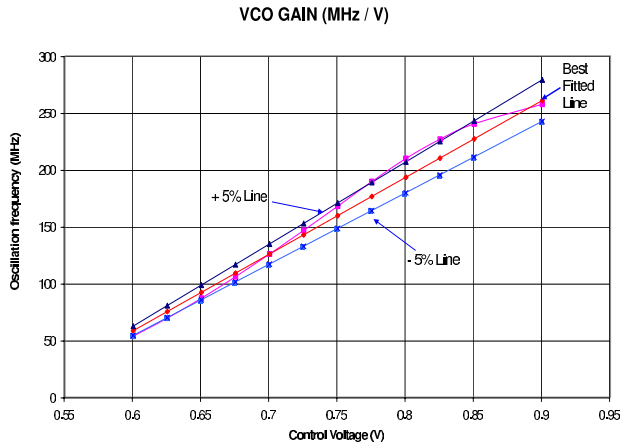

Fig. 5. Simulated VCO gain, linearity and frequency tuning range.

V. Silicon Implementation

The circuit has been designed and fabricated using a conventional 0.18μm CMOS (logic) technology. (The total area occupied by the circuit is only 95μm × 35μm). The measured tuning range has been reduced to 60MHz-195MHz, dissipating average power of 0.41mW throughout the tuning range. Measured VCO gain and frequency pushing of the design are 0.5GHz/V and 145MHz/V respectively. The design exhibits a linearity within ±5% limits. Measured regulator efficiency is 96.5%. It should be noted that device threshold voltages were found to be 100mV higher than specified in this particular fabrication run. The measured phase noise of the VCO (-82dBc/Hz @1MHz frequency offset) is shown in Figure 6. Still, the measurement results obtained from the test chip indicate that the performance of the proposed circuit will remain within the specified bounds, provided that the device parameter variations are limited. The designed bias regulator-VCO with its properties of very low power dissipation, low phase noise, wide tuning range with high linearity , high efficiency and very small silicon area, is a good candidate that can be used in portable, battery-operated applications. Especially considering applications where multiple units (modules) on a single SoC are subject to DVS (hence, they require individual adjustment of their clock frequencies), the availability of a very compact and low-power VCO that is constructed with no on-chip inductors could be very beneficial.

To prove the functionality of the proposed bias/clock generator, a simple (8×8)-bit parallel multiplier [8], unit was also implemented, where the supply voltage is controlled by the doubled bias regulator output and the clock frequency is provided directly by the VCO output. The multiplier was designed to operate in the range of 1.2V-50MHz to 1.8V-200MHz.

Functionality of the (8×8)-bit parallel multiplier is tested for different supply voltage operating frequency settings. As shown in Figure 7 design is functional for

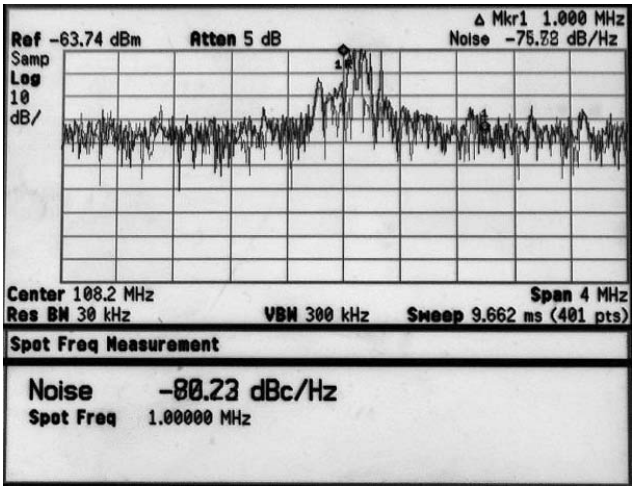

Fig. 6. Measured phase noise of the proposed VCO is -82dBc/Hz 1MHz offset from the carrier.

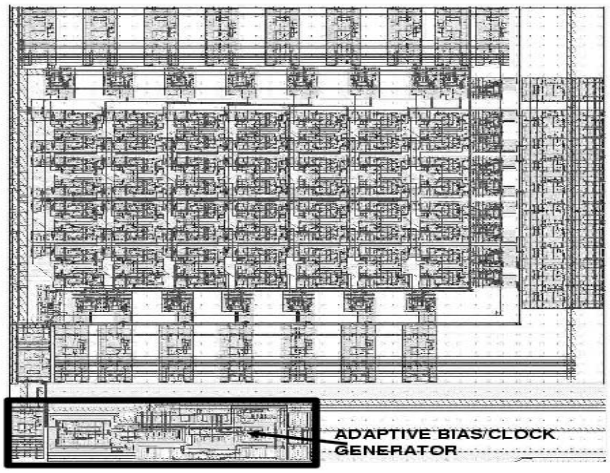

Fig. 8. Full custom layout view of the designed (8X8)-bit parallel multiplier with dedicated adaptive bias/clock generator. The total silicon area of the design is 220μm by 235μm.

125MHz operation speed for all three voltage settings, 1.2V-1.5V-1.8V. The amount of power savings by reducing the clock frequency alone (from 200MHz to 50MHz) is 17.74%, whereas the power savings is shown to be 74% when both supply voltage and clock frequency are scaled down simultaneously. Layout view of one of the (8×8)-bit multiplier circuit neighboring bias regulator-VCO couple with necessary in/out-put level shifters (LS) can be seen in Figure 8. Total area occupied by the design is only 220μm × 235μm.

VI. Conclusion

Dynamic voltage scaling (DVS) is a popular approach for reducing energy consumption of integrated circuits when peak performance is unnecessary. However, achievable energy saving by discrete voltage-frequency steps alone is becoming limited as both energy and time overheads are considered between discrete state transitions. The designed adaptive bias/clock generator block with its properties of very low power dissipation, high efficiency, low phase noise, wide tuning range with high linearity and very small silicon area, is a good candidate that can be used in portable, battery-operated applications. Especially considering applications where multiple units (modules) on a single SoC where power management problem becomes much more challenging when considering dynamically changing energy trade-offs between various system components, including multiple processor cores, memory blocks, RF front-ends, analog interfaces, etc.Thus utilizing a unique supply voltage - operation frequency couple for each core subject to DVS in SoC designs become virtually ubiquitous and very beneficial. The proposed solution is capable of adjusting voltage supply-operation frequency in a continuous manner, further reducing related overheads and increasing power efficiency of SoC (i.e. lower energy per instruction).

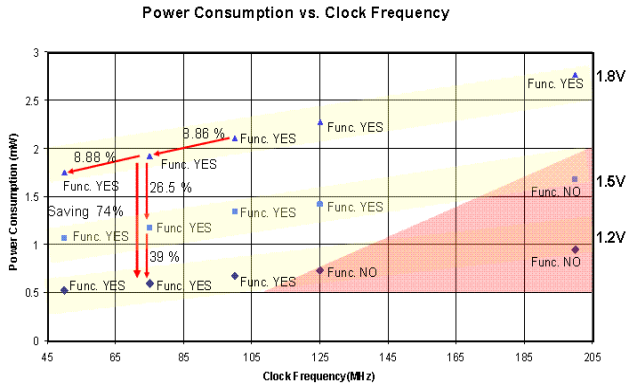

Fig. 7. Measured power dissipation of the (8×8)-bit multiplier unit under three different operating voltages, and varying clock frequencies where functionality violations are indicated as *Func.NO*. The power savings obtained by voltage-frequency scaling are indicated in the figure.

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