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A Perfect Matching Layout for Multiple Cascode Current Sources

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Abstract: - The paper proposes two novel perfect-matching layout techniques for four or more cascode current sources. The purpose is to reduce the matching sensitivity of linear parameter gradients in high performance integrated circuit applications. One layout technique for matching four current sources consists of three sets of four-segment rectangular structure and utilizes two level hierarchies to equalize the outputs of four current sources. Another proposed novel layout technique adopts an inner four-segment two-current-source rectangular structure to uniformly distribute the current to outer four-segment four-current-source rectangular structure for perfect matching. The latter topology has better area efficiency. Furthermore, these two proposed layout techniques can be easily extended to 8, 16 or more perfect matching current sources. With MATLAB simulations, both layouts are verified to completely eliminate current mismatch caused by the linear gradient of threshold voltage.

Key-Words: - device mismatch, current sources, linear gradient, matching layout

1 Introduction

Due to the influence of many unavoidable factors including process variation and environment difference, present manufacturing echnologies are still unable to produce devices without mismatch problems. However, these component mismatches destroy the performance of high accuracy integrated circuits. For example, a simple current mirror usually requires two perfectly matched transistors. But there is always some mismatch between these two transistors after fabrication and the circuit performance will be degraded seriously. In general, the mismatches caused by manufacturing processes can be classified into systematic mismatch and random mismatch. The random mismatch can only be reduced by increasing layout area, but the systematic mismatch can always be alleviated through proper layout techniques. This is the exact focus of the proposed paper.

The amount of mismatch can be simulated by establishing a gradient model for the manufacturing process and the layout technology [1],[2]. The paper adopts the linear gradient model as did by Lans'[3-8]. Any parameter variation would alter the characteristics of transistors and their applications. Among lots of transistor parameters, the variation in threshold voltage has the most serious impact on transistor currents [3]. The former researches all focused on the layout techniques for two matching transistors or two matching current sources under the presence of linear parameter gradient. Nowadays, integrated circuits are getting more complicated. The dual matching layout techniques no longer satisfy all of the high performance integrated circuits. Therefore, two novel layout techniques for matching four current sources are proposed in this paper.

One layout technique is based on the four-segment rectangular layout, capable of canceling the linear gradient mismatch of two current sources, proposed by Lan *et al*[4]. A four-segment rectangular layout is utilized first to cancel the linear gradient mismatch of those two transistors in base current mirror. Then, the other two four-segment rectangular layouts are adopted to equally divide two currents of the base current mirror into four cascode transistors to generate four fully matched current outputs. An alternative way to match four cascode current sources is to use the inner four-segment rectangular layout to generate two matched currents for the base current mirror as described in the former technique. However, four cascode transistors are evenly distributed around the outer four-segment rectangular layout to evenly divide two currents into four outputs.

The paper is organized as follows. Section 2 introduces the influence of linear gradient to transistor threshold voltage. In section 3, prior studies related to two matched current sources are discussed. These two novel layout techniques related to matching four current sources are depicted in detail and verified with simulation results in section 4. The conclusion is given in section 5.

2 Linear Gradient Model

For clarity, the linear gradient model adopted by Lan *et al* is redrawn in Fig. 1 where α and θ represent the magnitude and the orientation of the gradient vector ***G*** respectively. For a given reference origin ***O***, the parameter variation at any location is given as the inner product of its position vector and the gradient vector ***G***. For example, the parameter variation for a location with position vector $A = \beta\angle\phi$ is calculated as:

$$\begin{aligned} G \bullet A &= \alpha\beta\cos\theta\cos\phi + \alpha\beta\sin\theta\sin\phi \\ &= \alpha\beta\cos(\theta-\phi) \end{aligned} \quad (1)$$

The less phase difference between position vector and the gradient vector is, the larger the parameter variation will become. The best way to eliminate the linear gradient mismatch is to make both vectors perpendicular to each other. However, the orientation of the gradient vector cannot be predicted in advance. A better strategy is to generate symmetric layouts for matched devices to make their parameter variations as closed to each other as possible. As shown in Fig. 1, the parameter variations for devices with position vectors A and A′ will be the same and their characteristics will be perfectly matched. In brief, the layout for devices owns more degrees of symmetry, the better matching performances can be fulfilled.

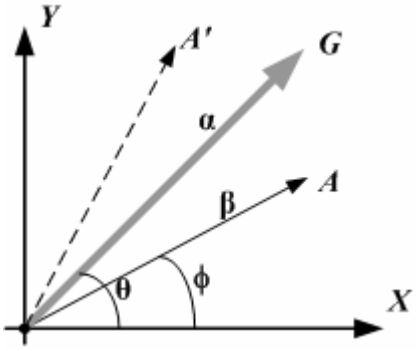

Fig. 1. Linear gradient model.

In the following sections, only the linear gradient model is considered for the layout matching of current sources. Without the consideration of random mismatch in this paper, the research will be focused on better matching layout strategies instead of device sizing. The simple current mirror is plotted in Fig. 2 to initiate the discussion of matched layouts. Later, it will be extended to more complicated circuits. All simulations in this paper will be done by MALTAB.

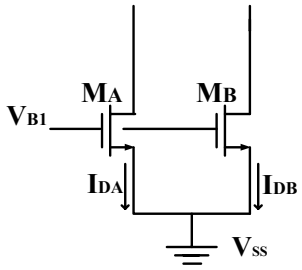

Fig. 2. Basic current mirror circuit.

3 Layout Matching for Two Current Sources

The widely used approach for predicting the effects of the threshold voltage gradient is based upon deriving an equivalent threshold voltage for the device as given by the following equation[4].

$$V_{Teq} = \frac{\iint_{Active\_Area} V_T(X,Y)dxdy}{Active\_Area} \quad (2)$$

Where V_{Teq} can be viewed as the equivalent threshold voltage at the moment of the device. The simplest layout for basic current mirror is shown in Fig. 3 where W and L are the width and length of the channel region, and D is the spacing between the channel regions of two transistors. The reference origin ***O*** is chosen to simplify the overall calculation. The linear gradient of threshold voltage is assumed to spread over the channel regions of transistors. With moments locating at (-D/2-W/2,0) and (D/2+W/2,0) respectively, the average threshold voltages of M_A and M_B can be calculated by (1) as:

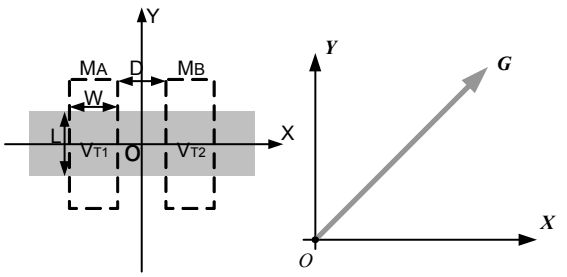

Fig. 3. Simple layout for current mirror.

$$\begin{aligned} V_{T1} &= V_{TN} + (-D/2 - W/2, 0) \bullet (\alpha\cos\theta, \alpha\sin\theta) \\ &= V_{TN} - \alpha\left(\frac{W}{2} + \frac{D}{2}\right)\cos\theta \end{aligned} \quad (3)$$

$$\begin{aligned} V_{T2} &= V_{TN} + (D/2 + W/2, 0) \bullet (\alpha\cos\theta, \alpha\sin\theta) \\ &= V_{TN} + \alpha\left(\frac{W}{2} + \frac{D}{2}\right)\cos\theta \end{aligned} \quad (4)$$

where V_{TN} is the threshold voltage at the reference origin ***O*** and V_{T1}, V_{T2} are the equivalent threshold

voltages of M_1 and M_2 correspondingly. Neglecting the early effect, the currents I_{D1} and I_{D2} of M_1 and M_2 in saturation region can be obtained by substituting (3) and (4) into the following equation.

$$I_D = \frac{1}{2} C_{OX} \mu_N \left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \quad \textbf{(5)}$$

The definition of mismatch is shown in (6) [4]. This value will vary with the orientation angle θ of the linear gradient effect.

$$Mismatch = \frac{I_{D1} - I_{D2}}{I_{D2}} \times 100\% \quad \textbf{(6)}$$

The simulation result of the simple current mirror layout shown in Fig. 3 is depicted in Fig. 4 by calculating equations (1)-(5) with the help of MATLAB. The matching of I_{D1} and I_{D2} becomes the best when θ=90° and 270° which lie exactly along the symmetric axis of the layout as predicted in Section 2. On the contrary, the matching of I_{D1} and I_{D2} becomes the worst when θ=0° and 180°. The mismatch can approach as high as 5%.

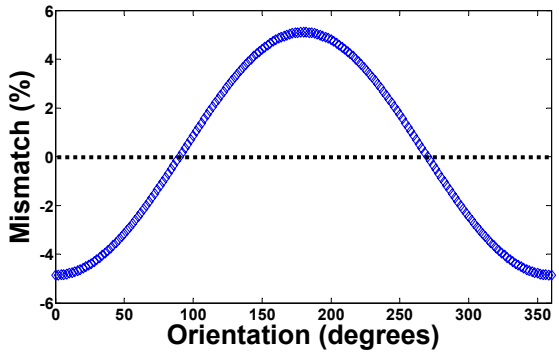

Fig. 4. Simulation result of simple current mirror layout.

The other five different layout techniques ever presented for matching two current sources are shown in Fig. 5. With only one symmetric vertical axis, the interdigitized layout structures in Fig. 5(a) and Fig. 5(b) can be used to reduce the matching sensitivity to horizontal device gradient. On the other hand, the common centroid layout techniques in Fig. 5(c) and Fig. 5(d) can be used to reduce the matching sensitivity to both horizontal and vertical device gradients due to symmetric vertical and horizontal axes. Since the layout in Fig. 5(d) is more compact, its performance is better than that of Fig. 5(c).

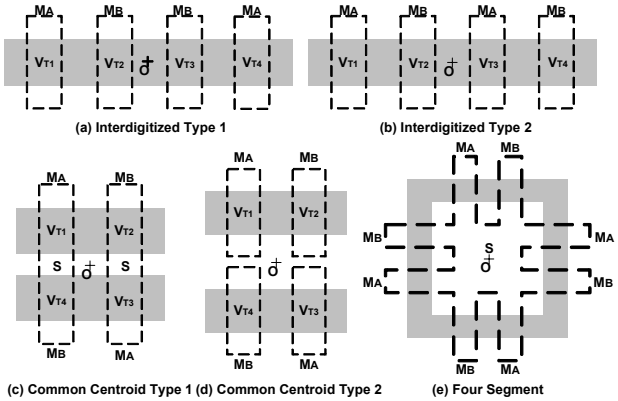

Fig. 5. Five different layout techniques proposed by prior researches

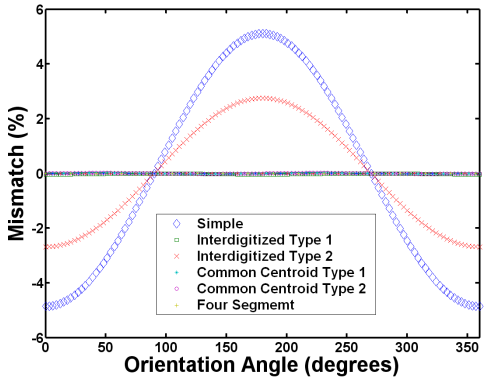

Fig. 6. Simulation results of six different layout methods with MATLAB.

Table 1. Comparison of the performance of six different layout techniques.

Structure	Worst Mismatch (%)			
	Simple integral model	Segmented integral model	Distributed simulator	Effective Resolution
Simple	5.1092	5.1092	4.8807	3-bit
Interdigitized Type I	0	3.6918e-2	3.0885e-2	11-bit
Interdigitized Type II	2.7552	2.7547	2.6329	4-bit
Two-Segment Common Centroid Type I	0	2.0005e-2	1.6966e-2	12-bit
Two-Segment Common Centroid Type II	0	1.6928e-2	1.8949e-2	12-bit
Four-Segment Common Centroid	0	2.0966e-14	1.4090e-4	18-bit

The most interesting topology called four-segment rectangular layout is redrawn in Fig. 5(e). With totally four symmetric axes, its performance is definitely better than those of Fig. 5(a)~(d). The simulation results are shown in Fig. 6 while the performances of these six different techniques are summarized in Table 1. The mismatch of the order 10^{-14} in Table 1 is caused only by the computation error of MATLAB. Since π is not perfectly represented in MATLAB, there is always some computation errors existed. For example, the value of sinπ, of the order 10^{-15} in MATLAB, is not exactly zero. Taking the error of MATLAB into consideration, the simulated mismatch for

four-segment rectangular layout should be precisely zero. It means that four-segment rectangular layout can fulfill perfect matching under linear parametric gradient.

In the following sections, the concept of four-segment rectangular layout will be extended to eliminate the mismatch of four or more current sources.

4 Proposed Perfect Matching Layout for Four Cascode Current Sources

Based on four-segment rectangular layout technique, two new layout topologies are proposed in this paper. The discussion is given in detail as follows.

4.1 Two-level Hierarchy Layout Technology for Four Cascode Current Sources

The proposed four cascode current sources circuit is shown in Fig. 7. along with the detail layout shown in Fig. 8.

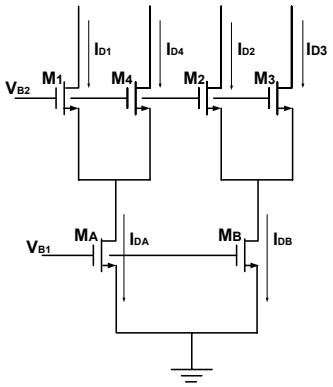

Fig. 7. Proposed four cascode current sources circuit.

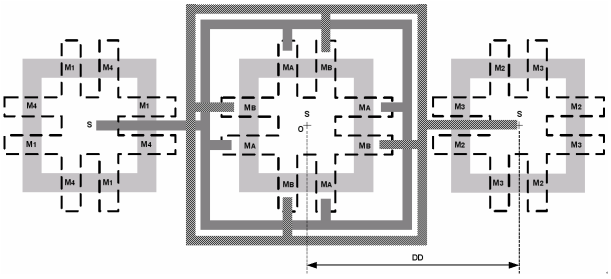

Fig. 8. Three-level hierarchy layout technology for eight cascode current sources

The first level four-segment rectangular layout is used to provide the perfectly matched currents I_{DA} and I_{DB} under linear gradient environment. For second level layout, two four-segment rectangular structures are utilized to uniformly split the currents I_{DA}, I_{DB} into I_{D1}, I_{D4} and I_{D2}, I_{D3} respectively. There are totally four perfectly matched current sources can be got. For mathematical formulation, the threshold voltages of unit transistors M_A and M_B can be easily derived as [3]:

$$V_{T1} = V_{TN} - \alpha\left(\frac{W}{8}+\frac{D}{2}\right)\cos\theta + \left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\sin\theta$$

$$V_{T2} = V_{TN} + \alpha\left(\frac{W}{8}+\frac{D}{2}\right)\cos\theta + \left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\sin\theta$$

$$V_{T3} = V_{TN} + \alpha\left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\cos\theta + \left(\frac{W}{8}+\frac{D}{2}\right)\sin\theta$$

$$V_{T4} = V_{TN} + \alpha\left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\cos\theta - \left(\frac{W}{8}+\frac{D}{2}\right)\sin\theta$$

$$V_{T5} = V_{TN} + \alpha\left(\frac{W}{8}+\frac{D}{2}\right)\cos\theta - \left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\sin\theta$$

$$V_{T6} = V_{TN} - \alpha\left(\frac{W}{8}+\frac{D}{2}\right)\cos\theta - \left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\sin\theta$$

$$V_{T7} = V_{TN} - \alpha\left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\cos\theta - \left(\frac{W}{8}+\frac{D}{2}\right)\sin\theta$$

$$V_{T8} = V_{TN} - \alpha\left(\frac{W}{4}+\frac{3D}{2}+\frac{L}{2}\right)\cos\theta + \left(\frac{W}{8}+\frac{D}{2}\right)\sin\theta$$

It was proven that the currents of M_A and M_B perfectly trace each other by substituting the above threshold voltages back into (5) [3]. The threshold voltages of M_2 and M_3 can be derived from those of M_A and M_B by:

$$V_{Ti}' = V_{Ti} + \boldsymbol{G \bullet DD} \quad 1 \le i \le 8$$

Since $\boldsymbol{G \bullet DD}$ can be viewed as a constant term in each threshold voltage and will induce symmetric impact on the drain currents of M_2 and M_3, the currents of M_2 and M_3 still perfectly trace each other. Similarly, the threshold voltages of M_1 and M_4 can be derived from those of M_A and M_B by:

$$V_{Ti}'' = V_{Ti} - \boldsymbol{G \bullet DD} \quad 1 \le i \le 8$$

And the currents of M_1 and M_4 are perfectly matched, too.

4.2 Four-segment Rectangular Structure for Four Cascode Current Sources

Although the above proposed layout technique could achieve four perfect-matching current sources, the layout itself is not compact and cannot be an area efficient solution!

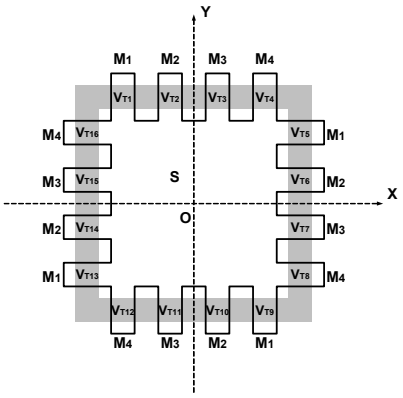

Fig.9. Four-segment rectangular structure for four current sources

Subsequently, we proposed another novel technique including four-segment rectangular layout for four current sources as shown in Fig. 9. There are four transistors M_1, M_2, M_3, and M_4 to be matched. The transistors are equally distributed onto the four sides to get maximal symmetry. The threshold voltages of 16 unit transistors can be derived as:

$$V_{T1} = V_{TN} - \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\cos\theta + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T2} = V_{TN} - \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\cos\theta + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T3} = V_{TN} + \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\cos\theta + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T4} = V_{TN} + \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\cos\theta + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T5} = V_{TN} + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta + \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\sin\theta$$

$$V_{T6} = V_{TN} + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta + \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\sin\theta$$

$$V_{T7} = V_{TN} + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta - \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\sin\theta$$

$$V_{T8} = V_{TN} + \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta - \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\sin\theta$$

$$V_{T9} = V_{TN} + \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\cos\theta - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T10} = V_{TN} + \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\cos\theta - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T11} = V_{TN} - \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\cos\theta - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T12} = V_{TN} - \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\cos\theta - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\sin\theta$$

$$V_{T13} = V_{TN} - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta - \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\sin\theta$$

$$V_{T14} = V_{TN} - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta - \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\sin\theta$$

$$V_{T15} = V_{TN} - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta + \alpha\left(\frac{D}{2}+\frac{W}{16}\right)\sin\theta$$

$$V_{T16} = V_{TN} - \alpha\left(\frac{5D}{2}+\frac{W}{4}+\frac{L}{2}\right)\cos\theta + \alpha\left(\frac{3D}{2}+\frac{3W}{16}\right)\sin\theta$$

The simulation results for current matching are shown in Fig. 10 and Fig. 11 respectively. It can be seen that ideal matching can only be realized for pairs (I_{D1}, I_{D4}) and (I_{D2}, I_{D3}). But the mismatch between these two pairs is too large to make this layout perfect. To solve this problem, an inner four-segment rectangular layout is adopted to generate two perfectly matched currents I_{DA} and I_{DB} first. Then the above four-segment rectangular layout for four current sources is used as the outer ring to route I_{DA}, I_{DB} to pairs (I_{D1}, I_{D4}), (I_{D2}, I_{D3}) correspondingly as shown in Fig.12.

It can be easily obtained that $2I_{D1}=2I_{D4}=I_{DA}$ and $2I_{D2}=2I_{D3}=I_{DB}$. Since $I_{DA}=I_{DB}$, $I_{D1}=I_{D2}=I_{D3}=I_{D4}$ could be obtained under linear gradient condition. The simulated result of current mismatch in Fig. 13 shows that the mismatches between each two current sources are all zeros. This layout is more compact and will be more area-efficient as compared to the matching layout stated in section 4.1.

According to the proposed layout technology, the topology for four perfectly matched current sources can be easily extended to match more current sources. For example, the circuit for matching eight cascode current sources is shown in Fig. 14. And the corresponding layout for three-level hierarchy layout technology and four-segment rectangular structure are depicted in Fig. 15 and Fig. 16 respectively.

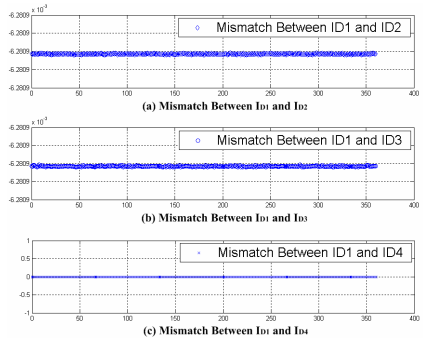

Fig. 10. (a) Mismatch between I_{D1}, and I_{D2} (b) Mismatch between I_{D1} and I_{D3} (c) Mismatch between I_{D1} and I_{D4}

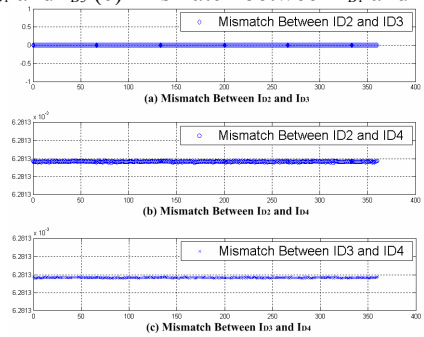

Fig. 11. (a) Mismatch between I_{D2} and I_{D3}, (b) Mismatch between I_{D2} and I_{D3}, (c) Mismatch between I_{D3} and I_{D4}

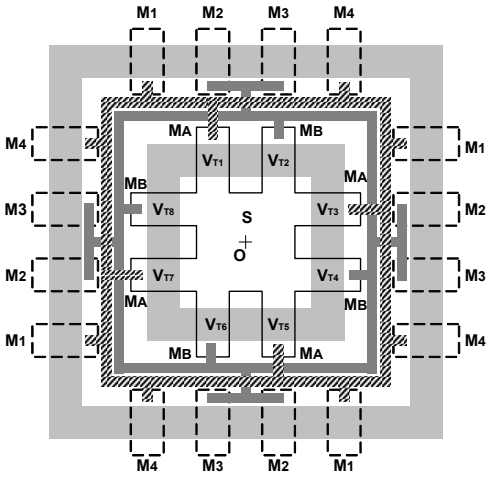

Fig. 12. The modified four-segment rectangular structure for four cascode current sources

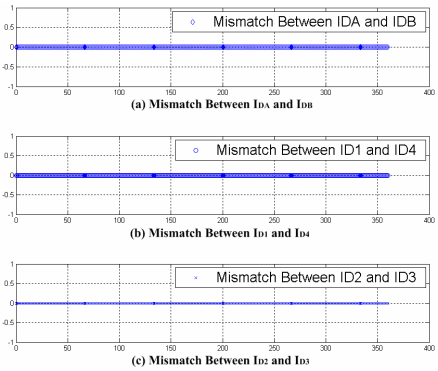

Fig. 13. (a) Mismatch between I_{DA} and I_{DB}, (b) Mismatch between I_{D1} and I_{D4}, (c) Mismatch between I_{D2} and I_{D3}

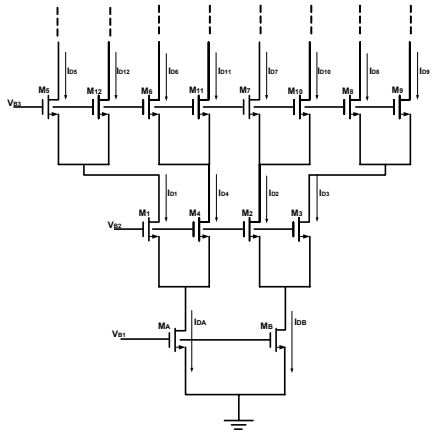

Fig. 14. Proposed eight cascode current sources circuit.

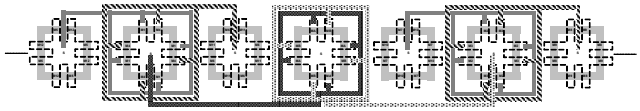

Fig. 15. Three-level hierarchy layout technology for eight cascode current sources

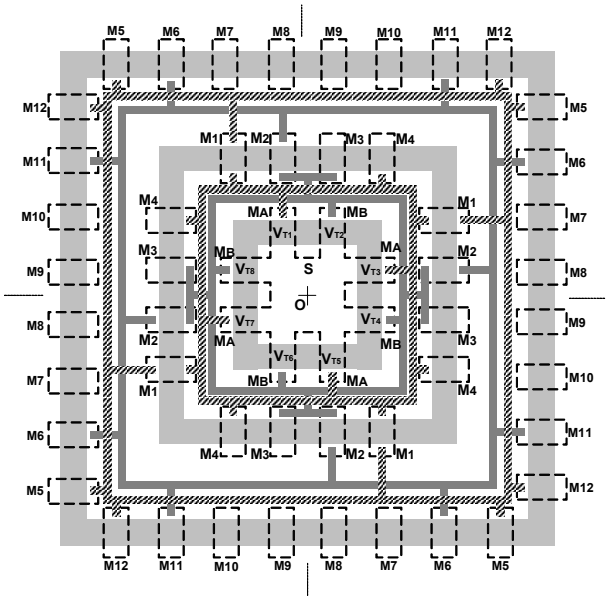

Fig. 16. Four-segment rectangular structure for eight cascode current sources

5 Conclusion

Two layout techniques for matching multiple current sources have been proposed to eliminate the mismatch in the presence of linear parameter gradient. First, by combining prior good practice in layout techniques called four-segment rectangular layout, the four perfect-matching current sources is achieved with two-level hierarchical topology at the expense of poor area efficiency. Second, a novel and compact layout technique based on the four-segment rectangular structure is developed to achieve perfect matching for four current sources. Both proposed layout technologies are verified by MATLAB simulations and readily extendable to the matching of even more current sources for future high performance analog IC applications. The authors would also like to thank National Chip Implementation Center (CIC) for test key fabrication and National Science Council for financial support under Grant NSC 94-2215-E-011-003.

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