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ΔΣ Modulation Based On-Chip Ramp Generator for ADC BIST

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Abstract: -Based on ΔΣ modulator, an on-chip analog ramp generator for ADC BIST (Built-in Self Test) is presented. Technique uses the over-sample and ΔΣ noise shaping to generate the on-chip precise analog ramp with the precise control of a calibrator of ramp slope. Moreover, because of over-sample and ΔΣ noise shaping, the design of analog circuits is simplified, and is tolerant to the mismatch of technology. Thus, the precision of the analog ramp generator is preserved. The analog ramp generator, which is implemented using a 0.18 μ m process from HJTC, has the 76dB SNR. It has wide output swing up to 1 voltage and maximum integral nonlinearity error (INL) of 190 μ V that is equivalent to 12 bits. The area overhead is 0.328mm ×0.276mm.

Key-Words: - ADC Self Test; Built-in-Self-Test; On-Chip Ramp Generator; ΔΣ Noise Shaping

1. Introduction

While the electronics control systems are becoming more and more complex, testing capabilities face challenges to follow the design evolution. Recent advance in IC design methods and manufacturing technologies allow designer to integrate the complete systems on a single chip. These so-called SoCs (System-on-Chips) improve the IC performances such as large bandwidth, high speed, low power consumption, and smaller volume and weight compared to their traditional multi-chip equivalents. However, these SoCs introduce new challenges to the test [1]. ADCs (Analog-to-Digital Converters) are one of the most frequently used in mixed-signal SoCs. Such mixed-signal IP (Intellectual Property) introduces more challenges to test SoC due to the nature of mixed signal. The insertion of DFT (Design-for-Testability) structures for IP blocks and effective techniques are needed in order to alleviate the test difficulties [1]. The BIST (Built-in Self Test) technique is effective for testing of on-chip ADCs because that it can offer a possibility of in-field verification and test besides improving testability [2-10]. Most of the proposed technique study designs that include both an ADC and a DAC (Digital-to-Analog Converters) [3, 4], or rely on the use of DSP or CPU capabilities to compute the characteristic parameters of ADC [5, 9]. Obviously, the chip area overhead is high unless the DAC, DSP or CPU can available or chip.

One of the most popular techniques used for testing of ADCs is the histogram test technique [6, 7, 10-12]. A complete BIST based on histogram scheme for ADCs requires a digital output response analyzer and a linear analog generator. Several techniques have been published to generate on-chip linear analog stimuli [2, 8, 9]. The basic ramp generator, which consists of a charging capacitor and a constant current, is frequently used. Because basic ramp generators are sensitive to circuit mismatch and process fluctuations, some calibration schemes make great efforts to achieve better linearity for basic linear ramp generators [2, 8]. The approach in scheme [9] uses a test stimulus generator composed of a pattern memory and a simple 1-bit DAC. The pattern memory holds a delta-sigma bit stream generated by a software model for the desired stimulus. The large amount bit-stream data required for high accuracy stimulus will result in large pattern memory size. Moreover, the measurements of DNL and INL are also implemented in software, and also rely the digital processing capabilities of CPU or DSP.

Considering hardware overhead and tolerance to analog variation, a linear ramp waveform generator based on digital delta-sigma modulator is discussed for ADC BIST based on linear histogram.

2 Linear Histogram-Based BIST Scheme

In ADC testing, a histogram shows how many times each different output code word appears in the response vector. These records are then compared with theoretical references (H_{ideal}) and comparison results are processed in order to determine the ADC parameters such as DNL, INL, offset and gain error [6, 7, 10-12]. The analog input signal can be any wave whose amplitude distribution is known. A linear (triangular or ramp) wave is usually as stimulus, as illustrated in Fig. 1.

Fig. 2 shows the structure of BIST based on linear histogram. The BIST structure is composed of main modules as below:

1. Output analyzer measures the outputs of an ADC under test to derive the DNL, INL, offset and gain errors.
2. On-chip analog generator provides the linear stimulus.

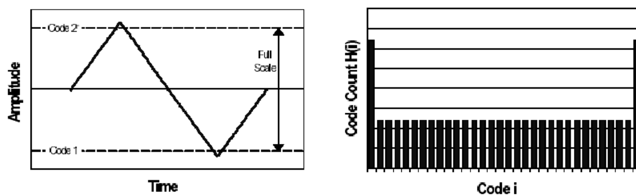


Fig. 1 The Ramp Signal in Linear Histogram and Ideal Output Histogram of ADC under Test

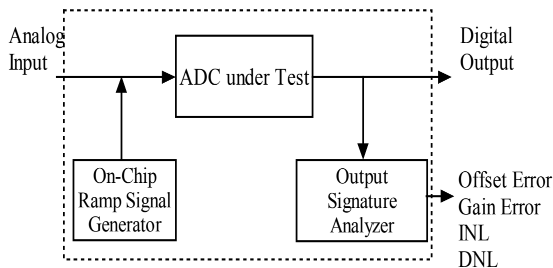


Fig. 2 General ADC BIST Scheme Based-on Linear Histogram

Because the analog generator will be fabricated on the same chip as the ADC under test, the silicon area of generator must be concerned. Another constraint concerns the quality of the test signal. The accuracy of the generator must be higher than one of the ADC under test.

3 On-chip Analog Generator

3.1 Structure of on-chip Analog Generator

The structure of on-chip analog Generator based on delta-sigma modulator is proposed as Fig. 3. It is composed of modules as below:

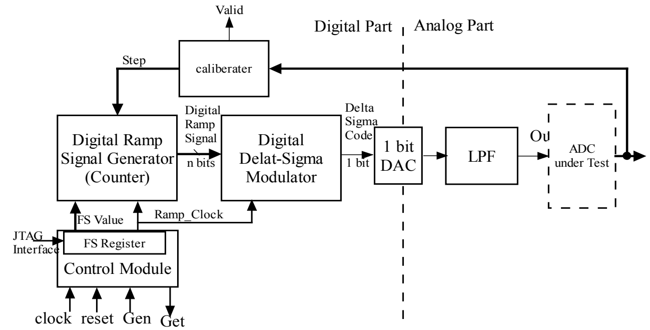


Fig. 3. Structure of On-Chip Analog Ramp Generator

1. *Control and interface module* provides the control of the generator and interface to JTAG [13]. Through JTAG interface, the full-scale value of ADC under test is shift to FS register. When GEN, which can also be activated through JTAG interface, is valid, the generator starts to generate linear stimulus. The GET signal generated by Control module identifies the valid linear portion of triangular waveform that covers the full-scale of the ADC under test.
2. *Counter* generates the linear digital signals as digital input patterns to a modulator according content of FS register. The bit-width of counter (n), which decides the precision of digital input to modulator, must be wide enough. But more bits will result in larger hardware overhead.
3. *Delta-sigma modulator* converts the n-bit digital pattern to 1-bit digital stream of delta-sigma for generating a linear stimulus.
4. *1-bit DAC* transfers the digital values to two discrete analog levels.
5. *Low-pass filter (LPF)* removes the out-of-band modulation noise and thus get linear analog waveform.
6. *Slope calibrator* controls the step length of the counter according total hits in the histogram of output codes of the ADC under the test. When the slope of ramp signal coincides with a required value, the *Valid* signal will be active.

3.2 Digital Delta-sigma Modulator

Delta-sigma modulators are commonly known as noise shaping that suppresses in-band noise to improve the resolution of modulator. For a k-order sigma-delta modulator, the ideal in-band SNR is a function of over sampling ratio (OSR), noise-shaping order (k) and quantizer resolution (m) [14].

$$SNR = \frac{3}{2}\left(\frac{2k+1}{\pi^{2k}}\right)\left(2^m - 1\right)^2 OSR^{2k+1} \quad (1)$$

Hence, the resolution of the modulator can be improved by increasing either the sampling rate or the order of the modulator. However, a modulator with an order greater than two becomes unstable and difficult to implement. The modulator's resolution can also be improved by using multi-bit quantization. However, multi-bit quantization will require a multi-bit DAC. A 1-bit DAC modulator has a quantizer with only on decision level. The implementation of the 1-bit DAC is easy and highly linear. The second-order single-bit delta-sigma modulator we used is illustrated in Fig. 4.

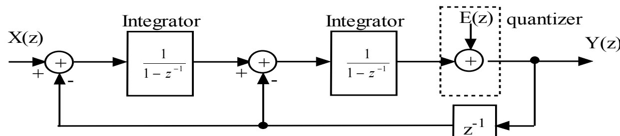


Fig. 4. 2nd-order Δ∑ Modulator

The OSR of modulator will be assign as high as possible. Finally, The second-order single-bit delta-sigma modulator with 100MHz sampling rate will be used. The scheme is implemented using a 0.18μm process from HJTC.

3.3 1-bit DAC

The 1-bit DAC can be as simple as a buffer or a more complex circuit between the digital logic and the analog filter. The circuits presented in this paper use a simple voltage buffer.

3.4 Low-pass Filter

A majority of frequency components of the quantization noise have been removed to high frequency domain far away from signal band. Thus, the simple first-order active low pass filter is suitable to remove the out-of-band modulation noise. A wide-swing operational amplifier, as shown in Fig. 5, is used in the filter in order to get wide swing at output.

3.5 Slope Calibrator

The process fluctuations and devices mismatch will

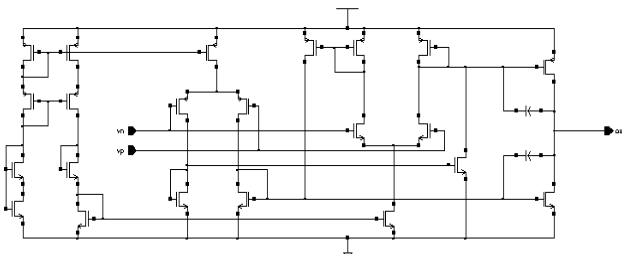


Fig. 5. Wide Swing Operation Amplifier

affect the precision and slope of the ramp signal. Moreover, in ADC BIST scheme based on linear histogram, we hope the histogram data of each code is power of 2, i.e. $H_{ideal}=2^p$ so that divisions of the calculation of the DNL and INL can be equivalent to shift operations in the register [6, 7, 10]. Thus, we collect the histogram of total hits of codes from 1 to 2^N-2 for N-bit ADC. The extreme code 0 and code 2^n-1 are discarded because these histogram have no outer bound. Then the collected histogram data (S) will be compared with required value (S_{ideal}) to calibrate the step length of the counter.

$$S = \sum_{i=1}^{2^N-2} H[i] \equiv (2^N - 2)\overline{H} \quad (2)$$

Here, *H[i]* is histogram of code i.

$$S_{ideal} = \sum_{i=1}^{2^N-2} H_{ideal}[i] = (2^N - 2)H_{ideal} \quad (3)$$

Here, $H_{ideal}[i]$ is required ideal histogram of code i.

According difference of real histogram S and required ideal histogram S_{ideal}, change the step length from 1 to step[n]. As a result, the new histogram S comes out.

Ideally,

$$S[n+1] = \frac{S[n]}{step[n]} \quad (4)$$

Here, S[n] is nth histogram statistics.

Choosing $S[n+1] = S_{ideal}$, we can derive the step[n] and get required the *S* directly. But as mentioned above, the process fluctuations will affect the analog circuits and result in $S[n+1] \neq S_{ideal}$, so we use the multi-calibration as below,

$$step[0] = 1,$$

$$step[n] = \frac{S[n]}{S_{ideal}} + step[n-1] - step[0] \quad (5)$$

$$n = 1, 2, ...$$

4 Results and Evaluation

The digital portion of on-chip analog generator is described by verilog hardware description language, and implemented using top-down design methodology. The analog portion is implemented using full-custom methodology. The on-chip analog generator is implemented using a 0.18μm process from HJTC. The layout of it is shown in Fig. 6. Dimensions are 0.328 × 0.276mm^2. The digital portion of the generator occupies only the chip area of 0.0254 mm^2.

Fig. 7 shows the frequency domain response when the Delta-sigma modulator is applied the sine wave with 4.578kHz. We can find that the in-band quantization noise has been reduced. Thus, we can use the low pass filter to suppress noise to improve

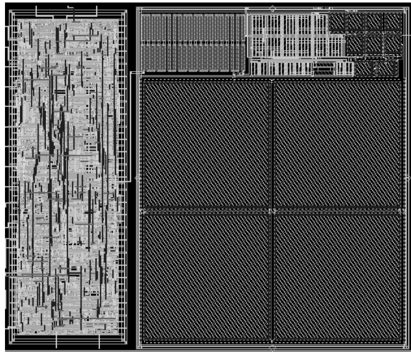


Fig 6 Layout of the Generator

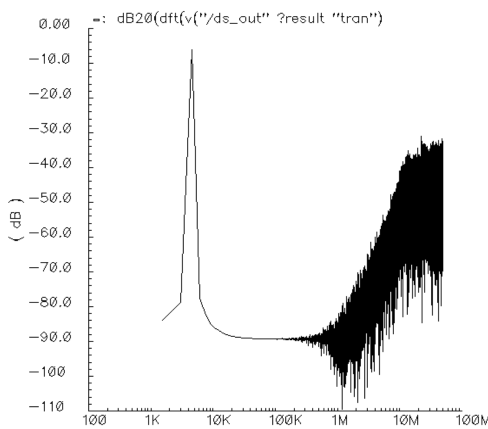


Fig. 7 Output Spectrum of Δ∑ Modulator

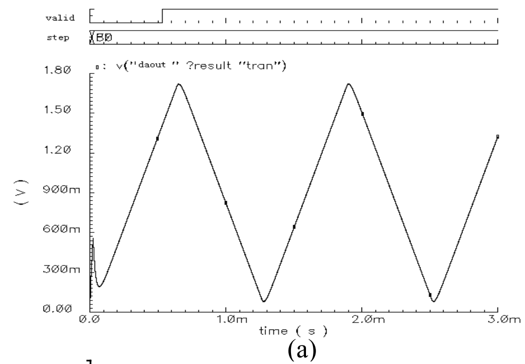
the resolution. The SNR in band is about 76dB.

Fig. 8 (a) (b)shows the waveform and INL of generator's output. The linear ramp portion of output goes from 0.4 to 1.4V. The ramp maximum INL is $\pm 190\mu V$. Fig. 8 (c) shows the calibration process when the required $\overline{H}$ changes from 128 to 256.

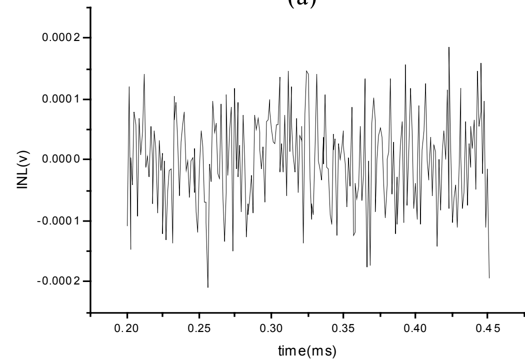
The table 1 shows the comparison results among this paper, Benoit et al [2] and Huang [9]. We implement the linear generator in the scheme of Huang by 0.18 μ m process from HJTC for the purpose of a comparison of hardware overhead. It can be find that the analog generator of this paper occupies less chip area and provide higher output swing and precision.

5 Conclusion

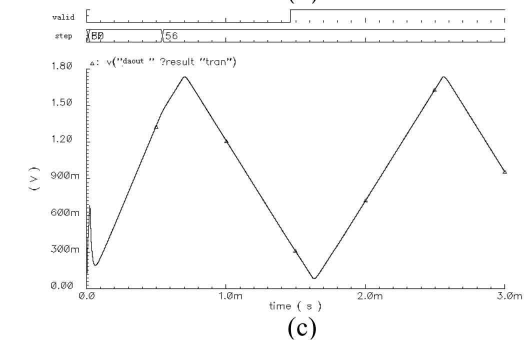
Based on digital delta sigma modulator, the on-chip analog generator dedicated to the test of ADC using a linear histogram is developed. Moreover, with the precise control of the calibrator, the generator can deal with process fluctuations and mismatches of devices and keep the required slope of ramp. The on-chip analog generator is implemented using a 0.18 μ m process from HJTC. It has wide output swing up



(a)



(b)



(c)

Fig 8 On-Chip Analog Ramp Generator
(a) Output (b) INL (c) Output under Calibration

to 1V and maximum INL of 190 μ V. The area overhead is 0.328mm ×0.276mm.

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Table 1 Performance and Comparison of On-Chip Analog Ramp Generator

Name	Output Swing (of percent of power)	Integral Nonlinearity (INL)	Equivalent bits	Technology （Power Supply）	Area Overhead	Analog Or Digital
Benoit et.al [2]	0.6V (0.6V/1.8V=33%)	Max.：190μV Min：150μV Average：170μV	11bits	TI 0.18μm （1.8V）	0.3 ×0.6㎟＝0.18 ㎟	Analog
Jiun-Lang Huang [9]	3V (3V/5/V=60%)	Max. 570μV	12bits	-	2^{14}×1bit RAM +1DAC+LPF (0.269 mm^2 @ 0.18μm Hjtc)	Mixed signal
This paper	1V (1V/1.8V=56%)	Max.190μV	12bits	Hjtc 0.18μm （1.8V）	0.328 ×0.276㎟＝ 0.090528 ㎟	Mixed Signal

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