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# Some Insight Into The Implemenattion Of A Trans-Impedance Amplifier In CMOS Technology Using Two-Port Network Parameters

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*Abstract:*This article proposes a two-port network theoretic approach towards implementation of a trans-impedance amplifier (TIA) using a given (i.e. CMOS) VLSI technological process. Several existing TIA structures are reviewed regarding their respective compliance with the basic equivalent circuit model of a TIA. It is shown how the z-matrix paarmeters of the system can be exploited to obtain several desirable characteristics of a TIA. A new approach towards maximizing the gain-bandwidth of a TIA is presented.

*Key- Words:* Transimpedance amplifier, two-port z-parameters, gain-bandwidth optimization, use of negative resistances.

## 1. Introduction

Trans-impedance amplifier (TIA) networks implemented using CMOS VLSI technology are being utilized as the front end in various wide band communication systems [1] -[3]. The principal motivations are realization of very high gain-bandwidth with low input and output impedances. To the best of knowledge of the author, analysis and implementation of a TIA conforming to the basic equivalent circuit model has not been reported yet. The reason for this assertion lies in the fact that many of the TIA networks, reported so far, use shunt shunt feedback, which invariably produce a finite value of the reverse transimpedance thus failing to comply with the equivalent circuit model of a basic TIA. On the other hand an approach using the Z parameters could lead to judicial choice of the circuit parameters to arrive at an optimum design of the system.

Towards this, section 2 of this article establishes several characteristics of a TIA based on the elements of its associated Z-matrix parameters. In section 3, several known TIA structures are examined with regard to their respective compliance with the two-port Z-matrix model of a basic TIA network. In section 4 we present some ideas to improve the characteristics of a TIA by manipulating the z-parameters. Section 5 provides analysis and discussion regarding maximizing the gain-bandwidth value of the TIA networks. Section 6 presents simulation results validating the conclusions arrived at in sections 4 and 5. MOS transistors in 0.18 micro-meter (μm) CMOS VLSI process have been used for this study. Section 7 concludes the article by highlighting the important contributions.

## 2. TIA and Two-Port Z-Paremeters

Figure 1(a) shows the basic equivalent circuit model of a TIA [4]. Figure 1(b) shows the impedance (i.e., z-parameter) model of a two port network. Any practical TIA system can be easily related to the model of figure 1(b). It is easily recognized that for a practical TIA to conform to the basic model (Fig.1(a)), one must ensure $Z_{11} \rightarrow R_{in}$, $Z_{21} \rightarrow R_m$, $Z_{22} \rightarrow R_{out}$ , and $Z_{12} \rightarrow 0$. For a terminated model of a TIA, shown in figure 2, we can derive that:

$$Z_{in} = \frac{v_i}{i_{in}} = z_{11} - \frac{z_{12}z_{21}}{z_{22} + z_L} \qquad (1)$$

$$Z_{out} = \frac{v_o}{i_{out}} = z_{22} - \frac{z_{12}z_{21}}{z_{11} + z_s} \qquad (2)$$

$$Z_T = \frac{v_o}{i_s} = \frac{z_{21}}{(1+\frac{z_{11}}{z_s})(1+\frac{z_{22}}{z_L}) - \frac{z_{12}z_{21}}{z_s z_L}} \qquad (3)$$

The reverse trans-impedance parameter $z_{12}$ provides a feedback effect. If this can be eliminated, the two-port model will conform closer with the basic CCVS model as in Figure 1(a). When this is not possible, we can try to adjust this parameter to make the TIA offer an improved performance in several respects. These considerations are discussed below.

### 2.1 Input impedance matching

We shall assume that zero reflection condition ensures impedance match at the input port. It is welknown that for high frequency system, zero reflection is necessary for maximizing power transfer at the input. This is possible by having $Z_{in}=z_s$. This leads to (using eq.1)

$$z_{12} = \frac{(z_{11} - z_s)(z_{22} + z_L)}{z_{21}} \quad \ldots (4)$$

If we arrange $z_{11}=z_s$, we shall get $z_{12}=0$, and $Z_{in}=z_{11}$ (from eq.1)$=z_s$ (from eq.4a), producing zero reflection coefficient. Thus having $z_{12}=0$ facilitates achieving input matching condition by the simple arrangement of $z_{11}=z_s$.

### 2.2 Output impedance matching

For zero reflection at the output port, we should have $Z_{out}=z_L$. This leads to (using eq.2)

$$z_{12} = \frac{(z_{22} - R_L)(z_{11} + z_s)}{z_{21}} \quad \ldots (5)$$

It follows, as above, that achieving $z_{22}=R_L$ will lead to $z_{12}$=0, and $Z_{out}=z_{22}=z_L$ . Thus having $z_{12}=0$ facilitates achieving output matching condition by the simple arrangement of $z_{22}=z_L$.. It is clear that $z_{12}=0$ opens up the possibility of achieving input and output matching indpendently.

### 2.3 Optimizing the system gain $Z_T$

Using eq.3, we find that

$$z_{12} = \frac{(z_s + z_{11})(z_L + z_{22})}{z_{21}} \quad \ldots (6)$$

will lead to $Z_T \rightarrow \infty$. It may be remarked that a more important system parameter is, however, the gain-bandwidth of the system. An infinite value of $Z_T$ does not necessarily lead to infinite gain-bandwidth value. This is clarified below.

### 2.4 Gain-bandwidth of the system

If we assume that the frequency response of the two port network is determined only by the capacitive loading at the two terminals, and that $C_s$ and $C_L$ are these capacitors, we could write $\frac{1}{z_s} = g_s + sC_s$, and $\frac{1}{z_L} = g_L + sC_L$. Similarly, we shall assume that all the two-port impedance parameters are resistive only. Then we have (from eq.3)

$$Z_T = \frac{r_{21}}{\{[1 + r_{11}(g_s + sC_s)][1 + r_{22}(g_L + sC_L)] - r_{12}r_{21}(g_s + sC_s)(g_L + sC_L)\}} \quad \ldots (7)$$

If the two capacitors have widely different values, the one with higher values will affect the band-width of the system. If $C_S >> C_L$, the system can be regarded as a one-pole system with the pole

$$s = -\frac{1 + g_L r_{22} + g_s r_{11} + g_s g_L r_{11} r_{22} - r_{12} r_{21} g_s g_L}{C_S(r_{11} + r_{11} r_{22} g_L - r_{12} r_{21} g_L)} \quad \ldots (8)$$

If $r_{12}$ =0, as in the basic model of a TIA (fig.1(a)), the pole will remain in the left half of S-plane and the system will be stable. If, however, $r_{12}$ is not zero, the pole may fall on the right half of the S-plane and the sytem will potentially be unstable. To convince ourselves, we can choose

$$r_{11} = 50\Omega,\ r_{22} = 50\Omega,\ g_s = 10^{-4} mho,$$
$$g_L = (50)^{-1} mho,\ r_{21} = 100\Omega$$

If we set $r_{12}$= 59Ω, we shall get $s$=+.11. This represents an unstable system. On the other hand if $r_{12}$=0.1Ω, we shall get $s$=-0.02. This corresponds to a stable system. Similar calculations can be done with the assumption of $C_L >> C_S$.

We have thus established that a unidirectional characteristic of a TIA is required ( i.e., $z_{12}$=0 ) to avoid potential instability. *This information came to light by considering the two-port impedance parameters* model of the TIA. This has not been done by previous researchers.

The denominator of eq.7 can be expanded into a second degree polynomial in $s$ and is given by:

$$D(s) = -C_s C_L (r_{11} r_{22} - r_{12} r_{21}) s^2 + (r_{11} C_s + r_{11} g_s r_{22} C_L + r_{22} C_L + r_{11} C_s r_{22} g_L - r_{12} r_{21} g_L C_s - r_{12} r_{21} g_s C_L) s + 1 + r_{22} g_L - r_{12} r_{21} g_s g_L + r_{11} g_s + r_{11} r_{22} g_s g_L$$

The dominant pole of the system is given by:

$$\omega_p = \frac{1 + r_{22} g_L - r_{12} r_{21} g_s g_L + r_{11} g_s + r_{11} r_{22} g_s g_L}{r_{11} C_s + r_{11} g_s r_{22} C_L + r_{22} C_L + r_{11} C_s r_{22} g_L - r_{12} r_{21} g_L C_s - r_{12} r_{21} g_s C_L} \quad \ldots (9)$$

The gain-bandwidth of the system can be expressed as $Z_T(0).\omega_p$. This is (form eqs. 7,9)

$$GBW = \frac{r_{21}}{(r_{11} C_s + r_{11} g_s r_{22} C_L + r_{22} C_L + r_{11} C_s r_{22} g_L - r_{12} r_{21} g_L C_s - r_{12} r_{21} g_s C_L)} \ldots \quad (10)$$

The above equation reveals a potential to make $GBW \rightarrow$ infinity by arranging

$$r_{12} = \frac{r_{11}C_s + r_{22}C_L + r_{11}r_{22}(C_s g_L + C_L g_s)}{r_{21}(g_L C_s + g_s C_L)}$$

… (11)

However, one has to carefully evaluate the situation in a practical system for physical realizability of this solution.

### 2.5 Ideal input and output conditions

In 2.1,2.2 above we have considered matching condtions at input and output with radio frequency signal conditions. So far compliance with the basic model of a TIA is concerned, however, the ideal conditions are: $z_{12} = 0$, $Z_{in} \to 0$, and $Z_{out} \to 0$. These will lead to the following alternative realtions (from eqs. 1,2)

$$z_{11} = 0,\ z_{22} = 0 \text{ if } z_{12} = 0 \quad ..(12)$$

Or (if $z_{12}$ is not =0),

$$z_{12} = \frac{z_{11}(z_{22} + z_L)}{z_{21}} \text{ for } Z_{in} \to 0, \quad \ldots(13a)$$

$$z_{12} = \frac{z_{22}(z_{11} + z_s)}{z_{21}} \text{ for } Z_{out} \to 0 \quad \ldots(13b)$$

## 3. Analysis of Several TIA structures

The basic structure of a TIA is a CCVS i.e., a low resistance at the input, a low resiatnce at the output and a high transimpedance gain $R_m(\sim z_{21})$. Research on TIA has been continuing for almost last two decades. We have considered several TIA structures, which employ minimal number of devices and discrete components to realize the basic TIA function. These are: (a) Common-source in, common-drain out (CS-CD) TIA with resistive shunt-feedback [1], (b) Common-drain input and output (CD-CD) TIA with resistive shunt-feedback [2], (c) Common-gate in, common-drain out (CG-CD) with resistive shunt-feedback [3] ,(d) Regulated Cascode input, common-drain output (RGC-CD) [4], and (e) Cascaded inverters TIA (INV-INV) with resistive shunt-feedback [5]

Using low-frequency (~DC) small signal equivalent model for a MOS transistor we have analyzed the above TIA circuits. All the TIA networks except the RGC-CD architecture have non-zero reverse trans-impedance, i.e., $z_{12}$ is not zero. Thus the RGC-CD architecture complies with the basic model of a TIA. Of the other four structures, the CS-CD structure has a $z_{12}$ which does not depend upon the feedback resistance $R_f$. In the CD-CD, CG-CD, and INV-INV structures $z_{12}$ is dependent upon the feedback resistance $R_f$. Thus one could eliminate the resistance $R_f$ in these TIA networks rendering $z_{12}$ =0 (since $g_f$ =0). This could facilitate impedance matching at the input and at the output. Also it would remove the potential instability problem for the TIA. However, calculations show that the transimpedance $z_{21}$ in these networks depend upon $g_f$ as well. So $z_{12}$ cannot be adjusted independent of other z-parameters of the system. To conserve space, we shall discuss the case of only the CG-CD TIA (figure 3) now on and present our work.

For this TIA, the $z_{12}$ is given by $\frac{g_f(g_1 + g_{d1})}{\Delta_3}$, where

$$\Delta_3 = (g_{m1} + g_{mb1} + g_i + g_f + g_{d1})(g_1 + g_{d1})(g_{m2} + g_{mb2} + g_o + g_f + g_{d2}) - (g_{m1} + g_{mb1} + g_{d1}) \times \{g_f g_{m2} + g_{d1}(g_{m2} + g_{mb2} + g_o + g_f + g_{d2})\} - g_f{}^2(g_1 + g_{d1}) \quad ..(14)$$

and $g_x = 1/r_x, 1/R_x$, all $x$.

## 4. Improving the TIA characteristics

In this section we shall investigate the possibilities of attaining the desirable characteristics as discussed in section 2 above.

### 4.1 Matching at input or at output

Both of the above cases can be satisfied by having $z_{12}$=0, with either $z_{11}$=$z_s$ (for input matching), and $z_{22}$=$z_L$ ( for output matching). For the CG-CD TIA, this is achieved if $g_f$ =0 , or $g_1$=-$g_{d1}$.

### 4.2 Optimization of the gain-bandwidth

We can use eq. (11) and solve for the designable components in each of the TIA to get the optimum solution. This approach, however, assumes that only the input and output capacitances ($C_s$, $C_L$) are the determining factors for the dominant pole of the system, and that all the two-port impedance parameters are resistive only. In Table 1 we provide solutions applicable to the CG-CD TIA.

In a practical system, there will be internal nodes which would be effective for producing the dominant pole. So the gain-bandwidth should be calculated for each specific network and a search should be made for arriving at the optimum the value. This is discussed in section 5 of this article.

It may be noted that the solutions require negative valued resistances. These cannot be realized using passive components. However, negative resistances using MOS transistors have

been reported [6]-[8] in the literature. These could be employed for our purpose.

### 4.3 Ideal input and output impedance conditions

Table 2 presents solutions for this case for the CG-CD TIA network. The solutions correspond to eqs. 12 and 13(a)-(b) in *section 2* above.When a single solution meets all the three criteria, only that solution is shown in the Table. Again negative valued resistances are required to achieve the ideal impedance conditions.

## 5. Maximizing the transimpedance gain band-width product (GBW) value

In this section we shall consider a technique of optimizing (maximizing) the gain band-width (GBW) value [9]. We shall illustrate the technique with the CG-CD TIA.

We shall use the principle of open circuit time-constant method, so that the analysis remains simple and the results can be interpreted easily. Accordingly, the objective function to be optimized will be of the form $\frac{Z_T(0)}{R_x}$, where $R_x$ is the time-constant resistance associated with the parasitic capacitance $C_x$ at a given node (say, $x$) producing a pole frequency $\omega_x = \frac{1}{C_x R_x}$. The function $\frac{Z_T(0)}{R_x}$ may be considered as the gain bandwidth (GBW) value per unit node capacitance. For a TIA on hand, $Z_T(0)$ will be fixed, but $R_x$ will change depending upon the location of the node. So we have to evaluate all the $R_x$ values associated with different nodes of the system. It may be remarked that the GBW expression must be a nonlinear function [10] of a designable electrical parameter, so that an optimum result can be calculated in practice.

### 5.1 Example case

The ac equivalent circuit for the CG-CD TIA is shown in Fig. 4. In this we have lumped common node capacitances together as $C_1 = C_s + C_{bs1} + C_{gs1}$, $C_2 = C_{gd1} + C_{db1}$, $C_3 = C_{gb2} + C_{gd2}$, $C_{23} = C_2 + C_3$, $C_4 = C_{bs2} + C_L$. $C_s$ is the capacitance at the source end while $C_L$ is the capacitance at the load end. Further, we have $R_i'$ and $R_o'$ represent parallel combinations of $R_s$, $R_i$, and $R_o$, $R_L$ respectively. The time-constant (TC) resistance ($R_{Th1}$) for $C_1$ will be $v_1/i_s$, since $C_1$ is connected at node 1. Similarly, the TC resistance ($R_{Th2}$) for $C_{23}$ will be $v_2/i_s$, with $i_s$ placed across ground and node 2. The TC resistance ($R_{Th32}$) for $C_{gs2}$ will be $(v_3-v_2)/i_s$, with $i_s$ placed across nodes 2 and 3, and so on. It may be remarked that the time constant $R_{Th3}C_{gs2}$ will pertain to a zero of the overall transimpedance function $v_3/i_s$. Thus it will not be considered for optimizing the GBW of the TIA under consideration. The above Thevenin resistances and the system gain at low frequency (~DC) $Z_T(0)$ can be calculated using Krammer's rule in matrix analysis. Setting up the nodal matrix and using the following substitutions

$$\begin{aligned} x &= g_1 + g_{d1} \\ y &= g_{m1} + g_{mb1} = g_{m2} + g_{mb2} \\ z_1 &= g_i + g_{d1} + g_s \\ z_2 &= g_o + g_{d2} + g_L \end{aligned} \quad \ldots (15)$$

We can write:

$$\begin{aligned} Z_T(0) &= \frac{g_{m2}(y + g_{d1}) + g_f x}{\Delta_3'} \\ R_{Th1} &= \frac{x(y + z_2 + g_f)}{\Delta_3'} \\ R_{Th2} &= \frac{(y + g_f + z_1)(y + g_f + z_2) - g_f^{\,2}}{\Delta_3'} \\ R_{Th3} &= \frac{x(y + g_f + z_1) - g_{d1}(y + g_{d1})}{\Delta_3'} \end{aligned} \quad \ldots (16)$$

In the above $\Delta_3'$ is the determinant of the nodal admittance matrix and is given by:

$$\begin{aligned} \Delta_3' = {} & (g_{m1} + g_{mb1} + g_i + g_s + g_f + g_{d1})(g_1 + g_{d1})(g_{m2} + g_{mb2} + g_o + g_L + g_f + g_{d2}) \\ & -(g_{m1} + g_{mb1} + g_{d1})\{g_f g_{m2} + g_{d1}(g_{m2} + g_{mb2} + g_o + g_L + g_f + g_{d2})\} - g_f^{\,2}(g_1 + g_{d1}) \end{aligned} \quad \ldots (17)$$

Following the guidelines in [10], we can figure out that only the ratio $Z_T(0)/R_{Th2}$ is a candidate for analytic optimization. Specifically, we can cast this ratio to the form:

$$GBW(y) = \frac{ay + b}{y^2 + cy + d} \quad \ldots (18)$$

If a real solution exists for $y = g_{m1} + g_{mb1} = g_{m2} + g_{mb2}$, and if these parameters can be designed for the MOS transistors at hand, the TIA can be designed for a maximum GBW (per unit capacitance). It must be understood that the absolute value of the maximum GBW will be dependent upon the actual value of the parasitic capacitance at node 2. If this capacitance is very large compared with the capacitances at other nodes (i.e., nodes 1 and 3 here) the optimum

(maximum) value obtained will not be very attractive for practical purposes. All that we have demonstrated here is that the pole frequency associated with $R_{Th2}$ is optimizable by hand analysis.

# 6. Simulation Results

### 6.1 Validation of the results in section 4

In this section we shall present results obtained by HSPICE simulations and MATLAB calculationsto validate the calculations presented *section 4* above. Using a 0.18 micron CMOS process for the CG-CD TIA, we obtained the following data:

$$g_{m1} = 2.68m\ mho,\ g_{mb1} = 0.632m\ mho,\ g_{d1} = 362\mu\ mho$$
$$g_{m2} = 10.2m\ mho,\ g_{mb2} = 2.21m\ mho,\ g_{d2} = 1.38m\ mho$$
$$R_s = 10k\Omega = R_f,\ R_i = R_L = R_o = 50\Omega,\ R_1 = 4000\Omega$$

Table 3 presents the necessary (small signal) values of some of the design resistances in order to satisfy the conditions as shown in Tables 1 and 2. These are obtained using $C_s$=1pf and $C_L$=0.2pf.

The negative resistance networks reported in [6]-[8] have been simulated by HSPICE and it has been found that input resistance values between -2.77 kΩ to -10.3 kΩ can be obtained. These limits encompass the range of negative values required for $R_1$ in Table 3.

The values in Table 3 have been used in the equivalent circuit (with $C_1$=1pf, $C_4$=0.2pf, $C_{23}$, $C_{gs2}$=0) of Fig.4 to validate the theoretical predictions regarding $R_{in}$, $R_{out}$ and the GBW values. Table 4 present the results from HSPICE simulations. The optimum values are shown in bold face letters.

### 6.2 Validation of the results in section 5

The CG-CD TIA using MOS transistors produced a GBW of 95.2 G-ohms with a power consumtion of only 2.6 mW from ±1.5 V suply system. Using the optimization procedure, the GBW increased to 300 G-ohms. This is an improvement by a factor of 3.15 with an attendant increase in power consumption of only 3.4 mW. These results are better than the result reported in [11], where an increase of only 2.4 times was obtained after inductive bandwidth enhancement technique at a hepty power consumption of 137 mW! The GBW available with this power cosumption is, however, higher, i.e., 4611 G-ohms.

# 7. Conclusion

In this article a new viewpoint towards implementation of a TIA has been presented. This involves comparing the two-port impedance matrix description of a network with the small signal model associated with a basic TIA. Many TIA networks reported in the past have not considered this view point. Our two-port network theoretic study brought out several information which remained in the background so far. Thus it was revealed that many TIAs reported so far do not satisfy the unidirectional characteristics of the basic TIA (i.e., $z_{12}$=0). We could show that for non-zero reverse trans-impedance ($z_{12}$), judicious choice must be made to ensure stability. However, non-zero $z_{12}$ could be exploited to render $R_{in}$ (or $R_{out}$) to zero and/or achieve very large gain-bandwidth values. Analyses using the two-port parameters pointed out the necessity of negative valued resistances for achieving theoretical infinite gain-bandwidth or zero input/output impedance. This is also a new information in the domain of TIA implementation. The network function approach used in this article has also opened a new avenue to optimize the performance of the TIA. For lack of space, some of the results of analyses have been validated by considering a typical CG-CD TIA network implemented using TSMC 0.18um CMOS technology.We are confident that the approach suggested in this article will facilitate alternative implementation method of TIA networks with acceptable characteristics.

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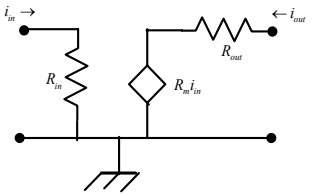


Figure 1(a) Equivalent circuit for basic TIA

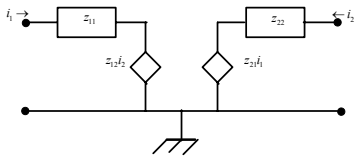


Figure 1(b) Z-parameters model of a TIA

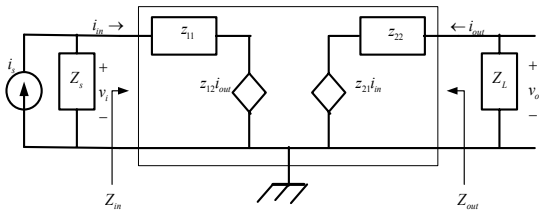


Figure 2: Z-parameter model of a TIA with terminations

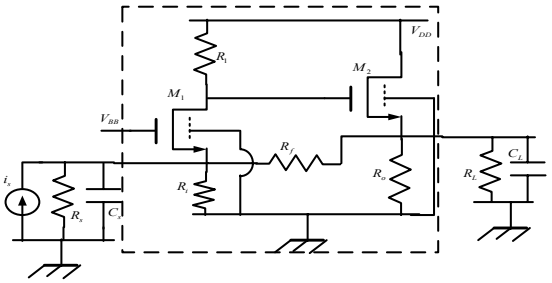


Figure 3: CG-CD TIA

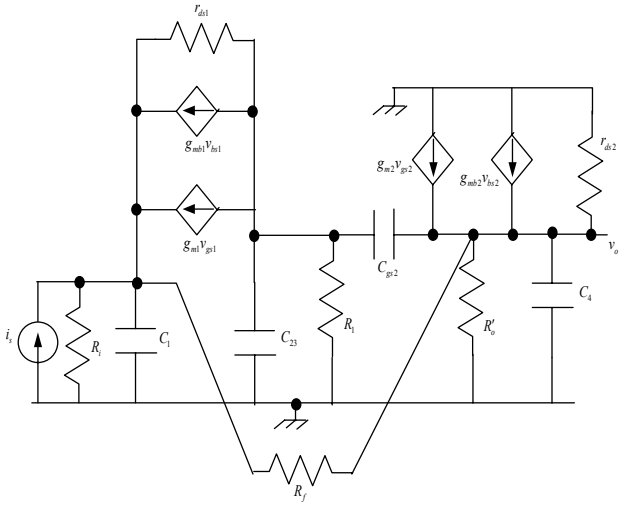


Figure 4: AC equivalent circuit for CG-CD TIA

**Table 1(**GBW → infinity condition, CG-CD TIA**)**

(note: $X = g_L C_s + g_s C_L$)

| $g_1$ | $g_f$ | $g_o$ |
|---|---|---|
| $-\frac{g_{d1}[C_s(g_{d2}+g_{mb2}+g_o+g_{m2}+g_f)+C_L(g_f+g_i)+X]}{[C_s(g_{m2}+g_{mb2}+g_{d2}+g_o+g_f)+C_L(g_{m1}+g_f+g_{d1}+g_i)+X]}$ | $-\frac{[C_s(g_1g_{mb2}+g_{d1}g_{mb2}+g_og_1+g_{m2}g_1+g_1g_{d2}+g_{d1}g_{d2}+g_{d1}g_o+g_{d1}g_{m2})+C_L(g_1g_{mb1}+g_{m1}g_1+g_1g_{d1}+g_ig_1+g_ig_{d1})+X(g_1+g_{d1})]}{(C_s+C_L)(g_1+g_{d1})}$ | $-\frac{[C_s(g_1g_{mb2}+g_{d1}g_{mb2}+g_{m2}g_1+g_fg_1+g_1g_{d2}+g_{d1}g_{d2}+g_{d1}g_f+g_{d1}g_{m2})+C_L(g_1g_{mb1}+g_{m1}g_1+g_1g_{d1}+g_1g_f+g_ig_1+g_{d1}g_f+g_ig_{d1})+X(g_1+g_{d1})]}{C_s(g_1+g_{d1})}$ |

**Table 2 (**Ideal input, output resistances**)**

| $g_1$ | $g_f$ | $g_o$ |
|---|---|---|
| $-g_{d1}$ (2)<br>$-\frac{g_{d1}[z_s(g_i+g_f)+1]}{z_s(g_{m1}+g_{mb1}+g_f+g_i+g_{d1})+1}$ (3) | $-\frac{1+z_L(g_{m2}+g_{mb2}+g_{d2}+g_o)}{z_L}$ (2)<br>$-\frac{1}{z_s(g_1+g_{d1})}[z_s(g_1g_{mb1}+g_1g_{d1}+g_{m1}g_1+g_ig_1+g_ig_{d1})+g_1+g_{d1}]$ (3) | $-\frac{z_L(g_{m2}+g_{mb2}+g_f+g_{d2})+1}{z_L}$ (2) |

(1) condition in eq. 12 satisfied, (2) $Z_{in}$→0 in eq.13(a) satisfied, (3) $Z_{out}$→0 in eq.13(b) satisfied

**Table 3**

| **Condition** | $R_1$ = ,or | $R_f$ = , or | $R_o$ |
|---|---|---|---|
| $Z_{in}$ → 0 | -2762 | -18.6 | -29.5 |
| $Z_{out}$→0 | -3265 | -46.4 | |
| GBW→ infinity | -2791 | -21 | -26 |

**Table 4** (Validation of theoretical results)

| Resistance | Values in ohms | GBW in Giga (Ω-radians/s) | $R_{in}$ ohms | $R_{out}$ ohms |
|---|---|---|---|---|
| $R_1$ | 4000 | 179.7 | 46.5 | 18.6 |
| | **-2762**, -2700, -2800 | | **81µ**, 5.2, 3.83 | |
| | **-3265**, -3200,- 3350 | | | **1.04**, 12.73, 30.19 |
| | **-2791**, -2600, -3000 | **1285**, 1176, 1241 | | |
| $R_o$ | 50 | 179.7 | 46.5 | 18.6 |
| | **-29.5**, -31, -27 | | **2.62**, 56, 42.5 | |
| | **-26**, -24, -22 | **1434**, 1032, 753.82 | | |
| | | | | |