

## Organization of a circuit simulator based on waveform – relaxation method

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*Abstract:* The waveform-relaxation method is an iterative method for analysis of nonlinear dynamical system. Two waveform-relaxation algorithms i.e., Gauss-Seidel(GS) and Gauss-Jacobi(GJ) algorithms are presented for analysis of dynamical system. Then organization of a waveform-relaxation circuit simulator is described.

*Keywords:* Waveform relaxation methods , Circuit simulator , Gauss-Seidel algorithm, Gauss-Jacobi algorithm, Nonlinear circuits.

### 1 Introduction

Electrical circuit simulation was one of the first CAD tools developed for IC design. Circuit simulators provide precise information such as frequency response, time domain waveforms and sensitivity information.

The conventional circuit simulators like SPICE and ASTAP were designed initially for the cost-effective analysis of circuits containing a few hundred transistors or less. A number of approaches have been used to improve the performance of conventional circuit simulators for the analysis of large circuits.

Recently, relaxation methods have been proposed [1] – [2] to provide accurate or more accurate waveforms than standard circuit simulators with upto two orders of magnitude speed improvement for large circuits. These methods attempted to exploit not only spatial sparsity but also the temporal sparsity and the unidirectional nature of MOS digital circuits. We describe the waveform relaxation simulator.

The Conventional circuit simulation tools such a SPICE and STAP apply kirchoffs current and voltage laws to the topology and branch relations of a circuit to derive a set of nonlinear differential equations describing the circuit behaviour. These equations are then transformed into a set of nonlinear algebraic equations through the use of an integration method. In general,such integration methods are of the implicit multistep type.Among the most commonly used techniques are the

backward-Euler, trapezoidal-rule. The resulting algebraic equations are then linearized and solved over a user specified analysis interval. Linearization is performed by application of the iterative Newton-Raphson method. Once linearized, the set of algebraic equation is usually solved by LU decomposition with sparse matrix techniques. At the start of the circuit analysis, all of the network equations are solved iteratively at the first time point until the differences between two successive iteration is sufficiently small i.e., the solution converges. Once convergence is achieved at the first point, a time step is calculated to determine the next time point. The size of the time step is determined by the difficulty encountered in solving the circuit at the current i.e., the first time point. The iterative solution process is repeated at the next time point and at all successive time points, until the stop time is reached. With such a scheme, once the stop time is reached, the circuit waveforms (the calculated voltages at all time points for all voltage nodes) are known for the entire analysis interval, and the simulation is complete.

### 2 Mathematical Formulation of WR Algorithms

Although the conventional method produce an accurate prediction of circuit behavior, it suffers several performance problems as the size of the analysed circuits increases. First, since all circuit equations are solved at the same time points, and each time point is determined on the basis of the

difficulty in converging at the previous time points, the entire system of equations is solved using time steps determined by the most difficult set of equations. This causes the entire system of equations to be solved repeatedly even when only a small part of the circuit is converging slowly. Second, as the size of the circuit grows, the time required to solve the set of equations grows nonlinearly. The growth factor is generally acknowledged to be proportional to  $N^\alpha$ , where  $N$  is the order of the matrix of linear equations ( $N$  is generally proportional to the number of voltage nodes contained in the circuit), and  $\alpha$  is between 1.4 and 1.6 [3]. So, not only are conventional methods constrained to solve the circuit equations repeatedly on the basis of the most slowly converging part of the circuit, but also the time required to solve those equations grows dramatically with circuit size.

Unlike conventional methods, waveform-relaxation methods do not attempt to solve the complete set of equations for a circuit simultaneously. Instead, large MOS circuits are algorithmically partitioned into interconnected subcircuits. These subcircuits are solved iteratively.

The Gauss-Seidel (GS) and the Gauss-Jacobi (GJ) relaxation can be used but the GS relaxation is preferred since it requires only one copy of the iterated solution as opposed to two copies required by the GJ relaxation. Also the speed of convergence is faster especially for MOS circuits.

### 3 The Waveform-relaxation Algorithms

The two waveform-relaxation algorithms for analysis of a dynamical system are presented.

#### 3-1 Gauss-Seidel algorithm

Consider the first-order two dimensional differential equation in

$$X(t) \in R^2 \text{ on } t \in [0, T],$$

$$\dot{X}_1 = f_1(X_1, X_2, t), \quad X_1(0) = X_{10} \quad (1-a)$$

$$\dot{X}_2 = f_2(X_1, X_2, t), \quad X_2(0) = X_{20} \quad (1-b)$$

The basic idea of the ‘‘Gauss-Seidel’’ waveform-relaxation algorithm is to fix the waveform  $X_2 \in [0, T] \rightarrow R$  and solve the equation (1-a) as a

one dimension differential equation in  $X_1(\cdot)$ . The solution thus obtained for  $X_1$  can be substituted into equation (1-b) which will then reduce to another first order differential equation in one variable,  $X_2$ . Equation (1-a) is then resolved using the new solution for  $X_2(t)$ , and the procedure is repeated.

In this manner, an iterative algorithm has been constructed. It replaces the problem of a differential equation in two variables by one of solving a sequence of differential equations in one variable. The unknown is the waveform (elements of a function space) rather than real variables.

The algorithm is a technique for time domain decoupling of differential equations.

#### 3-2 Gauss-Jacobi algorithm

The Gauss-Jacobi algorithm can be characterized by the following equation for  $X(t)$ , the vector of node voltages,

$$X^{k+1}(t) = f[X^k(t), \dot{X}^k(t), u(t), t]$$

Where  $k$  is the waveform iteration number,  $u(t)$  is a vector of external inputs, and  $t$  is time. To compute new values for the solution vector,  $X(t)$ , the GJ algorithm uses the results of the previous iteration. In contrast the GS algorithm uses a combination of results from the current and previous iterations. The GS algorithm forces an ordering of the analysis; hence some serialization among subcircuits occurs. Each subcircuit is assigned a level determined by its inputs.

Subcircuits that depend only on external inputs are defined to be level 1. Those that depend only on outputs from level-1 subcircuits and external inputs are defined as level 2, etc. The order of analysis is based on the circuit level, i.e., all level- $i$  subcircuits must be analysed before any level- $i+1$ . Fig.1 shows the subcircuit levelling.

### 4 Organization of the WR simulator

The WR circuit simulator will run in an iterative mode. The main routine will act as an interface between the user and the processors i.e. subroutines. It interprets the input commands and activates the corresponding internal processors implemented by subroutine calls. Some typical commands will be for:

- (i) Reading the description of the circuit from an external file.
- (ii) Continuing the execution of the WR iteration
- (iii) Setting the accuracy of the analysis.
- (iv) Monitoring the waveforms at each iteration and for bad accuracy go to (ii).
- (v) End.

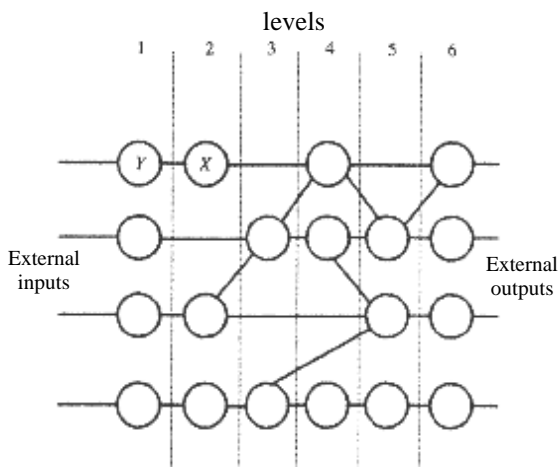


Fig.1 Example of subcircuit levelling.

The flow chart is given in Fig.2 .The circuit simulator can use the Shichman-Hodges model [4]-[7] for the MOS device. All the computation will be performed in double precision and the results are also stored in double precision. As such the simulator will require large amounts of storage especially when large circuits are analysed e.g. for a MOS circuit containing 1000 nodes with 100 analysis time points per node, the waveform storage is required to store approximately  $3 \times 1000 \times 1000$  floating point numbers corresponding to 24 MB if each number is stored in simplified storage buffering scheme can be implemented. In this scheme, the amount of primary storage allocation for the waveform is limited. When this storage is not enough to store all the waveforms, a secondary storage such as a disc is used to supply the additional storage needed. Other extensions to the WR method which can be incorporated in the circuit simulator involve the approximate solution of the sub circuit equations. Another approach to simplifying the calculations is to allow the numerical integration algorithm, which

is used to solve for the node waveforms of the decomposed sub circuits to use a larger truncation error.

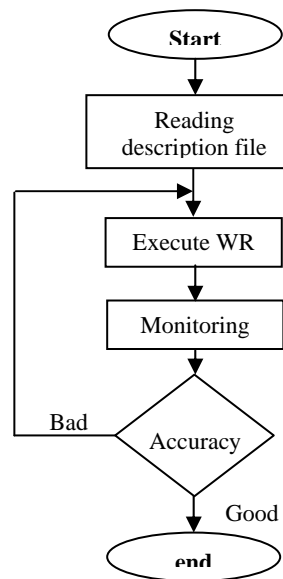


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## 5 Conclusions

Two waveform-relaxation methods i.e., Gauss-Seidel(GS) and Gauss-Jacobi(GJ) methods are presented for analysis of dynamical system. It is observed that the relaxation method have proven to be effective decomposition method for analysis of large scale circuits. It is based on the relaxation of non linear algebraic-differential equations describing the system to be analysed.

The design and organization of a circuit simulator based on the WR method is presented. There is a lot of scope for further work with the coding of each of the modules and their linking up.

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