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Design of an Ultra Low leakage Buffer Chain

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Abstract: -With technology scaling to deep submicron region, leakage power becomes dominant. With technology scaling, lower supply voltages are required to limit active power dissipation, excessive electric field & gate oxide leakage. Threshold voltage scaling has reached to a limit. Low threshold voltage results in excessive leakage [1]. Apart from device level tailoring, circuit design efforts are ongoing for leakage reduction in standby as well as active mode. We are presenting a methodology for reduced leakage databus which uses split supply rails. Compared to conventional power down methods, scheme is better in terms of leakage reduction, noise margin & reactivation time. Scheme is useful for long datalines particularly used in SOCs.

Key Words: - leakage, low power, databus design, deep submicron design, power down method.

1 Introduction

Scaling of semiconductor devices to smaller and smaller geometry has led to the reduction of supply voltage also. As the ratio of supply voltage to the threshold voltage becomes smaller, circuit speed is reduced due to reduced saturation current. In order to achieve speed threshold voltage is also reduced. As the threshold voltage is reduced, subthreshold leakage component also increases[1],[2]. This enhanced leakage is a big problem for large scale designs, where the leakage component equals or surpasses active component of the system at higher temperatures. As the technology is scaled & threshold voltage is also scaled, we could achieve proper drive capability. After a certain limit, it's not possible to scale down the threshold voltage keeping in view the excessive leakage and noise margin issues. This leads to reduced drive capability and large buffer sizes. Further, increased wire resistance demands large buffers to minimize path delay.

To reduce this leakage current, several design changes as well as device level optimizations are being done. High-Vt implant is used to reduce leakage if the speed can be compromised. Multi threshold voltage devices are another effort in this direction. Power gating in standby mode of operation is used to reduce the leakage current when system is not in use[3]. Power gating uses blocking of power supply with gating device. Power gating can be realized with VDD and/or VSS with the help of pmos and nmos devices as shown in Fig-1[4]. For ultra low leakage operation power is needed to be blocked completely & hence the intermediate data value is lost, also the reactivation of the system is large. We are analyzing a method which uses split power supply. For VDD as well as VSS rail. Method is applied for a chain of inverters and comparison is presented for both the schemes. A detailed discussion about the implementation & issues is also presented. Simulations are also done for the proposed scheme and results show the relevance of scheme with respect to its usage for leakage power reduction.

2 Problem Statement

Leakage in deep submicron cmos technology is a matter of concern [1], [2]. Several methods for leakage reduction has been proposed & being used. The growing density of devices makes it difficult for the designers to manage onchip standby/active power. Component of standby power is increasing significantly. Taking into consideration of such facts we need to find some methodology for near zero standby power dissipation. Since at process level we have severe limitations so this issue needs to be addressed by both, design as well as process. In course of application of such methods we need to take care of data integrity & noise margins also. There are already in use few very common methods such as complete power gating, power gating using diodes, high Vt devices, stack devices [2], [4]. All these methods have been extremely useful & successful in solving the problem of standby current. However we need to find some methodology, which goes beyond the reach of these methods, which makes our life easier. Reduction in noise margin

introduced by these methods puts a limitation on their use because we are operating in deep submicron region where supply voltage is below 1V. There is little room for further lowering the rail-to-rail voltage in order to accommodate these methodologies.

3 Split Supply Method

Subthreshold leakage can be expressed by following equation[5]:

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\xi V_T}\right) \qquad (1)$$

Where $\xi > 1$ is a nonideality factor and $V_T = kT/q$. In this region, device operates in weak inversion. With typical value of ξ, at room temperature V_{GS} must decrease by approximately 80mv for I_D to decrease by one decade. Thus reduction in threshold voltage results in significant increase in subthreshold current and power dissipation.

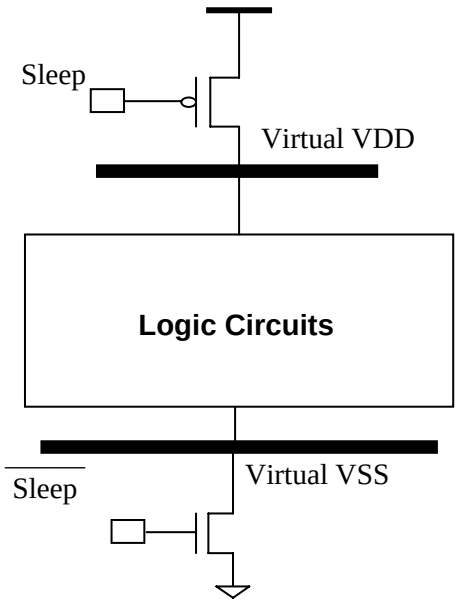

Fig.1 – Normal Power Gating

The proposed split supply method makes gate and source voltages different in standby mode and makes the junction reverse bias. Thus effective threshold voltage of the transistor is increased and leakage is reduced significantly. Fig-1 explains the normal power gating in use. Here the supply vdd/vss is provided through a pmos and a nmos. Control signal sleep is used to switch between active and sleep modes. A low sleep signal enables pmos & nmos, thus providing operating current for the circuits. A high sleep signal cuts-off the supply. Virtual-vdd and virtual-vss levels as shown in Fig-1 are now floating. In sleep mode virtual-vdd dips and virtual gnd rises so as to reduce the leakage current. For data retention purpose a diode in parallel is also used so that the virtual levels do not deviate more than a threshold. Normally this arrangement is used in SRAM memory array.

Fig-2 explains the proposed method of split supply. An inverter chain is shown where alternate inverter is connected to different vdd/vss lines. Supply vdd is now split in two through blocking pmos transistors 105 and 106 as vdd1 and vdd2. Similarly vss is split into vss1 and vss2 through transistors 107 and 108. If the input IN is 1 then power rail VDD2 and VSS1 are switched off. Supply to VDD2 is now available through diode 114. This diode does not allow the VDD2 line to go below VDD-Vt level. Similarly VSS1 does not rise due to diode 115. Supply rails VDD1 and VSS2 are at their normal values. Transistors responsible for leakage are 101, 104 and so on if the input is 1. These transistors are now reversed bias at their gate to virtual supply junction. This reverse bias condition increases the Vt of the transistor and leakage of these transistors decreases many folds. Since sizes of these buffers are very large for a long databus, application of the scheme provides an effective reduction in standby leakage for the system. As the input to the buffer in standby mode is uncertain, so we use a SRAM cell to store its state and to control the state of blocking transistors. Fig-3 explains the use of a SRAM cell along with Fig-2 where these control signals are used. SB is the standby mode signal which is active high. SB is low during normal fuction of the circuit and virtual rails are at their full values. As soon as SB goes low, input IN is sampled into SRAM cell & appropriate control is provided to all the control/Supply transistors to put virtual supply rails in favourable mode for leakage reduction. This can be used even in active mode also if the operational frequency is low. If switching is at high frequency then activation/deactivation of blocking transistors consume lot of power, hence it's not usable. If the statistical nature of switching is such that power invested in activation of these transistors during switching is less than the saving in leakage current over time, then we can use it. The main benefit and application of scheme is its use for standby mode leakage reduction, where an external signal SB is available for switching between active and standby modes. Time taken for reactivation is a timing

penalty for introduction to this system. Also we need to ensure enough decoupling capacitance attached to the secondary power rails VDD1, VDD2

control circuit is the main contributor towards the overall leakage of the buffer chain. Leakage of driving buffers in standby mode is more than Hundred times less in active mode. Thus the scheme

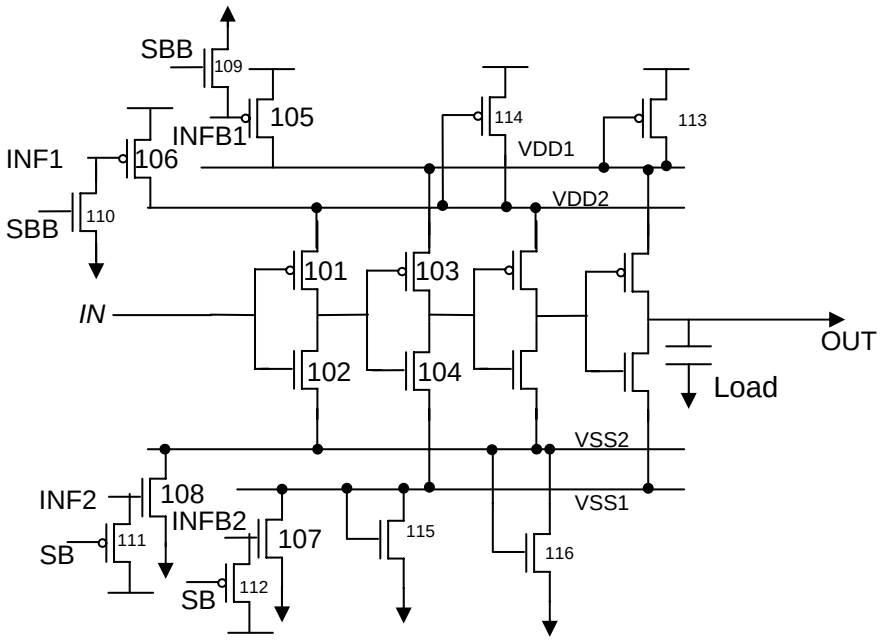

Fig .2- Split Supply Low Leakage Inverter Chain

VSS1, and VSS2. This is needed to ensure least timing penalty during active mode for the switching of buffer. Voltage drop caused due to series resistance offered by blocking transistor reduces speed as switching is delayed. Also we need to run these extra secondary power lines. Scheme is useful particularly for SOCs where large datapaths are required and very large buffers are used. Standby leakage becomes a bottleneck for high speed operation & also creates packaging issues.

4 Simulation & Results

To evaluate the concept, we have performed simulation over a series of inverters with the arrangement as shown in Fig-2. Virtual power rails are at their full value for the normal active mode operation. As soon as the standby mode signal is inserted, virtual VDD starts falling and achieves a stable value of VDD-Vt. Similarly, Virtual VSS starts rising and achieves a stable voltage of Vt as shown in simulation waveform (Fig-4). We could achieve a leakage reduction of 94% in standby mode. In fact the leakage component invested in

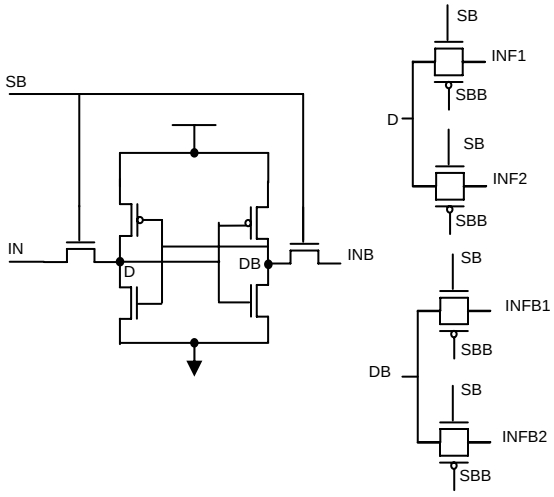

Fig.3 Control For Low-Leakage Buffer

is more useful for large buffers and buffer chains as the investment in terms of control circuitry is almost fixed for all sizes of buffers. In normal conditions, using a single rail supply we could achieve the leakage reduction of 45%. In normal gating method, we have used both p-diode on VDD and n-diode on VSS.Here also, this leakage depends on the value of

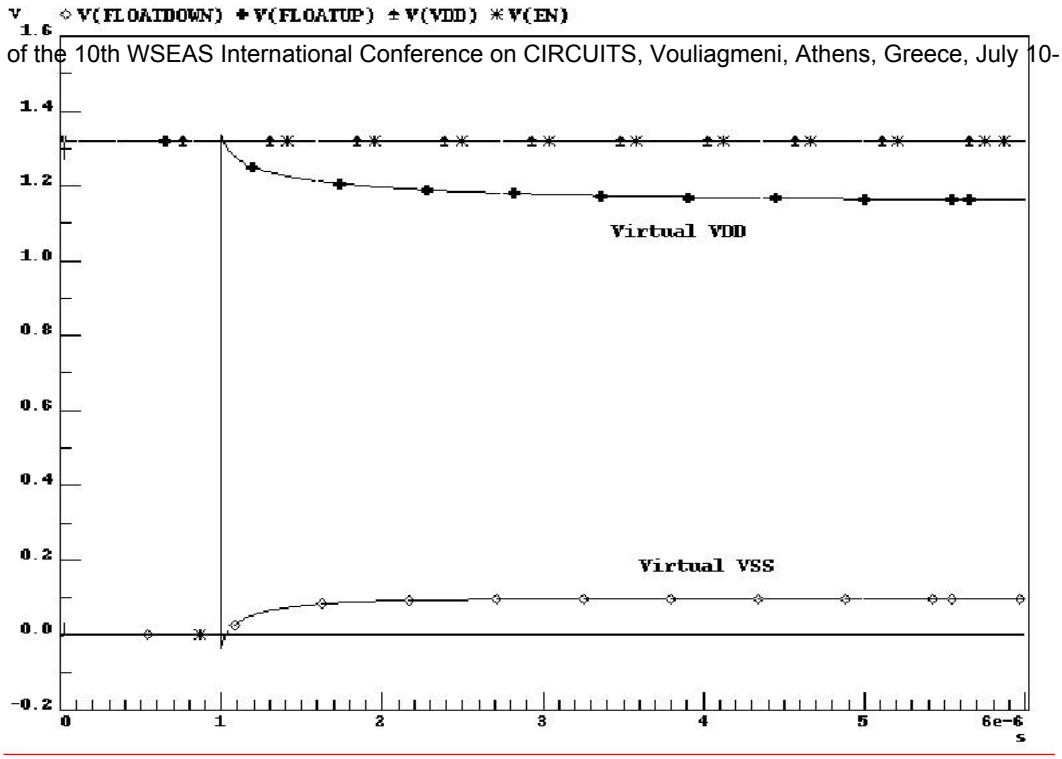

Fig.4 - Virtual VDD & VSS levels

input, as the last stage inverter is largest and major contributor for leakage in a particular state.

5 Summary & Discussion

Described method for leakage reduction is simple and more effective in comparison to other methods where we face problems related to noise margin and logic value isolation to avoid excessive current. In fact in normal gating method, gating is needed to be applied over the logic block/buffer chain, and we need to provide an isolation arrangement or data hold circuit. This is needed to store the previous data as well as to isolate the floating logic level from those blocks which are not put in standby mode, as this will result in DC power dissipation As we can observe in Fig-4, virtual VSS level is at Vt. This virtual level in normal gating method will interface with inverter with perfect VSS then a DC path will be created in the facing inverter. In the proposed & explained method intermediate logic states are maintained to their full values. Outputs of successive inverters are at full logic values, hence any interface will experience the perfect voltage required for its drive and no such DC path will be created. Further there is no need of any isolation stage or data hold stage. This removes the additional timing penalty faced by normal power gating method.

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