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A New CMOS-DC/DC-Step-Up Converter for up to *2 mW* Enduring Loads

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Abstract: This work provides an approach for a fully integrated step-up converter. It is designed for on-chip analog building blocks utilizing a *3.0 V* local power supply and specified for max. *2 mW* enduring loads. No external capacitors are needed. The voltage is generated from a *1.2 V* external voltage supply. After presenting the main circuit behaviour in ideal, parasitic effects are discussed which have an impact on the design-parameter. By continuous adjustments of the step-up frequency dependences of the output voltage from dynamic load variations are compensated.

Key-Words: step-up converter, DC/DC converter, voltage doubler, voltage booster, charge pump, bulk switching

1 Introduction

Increasing component density of MOS circuits demands a consistent decrease of the supply voltage. Current digital CMOS-circuits operate at about *1* to *1.4* volts. As well, an increase of the component density is appropriate for integrated microsystems, which means having digital and analog circuit functions on the same die. But mostly, precise analog CMOS circuits can *not* run at these low supply voltages or have improper design parameters. Therefore, complex mixed-signal circuits with a high gate count recommend two separate supply voltages – a low one for the digital gates and a higher supply voltage for the analog parts. In this work a circuit principle is presented for generating an on-chip high 'analog' supply out of the external low voltage 'digital' supply.

As mentioned in section 2 this circuit is very flexible in terms of its electrical characteristics. For example you can specify the output voltage and the maximum current load, which results in a certain area consumption, step-up frequency and power efficiency. Here we decided to have a *3.0 V* supply voltage for the analog part which is limited to an effective output power of *2 mW*. These specification appear to be the best compromise between usability of the generated voltage rail and the required chip area on the other hand which directly makes an impact on the costs. On this account the circuit has to be designed to be manufactured in a standard ('digital') CMOS technology line only, without any specific process options.

2 Circuit Function

For an on-chip voltage overshoot much higher than the supply voltage, mostly capacitors are used due to their charge-storing properties. When you load two equally sized capacitors C_0 with the voltage V_0 and stack one of them on top of the other, the resulting overall voltage will be:

$$V_{sum} = V_0 + V_0 = 2V_0 \qquad (1)$$

On the other hand its overall capacitance is reduced to:

$$\frac{1}{C_{sum}} = \frac{1}{C_0} + \frac{1}{C_0} = 2\frac{V_0}{Q_0} \;\Rightarrow\; C_{sum} = \frac{1}{2}C_0 \qquad (2)$$

When you use n capacitors C_0 the total voltage V_{sum} will be n-times V_0 and C_{sum}= *1/n* of C_0. Therefore, if we stack many loaded capacitors on each other, we generate an n-times voltage with in mind, that its overall capacitance is reduced to *1/n*. Fig. 1 shows this coherency.

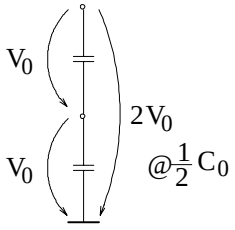

Fig.1: stacking loaded capacitors

Let's take a look at the discharge graph of such a configuration. Fig. 2 shows the terminal voltages of a three stage capacitor stack over time with a constant

resistive load on the top node. All of the voltages decrease in the same behaviour and have a constant deviation to each other. As the graphs point out it is not reasonable to make the highest possible voltage directly available as the output terminal because in this region the graphs have their highest negative gradient. This is another reason which practically limits the number of capacitors of the stack. But mostly the process' maximum physical breakdown field intensity of the thinoxide sets the hard limit for the generated voltage.

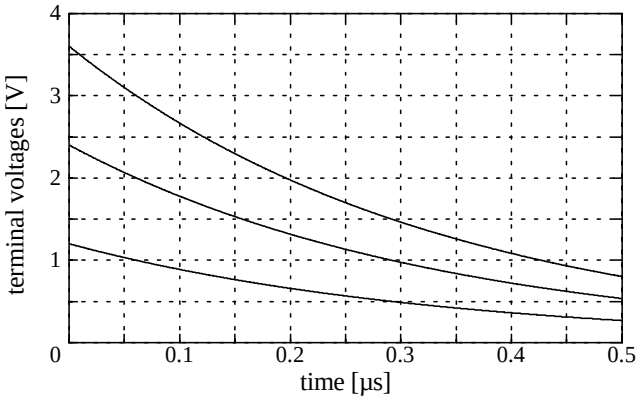

Fig. 2: stack discharge over time

For a continuous stepped-up supply voltage each of the capacitors has to be reloaded in dependence of its current drain. Since we have a single low voltage power supply only, the recharging has to be sequentially. Fig. 2 shows, that the discharge of the stack is equally distributed between the separate capacitors. Therefore the time intervals for the recharging can also all have the same period which is very comfortable. In Fig. 3 an ideal setup for the charging is depicted.

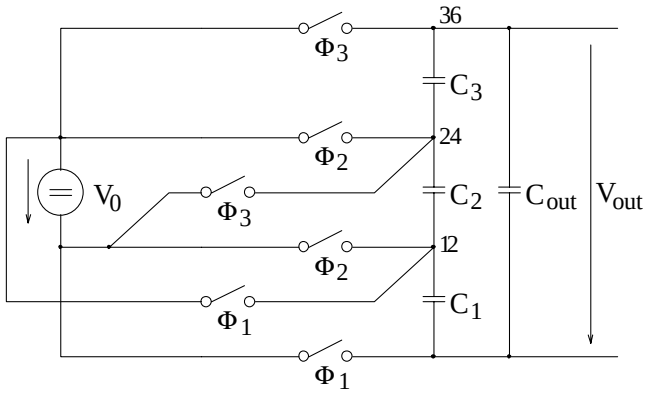

Fig. 3: cyclic charging of the stack

By using a switching matrix with clock signals Φ_1 to Φ_3 the single power supply is periodically connected to the corresponding capacitor of its associated time slice. Here another capacitance C_{out} is added as a supporting capacitor at the output to provide a more stable stepped-up voltage.

The circuit is designed for a *0.35 µm* CMOS technology line by Austria Microsystems. It is suggestive to apply a three stage capacitor stack here because the maximum rating for the voltage over the thinoxide of the standard process exactly is *3.6 V*.

This configuration is particularly suitable for an external *1.2 V* rechargeable battery: in the logic part of the overall circuitry we can use the external *1.2 V* source directly and the stepped-up voltage can drive the demanding analog part. So an originally double V_{DD} application can be satisfied with only one single battery cell, which is very convenient for mobile use.

In this CMOS process the logic can run at an energy-conserving *1 MHz* clock frequency which is good enough for a digital preprocessing of sensor signals from the analog part. Most of the integrated sensor types themselves require a supply voltage as high as possible. But since the time interval for a power cycle cannot be made arbitrarily small and MOS-switches have a finite conductance, there is a limit in the output current. A basic analysis of the ideal circuit behaviour is presented in Fig. 4.

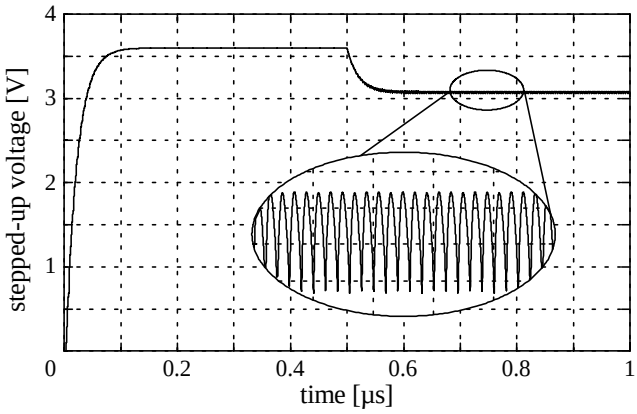

Fig. 4: circuitry running with ideal switches

The diagram shows the stepped-up voltage over time. For recharging the capacitors the time slices have a constant length of *4 ns* considering a rise-time t_r & a fall-time t_f each of *0.2 ns*. At $t_0 = 0\ s$ with unloaded capacitors the circuit starts up at no load and generates its ideal stepped-up output voltage of *3.6 V* in about *0.15 µs*. Then at $t_1 = 0.5\ \mu s$ the load jumps to *666.6 µA* causing the output voltage to fall down to an average of *3.07 V*. You can also see a magnification of the remaining output ripple under load situation with an amplitude of *27 mV*.

Due to continuous current drain all terminal voltages of the stack are pulled down (Fig. 2) but only one capacitor is recharged (the others follow in one of the next time slices). This leads to the shown

ripple form instead of the typical curve for a capacitance charge at constant voltage.

In a real environment any fluctuations of the *1.2 V* power supply (e.g. caused by dynamic load changes of the digital part) would not have an effect on the ripple of the stepped-up voltage. These variations are smoothed out via the low-pass filter characteristic composed out of the switch-resistance and the capacitance while recharging.

In this simulation with ideal components all of the capacitors were designed to have the same capacitance each of *20 pF*. In general using the thinoxide of a CMOS process for a capacitor yields in the highest capacitance per area but also you lose a bit of its linearity. However this is unconcerning here because we use the capacitors as a charge-storage only.

The most important design parameter for a concrete realization is the chip area this step-up converter consumes. Minimization of the chip area along with appropriate operation of the converter is the aim, which means, that very small capacitors are used only and no external components are intended.

With each stack level of *20 pF* plus an additional output capacitor a total sum of *80 pF* has to be integrated, which is set as an upper limit (in contrast to [2] even allocates *200 pF* in silicon). This can be done applying drain-source-bulk shorted MOS-structures (gatecaps).

As the AMS process is of n-well type, C_1 and C_{out} are modelled as N-MOS gatecaps on p-silicon whereas C_2 and C_3 are modelled as P-MOS gatecaps each having its own n-well. On the right side of Fig. 5 you can see the 4 gatecaps in a schematic view.

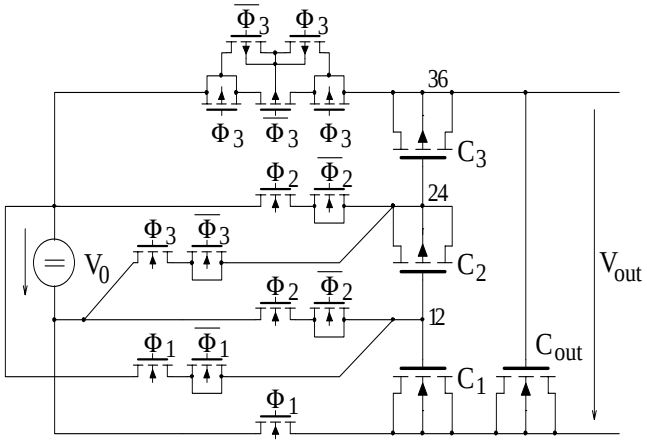

Fig. 5: equivalent circuit with integrated moscaps

To give an idea of the area consumption, each gatecap was designed with a W x L of *100 x 100 µm*, which only is about the size of a pad for manual chip contacts. Of course external capacitors would help very much but this would also let raise the total costs. On the other hand the output ripple would be much smaller or more drain current can be allowed at constant output voltage.

3 Parasitic Effects

When exchanging the ideal switches from Fig. 3 with MOS-transistors, some parasitic effects reduce the overall performance of the converter in each design parameter. All transistors used as switches (from Fig. 5) were designed with the minimum channel length of *0.35 µm*, whereas each of the widths is adapted to have a specified average on-resistance under its particular operating conditions. Simulations with HSpice revealed three main parasitic effects compared to the analysis with ideal components.

3.1 On-resistance

The MOS-switches have to conduct as much of current as possible to complete the charging within a minimum time interval. On this account the widths have to be maximized. Most of the shown MOS-switches also have a noticeable displacement of their threshold voltages which requires to make the widths even larger. With regard to the effect of charge injection (section 3.2) there is a trade-off between the channel-widths and other design parameters.

For good conductance in on-state the V_{GS} of each switch has to be at maximum (*3.0 V*). Unfortunately this lets the transistor go into triode region which means a decrease of V_{DS} during normal recharge also decreases I_{DS} and raises R_{ON} respectively. Therefore the on-resistance has a strong dependence on the current working point. It is changing in a wide range within its time slice. For this reason the stepped-up voltage of the MOS-circuit will never reach its ideal *3.6 V* (Fig. 8).

However it is not advisable to solve this problem with additional complementary MOS-switches. Because of strongly displaced threshold voltages these gates also had to be fairly wide which would decrease the total power efficiency of the converter. As a consequence the use of CMOS-transfer-gates is not very practical.

3.2 Charge injection

For lack of chip area we abandon the use of a huge supporting capacitor at the output terminal. The same reason limits the size of the capacitances of the stack. Therefore a noticeable reach-through of the clock signals can be observed from the MOS-switches in form of a big voltage ripple in all nodes. To lower this effect, dummy switches were applied. Fig. 5 shows that the dummies were only placed on the right sides since the left sides are connected to the voltage source. Unfortunately the use of dummy

switches stresses the output voltage as well, but at least they can be shaped in any wasted area within the layout.

However, even with dummies the switching noise cannot be overcome. Rather the relation between the switch-capacitances and the gatecaps has to be maximized. Since we focus on a cost-efficient and fully integrated solution here we set the limit for the overall capacitance to *80 pF*. On the other side reducing the switch-capacitances would decrease the effective output power.

3.3 Bulk voltage

As shown in Fig. 5 a PMOS-switch is used for charging the topmost terminal only. For each switch connected to node *24* a PMOS-switch configuration consumes more chip area than an ordinary NMOS-switch at comparable performance. The use of a PMOS-switch at node *36* causes its bulk voltage (which is the output terminal at the same time) to be lowered in line with the drain current of the load, if the bulk is hard-wired to the output node. Thus - at charging - it would be possible that a low output voltage biases the basis-emitter-diode of a parasitic vertical pnp-transistor in forward direction [1]. This would cause an unwanted current into the substrate consisting out of charges from V_0, C_3 and C_{out} . If the bulk of the PMOS-switch is hard-wired to the opposite side, this situation would be even worse at non-charging time.

A solution was proposed in [2], named bulk-switching. At the top margin of Fig.5 the schematic of this principle is shown. The underlying idea is, that the bulk always is connected to the higher voltage by proper control of the two gates, thus no substrate currents can occur. In the case of this step-up converter it is very easy to accomplish because the right timing signals for the two bulk-switching transistors are already available through Φ_3 and Φ_3 *inverse*. To simplify the schematic it is not depicted in Fig. 5 that the bulk-terminals of all P-MOS transistors - including the dummies - are short-circuited.

4 Timing

For proper control of the switching gates a defined clock scheme has to be generated. Fig. 6 shows how this can be done. There are no requirements to the duty cycle of the basic clock Φ_0 as it is fed directly into a negative edge-triggered synchronous modulo-3 counter. A demultiplexer chooses the appropriate clock-phase to be in on-state depending on the counter contents.

With a load of *2 mW* at *3.0 V* output voltage a basic clock rate for Φ_0 of *250 MHz* is required to generate the fastest timing. But as mentioned in section 6 Φ_0 will be controlled in dependence of the current load. Because of the segmentation of the three signals Φ_1 to Φ_3 each of them has a topmost frequency of *83.3 MHz* with an exact duty cycle of *33.3%*.

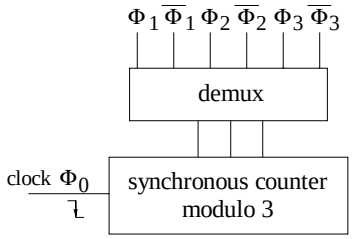

Fig. 6: generation of the clock scheme

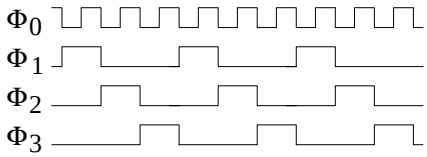

Fig. 7: timing of Φ_1 to Φ_3

5 Simulation Results

The dimensioning of this circuit was balanced to get many aligned values for most of the design parameters like an output voltage of *3.0 V, 2 mW* load, step-up time slices of *4 ns* or capacitors in size of a pad. For a concrete application it is better to optimize each of these parameters to their lower limits in order to leave others a bigger margin. Fig. 8 shows the simulation of the BSIM3V3 MOS-circuitry with HSpice.

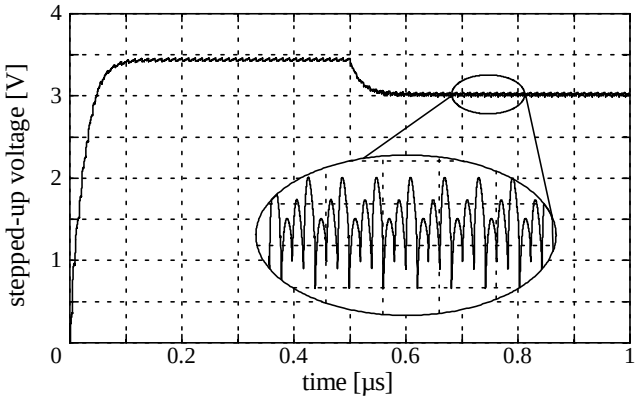

Fig. 8: circuitry running with MOS components

Again the step-up frequency under full load has a time slice for charging of *4 ns* (including t_r & t_f each of *0.2 ns*). At the beginning all capacitors are unloaded and the circuit is running with no initial load. Then at $t_1 = 0.5\ \mu s$ the load jumps to *2 mW* again, revealing the designed output voltage of *3.0 V*.

Here the observed output ripple has an amplitude of *52 mV*.

When the load goes beyond the specified *2 mW* this would have a further negative impact on the generated voltage and output ripple. If there is even a major lack of chip area, it is possible to omit C_{out} with in mind that the absolute level and the ripple of the output voltage will sink resp. grow up also.

6 Frequency Control & Efficiency

Without an adequate control mechanism the level of the stepped-up voltage will be changing contrawise with its drain current. Fig. 8 shows the two extreme values for a load of *0%* and *100%*. To obtain a good overall power efficiency it is advisable to reduce the step-up frequency in dependence of its current load situation. Thus, less reloads of all switch-capacitances have to be executed per time. So, if less drain current is pulled, the step-up converter consumes less additional power from the *1.2 V* voltage source resp. from the battery.

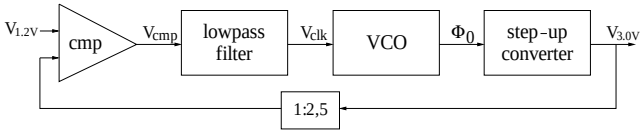

Fig. 9: control loop

If the low-pass filter is not set to a very high *RC*-constant, oscillations of the stepped-up voltage appear. Because the control loop then even tries to compensate the ripple of the output voltage as it is in the same dimension as the current step-up frequency. On this account the *RC*-constant rather has to be set to at least *500 ns*. However, this leads to a slow response time of the control loop when strong load changes occur suddenly, which means that the output voltage is not at a constant value for that period of time. Fortunately this is not very common in analog circuits.

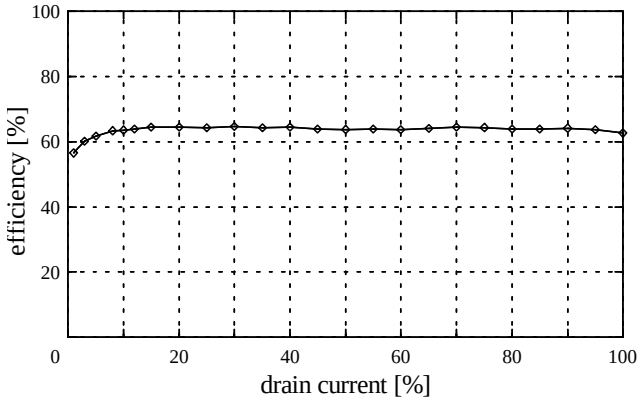

Fig. 10: simulated power efficiency vs. load

The diagram of Fig. 10 reveals the overall power efficiency of the converter in a steady state load situation. Compared to [2] for the fully integrated version the efficiency here is slightly less but still in a similar dimension. The maximum efficiency is *64.69%* at *30%* drain current with a Φ_0 of *44.2 MHz* (*14.7 MHz* for Φ_1 to Φ_3). With an increasing load it slowly falls down to *62.55%*. Overall the graph is relatively balanced. Towards an increased drain current the time slices decrease, thus t_r & t_f grow above average in relation to the total time interval. Towards a decreased drain current the efficiency also falls down because the energy-consumption of the voltage-booster has a larger share to the total power dissipation.

7 Conclusion

A principle for a CMOS-DC/DC-step-up converter was presented. In this fully integrated version the main focus is to keep the chip area to a minimum. Simulations confirm an enduring load of up to *2 mW* at *3.0 V* with a *1.2 V* power supply. This circuit is suitable for a high voltage sensor application with low power digital signal processing for mobile use. No external clock signals are required due to self-control of the step-up frequency.

In general with this circuit principle it is possible to exhaust the technological dielectric strength of the applied technology line. Also the principle allows a voltage multiplication of n times of V_0 in combination with a specific drain current depending on the other design parameters.

This dimensioning will be manufactured to verify the simulation results. Further, the control loop has to be optimized for quick load changes.

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