Proceedings of the 10th WSEAS International Conference on CIRCUITS, Vouliagmeni, Athens, Greece, July 10-12, 2006 (pp50-55)

RF On-chip Test by Reconfiguration Technique

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Abstract: The paper addresses on-chip test for IC RF transceivers. The baseband DSP available on chip serves as a tester while the RF front-end is reconfigured for test. The basic test setup is a loopback, enabled by a test attenuator and in some cases by an offset mixer, too. Different variants of this setup adopt the bypassing technique to boost testability. The existing limitations and tradeoffs in terms of test feasibility, controllability and observability versus the chip performance are discussed. The fault-oriented approach and the sensitization techniques are emphasized vs the functional test. The impact of production tolerances is addressed in terms of the detectability thresholds.

Key-words: RF test, DfT, BiST, on-chip test, RF transceivers

1. Introduction

Over the years of its development, production test of digital ICs has reached a significant degree of maturity. This progress has been enabled by several techniques, such as fault simulation, test-pattern generation and the built-in-self-test (BiST). Unlike this, much less success has been achieved in the analog/RF and mixed-signal ICs domain, where functional testing has been widely used and the major advances have been in the capabilities of expensive automatic test equipment (ATE). At present, the advancing complexity and performance of mixed-signal and RF ICs are pushing functional test methods and the ATE to the edge of their limits [1]. In this context, alternative approaches based on analog fault modeling, design for testability (DfT) and built-in self-test, so far not appreciated by industry, are appealing and can alleviate the problem [2]. While borrowed from the digital "world", the underlying concepts appear very different due to the continuous nature of analog/RF circuits, their sensitivity to small parameter variations and the problem of tolerances as well.

In fact, for the analog ICs of low- or mid-frequency a couple of DfT/BiST solutions have been proposed [2] (including the IEEE Std. 1149.4). For RF ICs, however, it has not been the case since RF designers used to be quite cautious to incorporate an extra test circuitry into their receivers or transmitters. Those choices have been justified by a variety of phenomena typical of RF ICs that are susceptible to crosstalk, loading, noise, etc. Nevertheless, under the pressure of increasingly high requirements for chip testing and the involved costs in mass production, the need for DfT/BiST suitable for RF circuits is gradually becoming a must [1,3]. On the other hand, having an insight into RF IC design one can realize the existing tradeoffs between testability enabled on chip and the required performance in the normal operation mode. Those tradeoffs and the area overhead are key factors in RF design for test.

Basically, only a limited test circuitry is accepted on a chip, nevertheless the available on-chip resources can be reused during test. Specifically, for a highly integrated mixed-signal/RF circuit, the available AD/DA converters and a signal processor (DSP/BB) can be used to test the analog/RF part. In this case, the DSP can serve both as a test pattern generator and response analyzer implementing in this way the BiST technique [3-8]. During test DSP verifies correctness of the analog/RF part of the chip and prompts with a fail/pass signal.

To enable different signal path in the test mode, other circuits, like switches or attenuators must be introduced. Those elements also provide flexibility needed to boost the test controllability and observability on a chip.

Since the specification-oriented tests, especially for RF front-end circuits, take long time, indirect tests based on nonlinear regression method have been investigated recently [8-10]. An alternative approach is fault-oriented RF test, where stimuli different from standard specs are employed. The latter technique is particularly useful in terms of a mature and stable manufacturing process, where

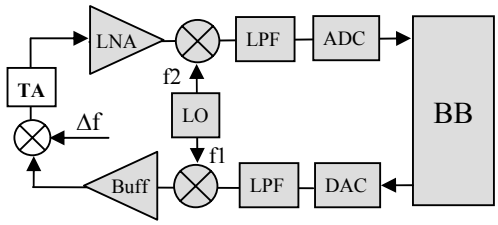

Fig.1. Loopback test setup for IC GSM transceiver

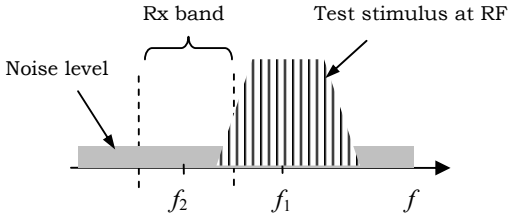

Figure 2. RF signals in test for selectivity faults

measurements of various RF specs can be replaced by simple test signatures [4-6,10,11].

In this paper we discuss various on-chip RF test techniques with the emphasis on the fault-oriented test. Both system- and circuit level perspective are used, which reflect the advantage of using different abstraction levels to develop the test. The existing limitations in terms of controllability, observability and the tradeoff with the chip performance are discussed in detail. The problem of circuit tolerances which tend to obscure faults is addressed as well. For a given test and given fault derived are detectability thresholds that also reveal advantages of one test over another. Implementations of the on-chip test circuitry and remarks on RF blocks designed for test illustrate the approaches.

2. Specs- and Fault-oriented Test

For RF receivers (Rx's) and transmitters (Tx's) a number of different tests have been specified, which mainly address sensitivity and selectivity of Rx, and power levels and spectral purity of Tx. Some of the RF tests are complicated and time consuming, so in mass production even when performed on chip, they are considered costly. For this reason, more time effective equivalent tests have been sought for. They fall in two categories: specification- and fault-oriented.

In [8] an on-chip test for an IC GSM transceiver has been demonstrated by implementing a loopbback setup (Fig.1), where an offset mixer compensates for the difference between the transmit and receive frequency, and the attenuator TA provides signal levels suitable for Rx. Optimized periodic bit sequences are used as stimuli at Tx baseband, and the Tx and Rx specs are extracted from the spectral response of the loop. For this purpose a non-linear regression method is employed. Specs that are correlated with the test response, like: gain, ACPR and IP3 of Tx, and gain of Rx can be measured in this way with good accuracy and reduced test time. Some specs, however, like IP3 of Rx display low correlation and require different techniques to be measured.

A similar approach has been demonstrated for a set of two-tone tests used to replace lengthy bit error rate (BER) test [9]. The BER value has also been estimated by non-linear regression technique.

As opposed to this, in the fault-oriented approach, impairments in specs are detected by a simple signature rather than identifying those specs. The method is supported by fault modeling. Specifically, using the loopback setup it is possible to detect faults in Tx or Rx that degrade their gain and noise figure (NF) by applying random digital patterns at Tx baseband. The response can be a simple signature like BER or error vector magnitude (EVM) measured at Rx baseband. While in the previous approach optimization of the bit test sequences was necessary to boost the correlation between the spectral response and the specs, here, a typical strategy is in tuning the RF signal down to the Rx sensitivity level, and/or using extra noise to reduce SNR at the same time. In this way the test achieves higher sensitivity to impairments in gain and NF, and also it takes much less time compared to a typical BER test (the small SNR raises BER by orders of magnitude). In case of spot defects (discussed in Sec.3) there is usually a correlation between impairments in linearity (IP3) and noise performance [6], so the BER/EVM test with enhanced sensitivity would cover most impairments in linearity as well. On the other hand, to detect defects which only affect linearity (such as an increased drain resistance in one branch of a differential amplifier) the test for linearity appears indispensable.

The application of BER test can be extended for verifying selectivity of the Rx or the corresponding impairments in Tx. For this purpose Tx and Rx operate with different carrier frequencies, f_1 and f_2 close to it, such as an adjacent channel (Fig.2). In this case, Rx would sense noise in f_2 band plus a portion of the test signal that would leak from f_1 to f_2 band, dependant on the signal level (and of course the selectivity). The response of the faulty chip displays an increased number of symbols received at baseband. The difference $|f_1 - f_2|$ can be smaller than the relevant channel spacing to make the test response sensitive enough.

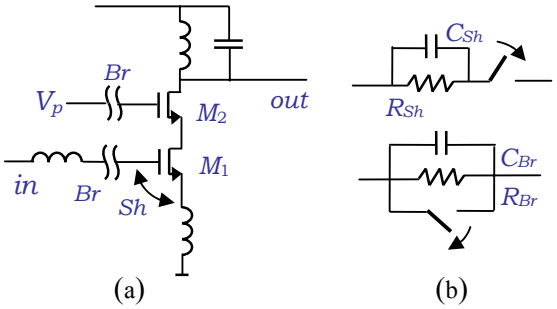

Figure 3. (a) Some possible spot defects in CMOS LNA circuit, (b) models of resistive bridge and break

The concept of the fault-oriented test is justified all the more, in mass production the simple *go/no-go* strategy is obeyed (diagnosis in not the issue). Moreover, investigation of specification oriented tests reveals that they tend to be redundant with respect to some faults, but also incapable of detecting others.

3. Fault Abstraction

The typical of CMOS, spot defects can evoke malfunction of a chip or degrade its performance. The defects, like cracks or "bites" in layout paths, resistive vias, "silvers" i.e. remains after polishing etc., are considered the main yield limiter in a stable CMOS production process [13]. A model of the spot defects represented at the circuit level is shown in Fig.3. [5,6,14]. By injecting the spot defects into RF circuits and running simulation a significant impact on specs like gain, NF or IP3 can be observed.

One can use this mapping to make the test model tractable in terms of testing a whole chip. The respective impairments in RF block specs are referred to as faults. To develop a test, behavioral models or high level simulation models (including the faults) are employed. In this way, other unintended local or global process variations that affect the measured responses are covered, too.

4. Sensitization Technique

In the loopback signal path the test controllability and observability are limited and detection of some faults proves difficult. In other words, a test response from a faulty RF block (such as amplifier, mixer, filter) can be obscured by the following blocks and tolerances of their parameter. Neither the quality of test stimuli after passing a chain of blocks can be guaranteed.

The conditions to enhance sensitivity of a fault-oriented test response can be formulated based on a behavioral model [6,15]. Specifically, for the EVM

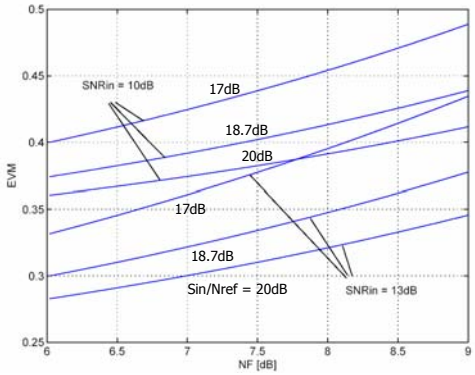

Fig.4. EVM response versus receiver NF for S_{in} and SNR_{in} mesaured at Rx input

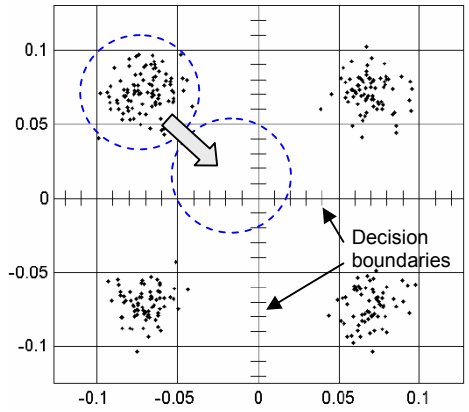

Fig.5. Constellation of QPSK signal in Rx with noise.

test, a very low signal power at the Rx input can be anticipated. By observation that EVM at the Rx output equals $1/SNR_{out}$, and signal-to-noise ratio in the Rx path is degraded due to

$$SNR_{out} = \frac{SNR_{in}}{1 + \frac{N_{ref}}{N_{in}}(NF - 1)} \qquad (1)$$

where N_{in}, N_{ref}, NF are the input noise, reference noise and noise figure, espectively, $dEVM/dNF_{Rx} = N_{ref}/S_{in}$. where S_{in} denotes the signal power at the Rx input. The relevant plot showing EVM versus NF and the involved parameters is given in Fig.4. During the test, SNR_{in} should be kept low (in practice, enriched with extra noise at Tx baseband) and otherwise EVM would be a small number, difficult to measure.

The conditions to sensitize the BER test can be derived from constellations which represent the modulated signal in Rx (Fig.5). The physical defects that degrade NF add extra noise to the noisy constellation points. The constellation points that are close to the decision borders tend to cross over, resulting in the reception errors. Then BER is raised, and the defect is visible. To place the constellation points close to the decision borders both low S_{in} and

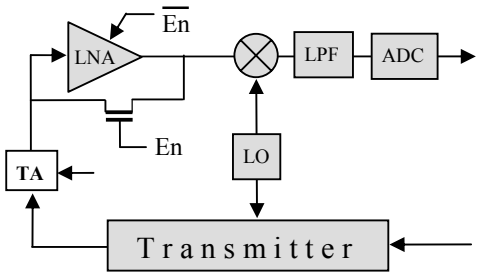

Fig.6. RF test path with bypassed LNA

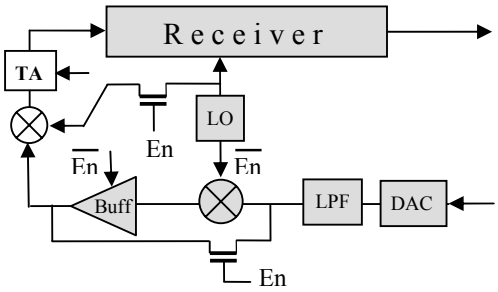

Fig.7. RF test path with bypassed up-conversion mixer

low SNR_{in} are useful (the latter provides more scattering). An alternative approach is to introduce an interferer at Tx baseband that renders the reference constellation points to split in circles, which adhere to the decision borders [15].

Using a mathematical model for probability of errors in e.g. *n*-PSK demodulator with additive white Gaussian noise

$$p_e = erfc(\alpha\, SNR_{out}^{0.5}) \qquad (2)$$

the optimum SNR for the BER test can be found. To achieve this point in practice, recently, a technique based on geometric translation of the constellation points has been proposed [16]. The dashed circles and the block arrow shown in Fig.5 illustrate the optimum translation implemented at Rx baseband. The test stimulus used in this case should feature a high SNR as opposed to the previous approach.

Sensitization of the IP3 test response is more difficult to achieve because the self masking effect plays role. Specifically, for two blocks in series the total IP3 can be found from $IP3^{-1} \approx IP3_1^{-1} + G_1 IP3_2^{-1}$. Assume a defect in Block 1 rendering both $IP3_1$ and gain G_1 degraded that is a typical case. So when the two blocks contribute to $IP3^{-1}$ equally, this fault can be invisible in spite it is strong. Fortunately, this drawback can be overcome by implementing the bypass technique that we discuss in the following section. It should be noted that the IP3 test is an important complement to BER (or EVM) test.

5. Chip Reconfiguration for Test

Testing of RF front-ends is increasingly difficult for limited test access, i.e. limited controllability and observability on a chip. Insertion of test points in today RF circuits is basically accepted at baseband only. In this context, chip reconfiguration and RF BiST techniques are gradually becoming a must. For an RF transceiver, the loopback test setup is beneficial as discussed before. However, extra test circuitry is required to enable the test (as shown in Fig.1). The direct loopback test, i.e. only using attenuator, is feasible when Tx and Rx are fully compatible. That is, they operate at the same RF, and when the frequency synthesizer (LO) is shared by the Tx and Rx, also the same IF must be used by them. Otherwise, the offset mixer is needed as well. The offset mixer can also enable loopback test for a class of transceivers where modulation is performed at RF (not at baseband) and LO is shared by Tx and Rx (e.g. low cost Bluetooth).

The advantage of the loopback setup is evident in terms of the limited test circuitry required. Also simple test signatures, like BER or EVM facilitate the test. However, faults affecting the RF blocks achieve different detectability depending not only on their strengths, but also on fault location and the type of test. For example, an impairment in NF or gain of LNA would be much more pronounced in the EVM or SER test response than even stronger impairments in the downconversion mixer specs. This is because LNA decides the receiver NF by raising the signal level before the mixer adds its noise. Invoking the Friis formula:

$$NF_{Rx} = NF_{LNA} + \frac{NF_{Mix} - 1}{G_{LNA}} + \frac{NF_{other} - 1}{G_{LNA} G_{Mix}} \qquad (3)$$

we find the corresponding sensitivities to the mixer parameters to be attenuated by the LNA gain. To overcome this drawback the bypassing technique can be used [17]. Fault diagnosis is also supported in this way. When LNA is bypassed, as shown in Fig.6, the faulty down-conversion mixer (with degraded NF) can achieve as good detectability as the faulty LNA in the basic loopback setup. Apparently, the LNA gain is replaced here by the attenuation of the enabled MOS switch. At the same time LNA is disabled to break the unwanted signal path and to circumvent loading. With this circuit, we avoid using a multiplexer which would degrade the Rx performance in the normal operation mode.

In a similar way the Tx output buffer can be bypassed, too. On the other hand, if the offset mixer is put on chip to enable the loopback test, it can also support bypassing of the Tx- or Rx mixer. The test

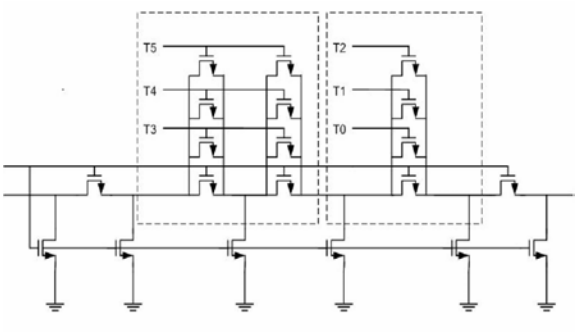

Fig.8. All-MOS digitally controlled test attenuator

setup shown in Fig.7 enables bypassing of the Tx front-end in order to emphasize possible impairments in receiver IP3. Specifically, the total loop IP3 obeys the formula:

$$IP3^{-1} \approx IP3_{Tx}^{-1} + G_{Tx}IP3_{Test}^{-1} + G_{Tx}G_{Test}IP3_{Rx}^{-1} \qquad (4)$$

so when the Tx front-end is excluded, the contribution of Tx and the test blocks (offset mixer and TA) is significantly reduced. At the same time, to compensate for G_{Tx} drop, G_{Test} can be increased using TA gain. The baseband signal in Tx must be kept low to avoid nonlinear distortions in the bypass switch.

The key issue here is to assure high performance of all the test circuitry. In particular, linearity of the offset mixer and TA can be crucial. A circuit implementation of a highly linear TA is shown in Fig.8 [17]. Designed in 0.35µm CMOS process it achieves IP3 > 20dBm and it can be disabled in the normal operation mode in order not to affect the chip performance. The same applies to the switches used for bypassing and disabling the RF blocks.

At the expense of more area overhead, different test configurations can be introduced, e.g. a loop closed at baseband. In this case the baseband blocks (DAC, ADC and filters) would be under test while LNA and the up/down conversion mixers would be excluded. The design requirements for those test blocks would be much relaxed due to their low-frequency application.

6. Detectability Thresholds

Parameter tolerances tend to mask faults during test. Using simulation it is possible to capture this effect for different types of faults and locations. Since the "worst-case" analysis or the Monte-Carlo technique provide over-pessimistic estimates or suffer from excessive simulation effort, respectively, one can refer to the behavioral models. The problem can be discussed in terms of statistical parameters supported by sensitivity analysis.

Consider a test response denoted by w (such as

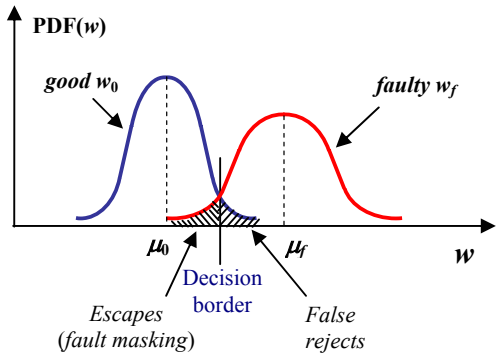

Fig.9. PDF of test responses for good- and faulty chip

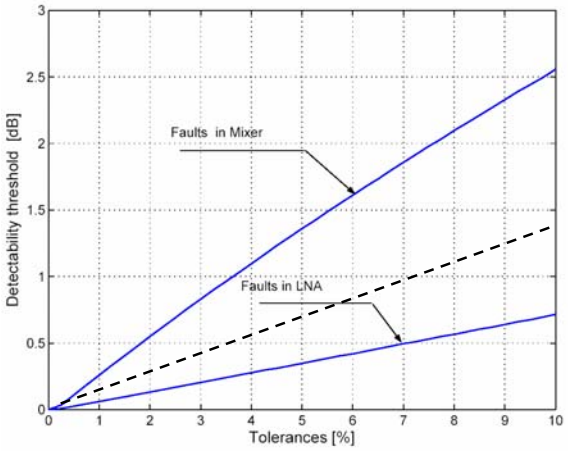

Fig.10. Detectability thresholds ΔG (ΔNF) for EVM test (solid lines), and for gain test (dashed line)

EVM or power gain) [6]. Its variance referred to parameters x_i of the involved RF blocks (NF, gain or IP3, respectively) would be

$$\sigma_w^2 = \sum_i \left(\partial w/\partial x_i\right)^2 \sigma_{xi}^2 \qquad (5)$$

As shown in Fig.9, a fault drives the test response from w_0 to w_f, and to make it detectable the distance between the corresponding mean values μ_0 and μ_f should be large enough. Otherwise, detection with a low confidence level would be achieved, and a significant number of "false rejects" or "escapes" during the test might be expected. Here, we assume:

$$\left|\mu_f - \mu_0\right| \geq 3\left(\sigma_0 + \sigma_f\right) \qquad (6)$$

which results in probability of fault masking equal 0.0013 for Gaussian PDF. For a given transceiver under test and given fault, solution of (6) provides the lowest detectable value of that fault, referred to as the *detectability threshold* (DT). Figure 10 illustrates results obtained for a given transceiver under EVM- and gain test for faults, which degrade both NF and gain (ΔNF = -ΔG) in LNA and in the down-conversion mixer. All the parameter tolerances of the transceiver were assumed to be of 3σ, i.e.

$t_{xi} = t = 3(\sigma_{xi}/x_i)\cdot 100\%$. In practice, those tolerances can be kept below 5% provided the blocks are designed as differential circuits, so that the corresponding detectability thresholds are relatively low. Also the design for correction mitigates the problem.

A few observations should be made here. Firstly, the EVM test displays its advantage over the gain test for faults located in LNA, the respective DTs are much lower for the same tolerances. On the other hand the DTs for gain test do not depend on fault location in the loop, which is advantage of the gain test. Finally, when LNA is bypassed during the EVM (or BER) test, the mixer achieves DTs similar to LNA that even more justifies the bypassing technique.

Basically, the detectability thresholds can be reduced at the expense of lower confidence level, i.e. more false rejects and escapes. Unfortunately, reduction of DTs entails significant increase in probability of masking and false rejection. Reduction of DTs (defined in dB scale) by a factor of 2, e.g. from 2dB to 1dB, raises the probability from 0.0013 to 0.067.

7. Summary

When designing a highly integrated RF transceiver, BiST can be implemented at a low cost. The on-chip AD/DA converters and the baseband DSP can be reused and usually extra test circuitry needed for test is very limited. For fully compatible transmitter and receiver a test attenuator is sufficient to enable the loopback test, while for other transceivers an offset mixer must be put on chip as well. In this case, also extra requirements for the frequency synthesizer follow.

More flexibility can be achieved using additionally the bypassing technique that can boost the controllability and observability in the loopback setup. This requires extra switches to be put on chip, which are also used to disable the bypassed blocks or enable different tests [11,12]. Using analog multiplexers instead, is discouraged since they cannot be disabled in the normal operation mode and thereby tend to deteriorate the gain and linearity performance. The primary requirement for the test circuitry is very good linearity and low parasitics affecting the chip in normal mode. Otherwise, the possible impairments in linearity of the RF blocks can be obscured or false rejects can occur during test.

A variety of tests can be run in the BiST setup. Flexibility in the stimuli generation at Tx baseband and control of the signal power provide opportunity to sensitize the test response in some cases. Still the parameter tolerances tend to obscure the possible faults and to drive the circuit out of specs. For this reason the design for correction should be combined with DfT. Also the respective detectability thresholds should be estimated carefully.

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