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Low Voltage Low Power CMOS Image Sensor with A New Rail-to-Rail Readout Circuit

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Abstract: - In this paper a new rail-to-rail pixel readout architecture is proposed to enhance the performance of CMOS image sensor for both low voltage and low power applications. Due to this new readout circuit, the enough input voltage swing under a low supply voltage is achieved and guaranteed for correct successive signal processing. As a consequence, the ability of working under a lower voltage using the same process is greatly improved. The layout size of each pixel is 17um×11.55um. The design of a 64×64 bits CMOS image sensor circuit has been completed. The proposed CMOS image sensor can extend its operating voltage from 3.3V even down to 1.8V for a 0.35um process. The total power dissipation is 0.528mW at 3.3V supply and down to 0.102mW at 1.8V.

Key-Words: CMOS, Image sensor, Rail-to-rail readout, Low voltage, Low power, Pixel

1 Introduction

CMOS image sensor has been widely used in various applications, such as video camera recorders, digital cameras, cell phones, PDA, etc [1-10]. It is expected that the demand of CMOS image sensor will rise up rapidly in the next few years. The image sensors which are designed to be used in mobile systems are now becoming a key point of research, especially. In order to make it capable of working in mobile systems, these two characteristics below are needed: (1) lower supply voltage and (2) lower power consumption. Because charge-coupled devices (CCD) need a high supply voltage and therefore they are unable to be integrated in the same chip with other circuits, CMOS image sensors gradually take the place of CCDs in mobile applications.

As the supply voltage scales down the readout circuit of CMOS image sensor becomes more difficult to meet the low voltage requirements. In order to improve the performance under lower supply voltage, a new rail-to-rail pixel readout architecture is proposed in this paper. Due to the new readout circuit, the enough input voltage swing under low supply voltage is achieved and guaranteed for correct successive signal processing. The ability of working under a lower supply voltage using the same process is greatly improved.

2 Conventional Circuits

The pixel circuits of CMOS image sensors are usually of either the passive type or the active type. The passive pixel contains a photo-diode and a transmission transistor for circuit operation. The active pixel sensor (APS) includes photo-diode type APS and photo-gate type. In the CMOS APS, besides a photo-diode, it mainly consists of a reset transistor, a source-follower and an address

select transistor.

As shown in Figure 1, it is a conventional pixel circuit [6] along with the readout structure. Transistor M02 plays the role of a source follower to generate the voltage level at node a which is resulted from the photo current in the photo-diode. To design a CMOS image sensor, many factors including array size, resolution, pixel size, fill factor, dark current, dynamic range, signal-to-noise ratio, quantum efficiency and fixed pattern noise should be well considered. In the literature, a reverse-biased pixel is proposed for low voltage operation [7], as shown in Figure 2. As illustrated in Figures 3 and 4, are the high dynamic range sensor [8] and the rail-to-rail readout sensor [9], respectively.

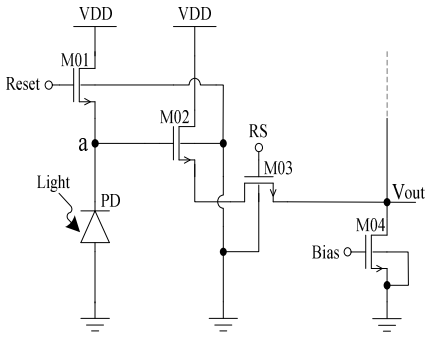

Fig. 1 Conventional pixel and readout [6]

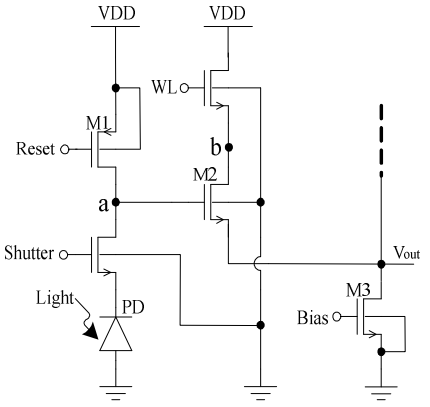

Fig. 2 Low voltage pixel and readout [7]

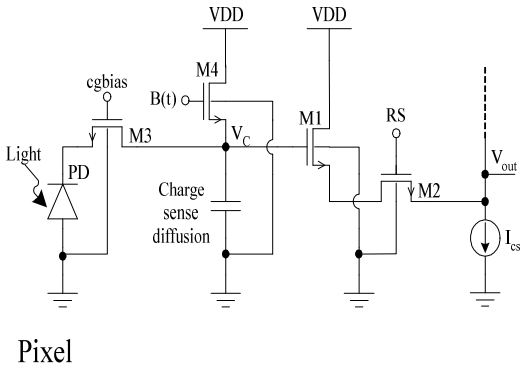

Fig. 3 High dynamic range CMOS sensor [8]

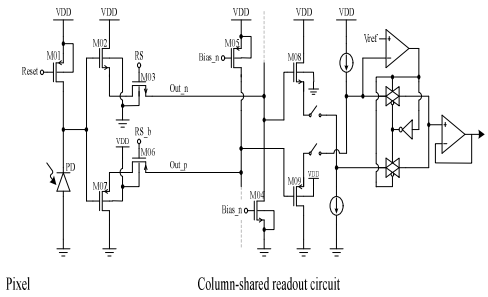

Fig. 4 Rail-to-rail readout and pixel [9]

3 Proposed Pixel Structure and Readout Design

As shown in Figure 5 is the proposed low voltage rail-to-rail pixel readout circuit. The presented CMOS image sensor is composed of both pixel and column-shared readout circuit. This readout circuit output is obtained by combining the two outputs coming out of the rail-to-rail pixels. After taking use of these two parts of circuits, both the input and output voltage swings remain in good performance even if the supply voltage is lowered down. The functions of pixel outputs (Out-p and Out-n) and the combined output Out-c can refer to Figures 6, 7 for further illustration. As for the convert stage, the simplified concept is shown in Figure 8 with the respective

timing controls in Figure 9.

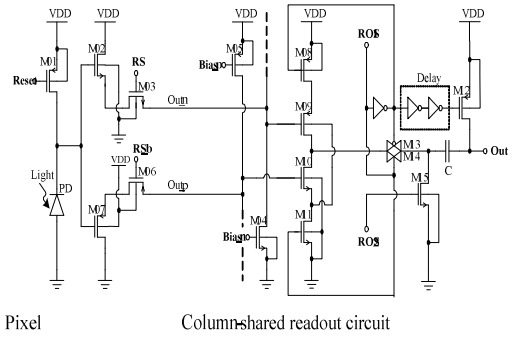

Fig. 5 Proposed rail-to-rail readout and pixel

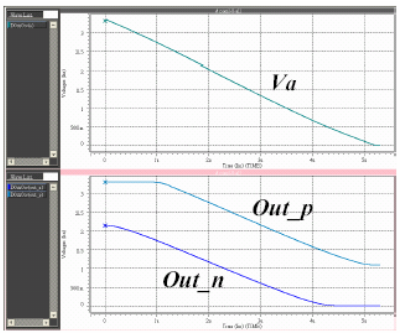

Fig. 6 Voltage outputs of Va, Out-p and Out-n

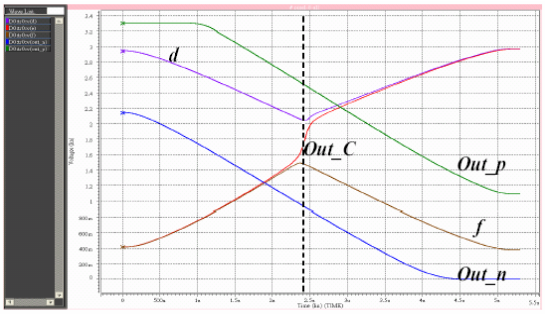

Fig. 7 Combined output Out-c

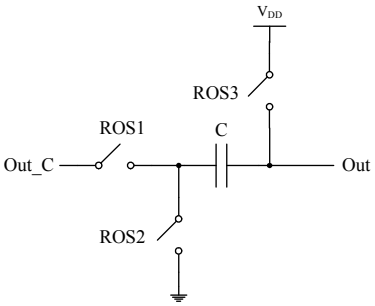

Fig. 8 Conceptual function of convert stage

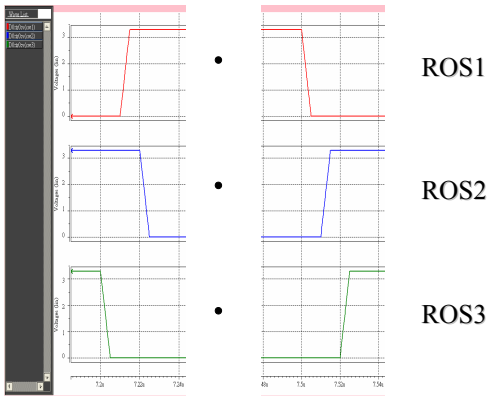

Fig. 9 Control timing for signals ROS1 ROS2 ROS3

4 Simulation Results

To verify the validity of the proposed rail-to-rail pixel readout circuit many simulations have been preformed by HSPICE. The circuit operations of one pixel is examined first. The voltage outputs at nodes a, Out-c and Out are shown in Figures 10-12 for VDD=3.3V, respectively. Once the power is reduced to 1.8V, the related results are shown in Figures 13-15. Very satisfactory pixel readout operation is achieved. A 64×64 bits CMOS sensor is designed using the proposed pixel and readout circuits. The simplified array structure is shown in Figure 16. The respective timing control is illustrated in Figure 17. Finally, the layout of one pixel is given in Figure 18. The summarized performance of the 64×64 bits CMOS image sensor is shown in Table 1.

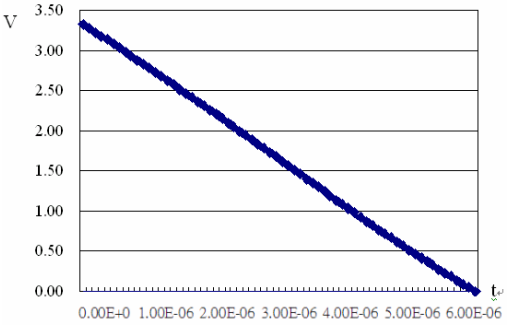

Fig. 10 Output of Va for VDD=3.3V

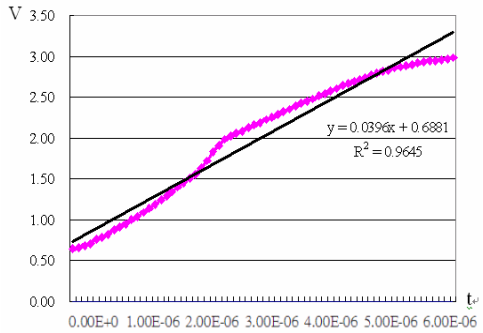

Fig. 11 Output of VOut-c for VDD=3.3V

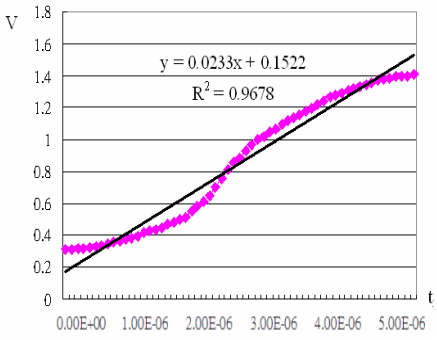

Fig. 14 Output of VOut-c for VDD=1.8V

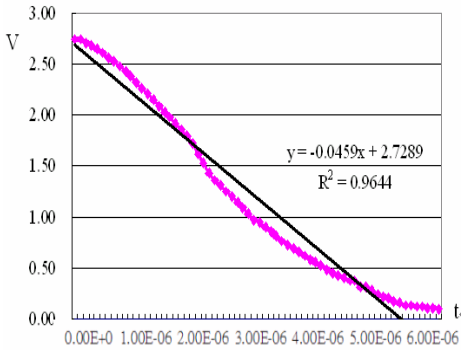

Fig. 12 Final output of VOut for VDD=3.3V

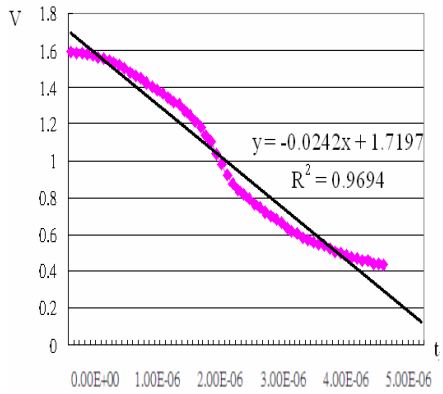

Fig. 15 Final output of VOut for VDD=1.8V

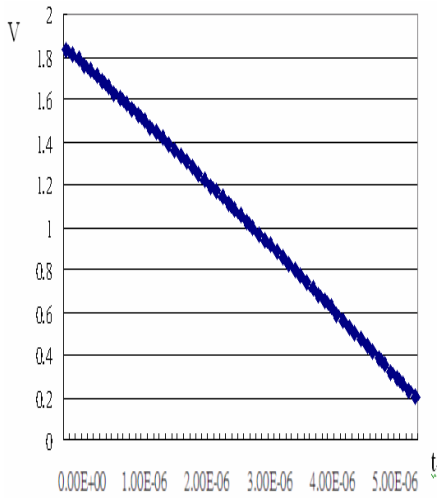

Fig. 13 Output of Va for VDD=1.8V

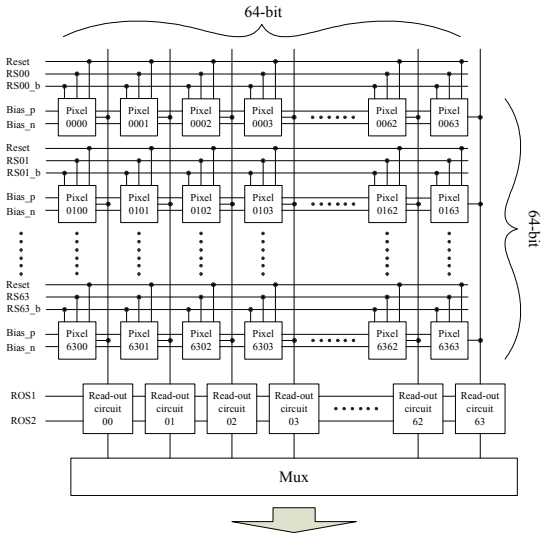

Fig. 16 Array structure of 64X64 bits

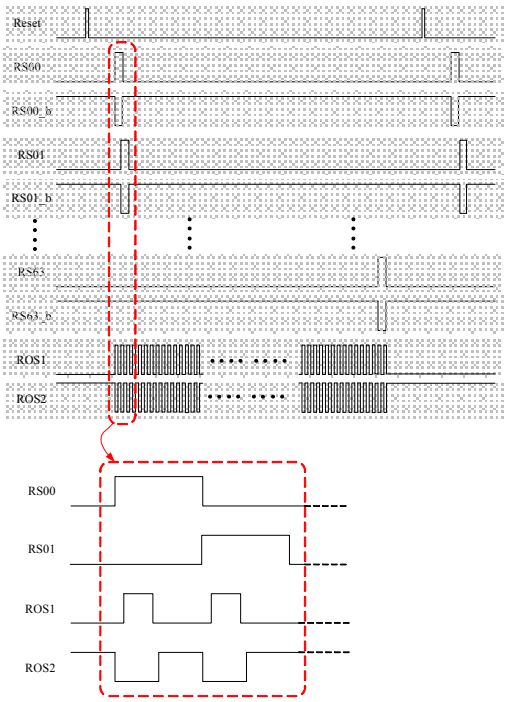

Fig. 17 Respective control signals and timing

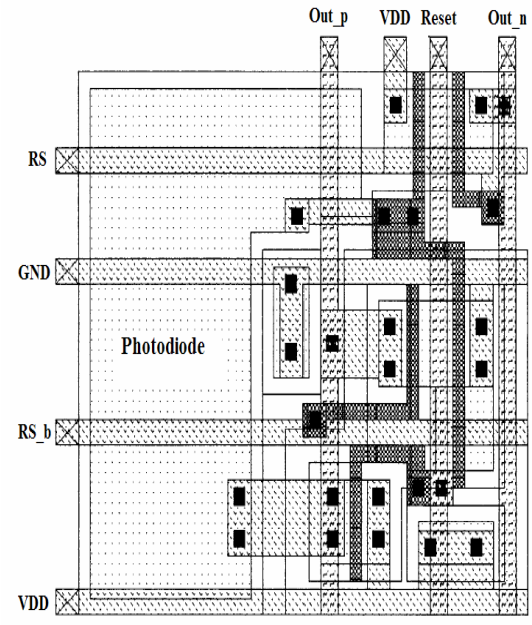

Fig. 18 Layout view of one pixel

Table 1 Performance summary

Process technology	0.35μm SPQM
Pixel Size	17×14 μm^2
Power supply	3.3V ~ 1.8V
Iutput voltage swing	Full swing (V_{DD}=3.3V) 0.2V~1.8V (V_{DD}=1.8V)
Output voltage swing	0.2V~2.8V (V_{DD}=3.3V) 0.4V~1.6V (V_{DD}=1.8V)
Pixel & Read-out power	0.9 μW ~ 8.5 μW
Pixel type	Rail-to-rail Active pixel

5 Conclusion

In this paper, a new rail-to-rail pixel readout architecture has been proposed and verified by HSPICE simulations. The input rail-to-rail pixel architecture in combination with the new readout circuit enable the capability of low voltage operations. The layout size of each pixel is 17um×11.55um. The design of a 64×64 bits CMOS image sensor circuit has been completed with verified satisfactory functions. The proposed CMOS image sensor can extend its operating voltage from 3.3V even down to 1.8V for a 0.35um process. The total power dissipation is 0.528mW at 3.3V supply and down to 0.102mW at 1.8V.

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