Proceedings of the 10th WSEAS International Conference on CIRCUITS, Vouliagmeni, Athens, Greece, July 10-12, 2006 (pp96-101)

A New Phase-Locked Loop with High Speed Phase Frequency Detector and Enhanced Lock-in

HWANG-CHERNG CHOW and NAN-LIANG YEH
Department and Graduate Institute of Electronics Engineering
Chang Gung University
259 Wen-Hwa 1st Road, Kwei-Shan, Tao-Yuan 333
TAIWAN, REPUBLIC OF CHINA

Abstract: - In this paper, we propose a new phase-locked loop design with both a high speed phase frequency detector and an enhanced lock-in feature. The proposed phase frequency detector is simple in its structure and has no glitch output as well as better phase characteristics. Based on simulation results, the proposed phase frequency detector shows satisfactory circuit performance with a very high operation frequency up to 3.5 GHz, but lower phase jitter and smaller circuit complexity as compared to prior art circuits. Furthermore, we present an auxiliary enhanced lock-in system for the phase-locked loop. The proposed mechanism can reduce the lock-time effectively by using the reference clock signal only. Besides, the whole enhanced lock-in circuit performs its operation in one reference clock cycle.

Key-Words: - Phase-locked loop, Phase frequency detector, Lock-in, Glitch, Jitter, High speed

1 Introduction

Phase-locked loop (PLL) circuits are well known and are often used for frequency multiplication, clock synchronization and clock recovery purposes [1-3]. Phase-locked loop circuits can be classified into four types, namely linear PLL, digital PLL, all digital PLL and software PLL. Among them, the main components of a digital PLL circuit comprise a phase frequency detector (PFD), a loop filter (LPF), a charge pump and a voltage-controlled oscillator (VCO), as shown in Figure 1.

The PFD compares both the phase and frequency difference between the reference input signal and the feedback signal. The LPF filters out the high frequency components of the output signal coming from the charge pump. While the VCO

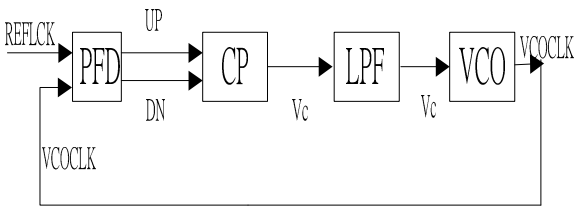

Fig. 1 Digital phase-locked loop

accepts this DC voltage from the low pass filter and then generates a corresponding output digital signal. Once the whole PLL loop becomes stable the output signal is synchronized with the reference input. There is ideally no phase difference. So far, there is much work on the design of the

phase frequency detector in the literature. However, as the application frequency increases, the operation requirement of a high speed PLL is becoming more and more important. Besides a high frequency VCO, a high speed PLL indeed needs a fast phase frequency detector. Therefore, a high speed PFD will be proposed in this paper first, which has better phase sensitivity, dead zone characteristics and maximum operation frequency. Furthermore, we present a simple enhanced lock-in system for the phase-locked loop. The proposed mechanism can reduce the lock-time effectively by using the reference clock signal only.

2 Prior Art

Consider the function of the PFD first. As shown in Figure 2, if the reference signal leads the feedback signal, the PFD will output an UP signal with its pulse width proportional to the phase difference. However, if the reference signal lags the feedback signal, the PFD will output a corresponding DN signal. The PFD usually contains flip-flops in its design, therefore it is either positive edge-triggered or negative edge-triggered. If we classify the PFD based on the state diagram there will be 3-state and 4-state design approaches. We will analyze many prior art PFD circuits [4-10] in the literature and make extensive comparisons between them.

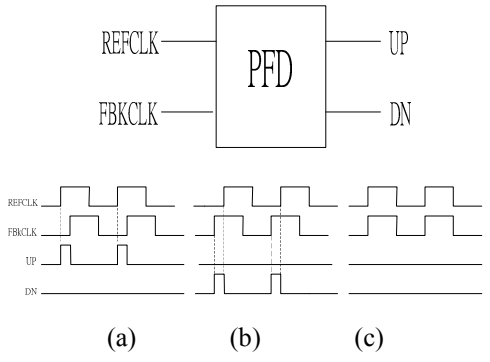

Fig. 2 Operation of PFD (a) lead (b) lag (c) in phase

3 Proposed PFD Design

The proposed PFD, as shown in Figure 3, is obtained by the combination of a 4-state PFD with a latch circuit. When the positive transition of the reference clock REFCLK happens, the voltage level of node U is high while the node D remains low. Therefore, an UP signal is generated and until the transition of the feedback clock FBKCLK happens to turn off this UP control signal. Likewise, when the positive transition of the feedback clock FBKCLK happens, the voltage level of node D is high while the node U remains low. Therefore, a DN signal is generated and until the transition of the reference clock REFCLK happens to turn off this DN control signal. While the transitions of both REFCLK and FBKCLK happen simultaneously the voltage level of both nodes U and D are low. Under this condition no output signal comes out of this PFD. This presented PFD is simple in its circuit structure and has no glitch output.

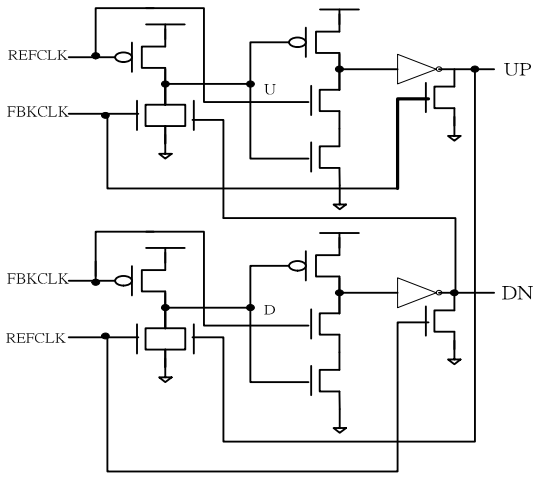

Fig. 3 Proposed high speed PFD

4 Enhanced Lock-in

In the PLL, the VCO generates a corresponding frequency according to the input DC voltage from the low pass filter. However, the output voltage of the low pass

filter is initially zero. Therefore, the output frequency of the VCO will always increase from the lowest frequency limit to the desired frequency for the whole loop to become stable. The lock time may be too long. If there is a suitable method to set an initial voltage to the low pass filter then the PLL lock time will be reduced since the VCO generates its output frequency from a better initial condition. In summary, we need an "initial bias circuit" to pre-charge the low pass filter based on the frequency of the reference clock. As shown in Figure 4 is our initial bias circuit design. The proposed design consists of a LPF network, a pre-charge controller and a pre-charge circuit. We simply provide three initial bias conditions for the low pass filter. That is, if the desired frequency is high then the capacitor is pre-charged to a higher DC voltage. Otherwise, it is set to a medium or lower DC voltage.

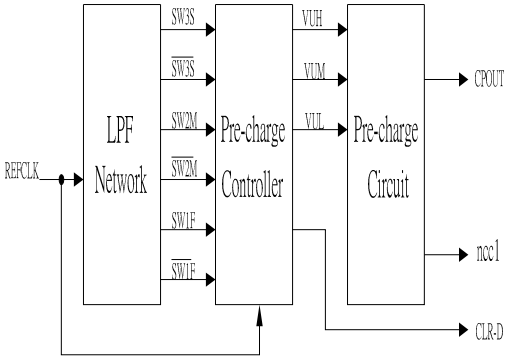

Fig. 4 Proposed lock-in enhanced design

5 Simulation Results

The circuit function of the proposed PFD is examined first. As shown in Figures 5 and 6, both signals have different frequency and phase. The proper UP and DN control signals are generated, respectively. The comparisons of dead zone for other PFDs are given in Table 1 for an input signal with 50% duty cycle.

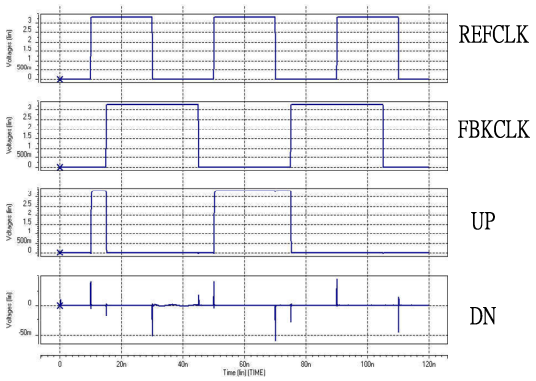

Fig. 5 Different frequency (REFCLK leads)

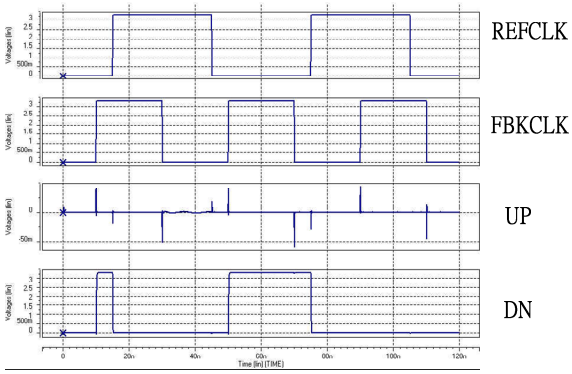

Fig. 6 Different frequency (REFCLK lags)

Table 1 Dead zone comparison

	Dead-zone
PFD-1 [4]	0ns
PFD-2 [5]	0ns
PFD-3 [6]	0ns
PFD-4 [7]	120ps/90ps(UP/DN)
PFD-5 [8]	0ns
PFD-6 [9]	0ns
PFD-7 [10]	0ns
Proposed PFD	4ps/4ps (UP/DN)

As for the maximum operation frequencies of these PFDs, they are shown in Figures 7-9. The proposed circuit has a superior advantage over the existing prior art [4-10]. The whole PLL loop function is verified. The used charge pump is a

differential type circuit and the VCO has its maximum operating frequency up to 1.25 GHz. As for the layout of this proposed PLL, it area is 216.3um×47.85um, as shown in Figure 10.

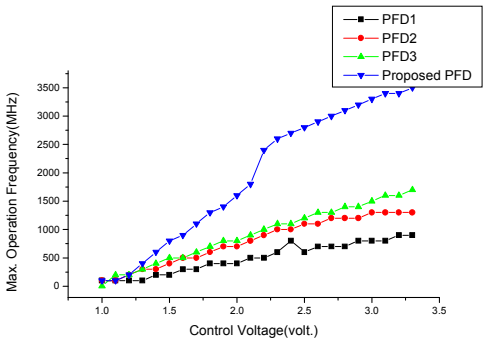

Fig. 7 Maximum operation frequency I

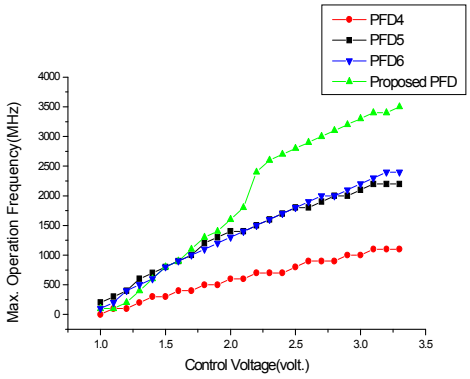

Fig. 8 Maximum operation frequency II

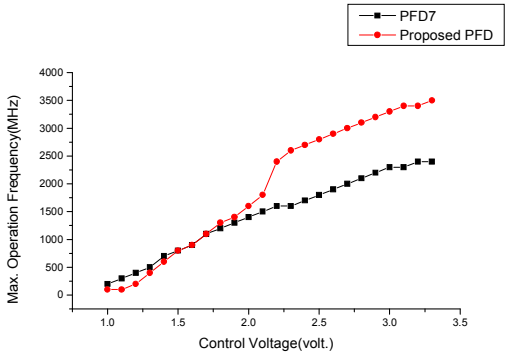

Fig. 9 Maximum operation frequency III

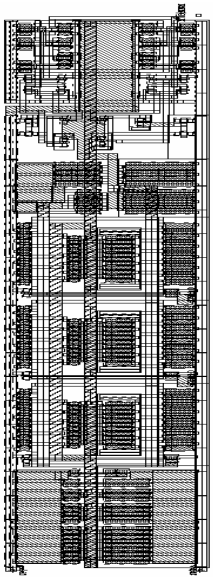

Fig. 10 Complete PLL layout view

The 1.1 GHz whole loop function is illustrated in Figure 11. The operating functions of the presented initial bias circuit are given in Figures 12-14 for a reference input clock at 3.0, 2.5 and 2.0 MHz, respectively. Note that the voltage level of CPOUT is properly set according to the input frequency. The lock time comparison is shown in Figure 15.

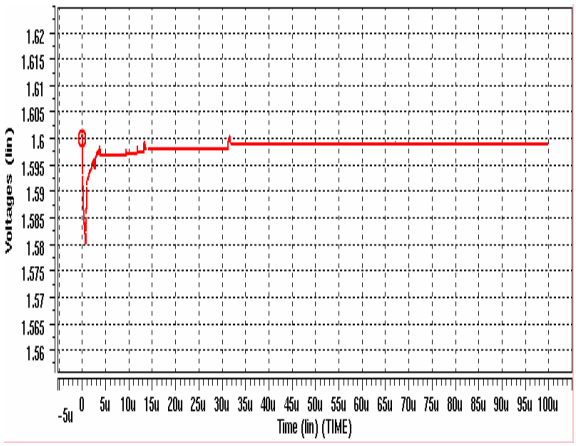

Fig. 11 1.1 GHz PLL whole loop function (Vc)

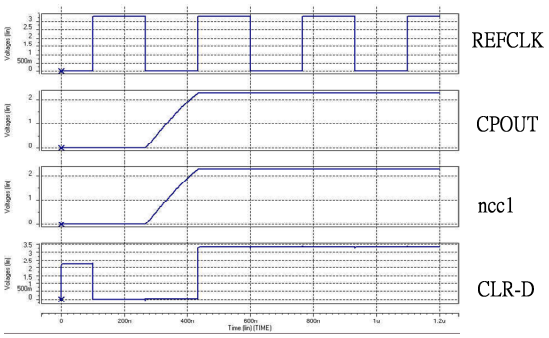

Fig. 12 Outputs of initial bias circuit for reference input clock at 3.0MHz

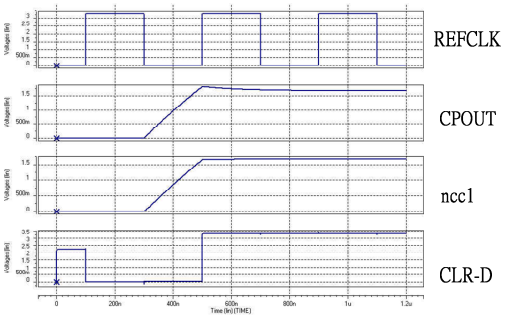

Fig. 13 Outputs of initial bias circuit for a reference input clock at 2.5MHz

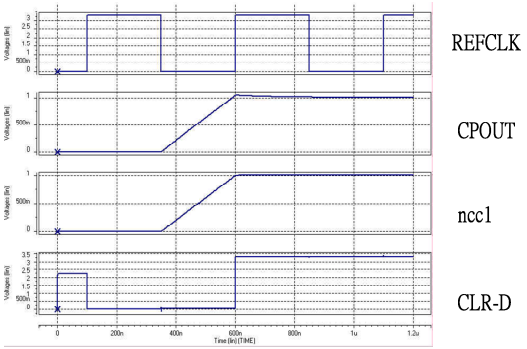

Fig. 14 Outputs of initial bias circuit for a reference input clock at 2.0MHz

Moreover, the measured results from simulations of lock time is improved to 50% as summarized in Table 2. The validity of the proposed enhanced lock-in design is therefore confirmed.

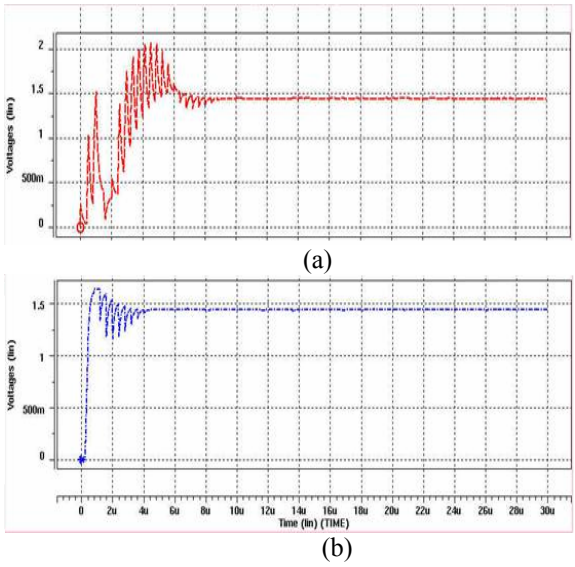

Fig. 15 Lock time comparison (a) without enhanced lock-in (b) with enhanced lock-in

Table 2 Lock time comparison

Reference input clock at 2.5MHz	Lock time (us)	Improvement %
Without lock-in (this work)	9	
With lock-in (this work)	4.5	50

6 Conclusion

In this paper, a high speed phase frequency detector has been proposed for the PLL design. The proposed phase frequency detector is simple in its structure and has no glitch output as well as better phase characteristics. Furthermore, some simulations results by HSPICE are performed based on 0.35um process parameters. Several prior art phase frequency detectors with the proposed one are compared for phase sensitivity, dead zone characteristics and maximum operation frequency. Based on simulation results, the speed of the proposed phase frequency detector is up to 3.5GHz. Moreover, the post-layout simulations for 1.1GHz PLL loop operation has been shown and verified.

Furthermore, a lock-in enhanced design is presented and verified to be effective. The reduction in the lock time can be up to 50%. Therefore, the proposed PLL is very suitable for high speed clock generation with reduced lock-in time.

Acknowledgment: This work was supported by the National Science Council, Taiwan, ROC under contract NSC91-2218-E-182-006.

References:

[1] D.-L. Chen, Designing on-chip clock generators**,** *IEEE Circuits and Devices Magazine*, Vol. 8, No. 4, 1992, pp. 32-36.

[2] B. Razavi, Monolithic Phase-Locked Loops and Clock Recovery Circuits : Theory and Design, *IEEE Press*, 1996.

[3] R. E. Best, Phase-Locked Loops: Design, Simulation, and Applications, 3rd ed. New York, *McGraw-Hill*, 1997.

[4] C. A. Sharpe, A 3-State Phase Detector Can Improve Your Next PLL Design, *EDN Magazine*, 1976.

[5] W.-H. Lee, and J.-D. Cho, A high speed and low power phase-frequency detector and charge-pump, *IEEE ASP-DAC '99*, Vol. 1, 1999, pp. 269-272.

[6] G. B. Lee, P. K. Chan, and L. Siek, A CMOS Phase Frequency Detector for Charge Pump Phase-Locked Loop, *IEEE Midwest Symposium on Circuits and Systems*, Vol. 2, 1999, pp. 601-604.

[7] N. H. E. Weste and K. Eshragrian, Principles of CMOS VLSI Design, 3rd ed., *Addison Wesley*, 2005.

[8] K.-H. Cheng, T.-H. Yao, S.-Y. Jiang, and W.-B. Yang, A difference detector PFD for low jitter PLL**,** *IEEE International Conference on Electronics, Circuits and Systems*, Vol. 1, 2001, pp. 43-46.

[9] S.-O. Jeon, T.-S. Cheung, and W.-Y. Choi, Phase/Frequency detectors for high speed PLL applications, *Electronics Letters*, Vol. 34, No. 22, 1998, pp. 2120 -2121.

[10] H. Kondoh, H. Notani, T. Yoshimura, H. Shibata, and Y. Matsuda, A 1.5-V 250-MHz to 3.0-V 622-MHz operation CMOS phase-locked loop with precharge type phase-detector, *IEICE Trans. Electron.,* Vol. E78-C, No. 4, 1995, pp. 381-388.