

# A novel High Bandwidth Pulse-Width Modulated Inverter

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*Abstract:* The bandwidth of PWM inverters is limited by the output demodulating L-C filter. In order to synthesize complex waveforms and modulate low distortion and high frequency sinewaves the cut-off frequency of the filter must be increased and consequently the switching frequency of the power semiconductors and the losses must be increased also. The output power stage of a single-phase single-supply PWM inverter very often consists of power switches, implemented with an adequate number of parallel-connected semiconductor switches. The separation of the parallel-connected semiconductor switches, that are often used, into groups (or the split of single high power semiconductors in more lower power semiconductor groups) with different drive can produce a multilevel PWM resulting a significant bandwidth increment, reduction of harmonic distortion and weight of the output L-C filter. This paper describes a method that produces a five-level (line-to-line) Sinusoidal Pulse Width Modulation (SPWM). Results show that if the inverter output THD that is caused from the SPWM carrier is reduced by 6dB, then a double bandwidth system is resulted. Furthermore a half weight output LC filter can be used to implement a higher power density system. The inverter output internal resistance is also reduced up to four times compared to the conventional design, when the inverter uses negative feedback.

*Keywords:* Modulated inverters, Pulse width modulation, Harmonics elimination

## 1 Introduction

Power switches used in Pulse Width Modulation (PWM) systems very often consist of a number of parallel-connected semiconductor switches. This can reduce the final cost, since lower power semiconductors are produced in greater quantities, and thus cost less. Moreover, the characteristics of the power system can be optimized, because paralleling power semiconductors may achieve low "ON" resistance and better fit the semiconductor's current rating to the required value. Low input voltage PWM inverters are typical applications of parallel semiconductor switches operation.

In this paper a new way to design a single-phase inverter and to produce a line-to-line multilevel SPWM is described. Multilevel PWM schemes approaches the sinusoidal signal more closely and thus improving harmonic distortion [1]. The generation of a multilevel PWM by using series combination of switches, or voltage sources, is particularly suitable for high voltage and power

applications. In low and medium power applications the multiple voltage sources increase the system complexity and the series-connected switches decrease the efficiency. In previous work in the field, it can be seen that adding two opposite carriers modulated with the same signal, results harmonic elimination around the carrier frequency. Consequently, parallel operation of inverters for multilevel line-to-line voltage output and harmonics cancellation [2] is most suitable for low and medium power systems. This is applicable for current mode inverters. The use of split inductors [3] for current sharing increases the inverter complexity and cost. Negative feedback is possible to be proved very beneficial in waveform synthesizing inverter systems and none of the above designs uses it.

A small change in a conventional SPWM system can result harmonics elimination around the SPWM carrier. This can be achieved with the addition of two opposite carriers that are modulated

with SPWM with the same signal. This approach can be generalized in voltage mode single-phase inverters. This way, the distortion, caused by the harmonics that the modulation introduces, is reduced. Output THD, that is caused from the SPWM carrier, is reduced by 6dB, a half weight output LC filter can be used, and this is possible to reduce the inverter output internal resistance up to four times compared to the conventional design, if the inverter is using negative feedback.

In section 2, of this paper the derivation of the topology and its relation with the conventional SPWM topology is presented. In section 3, the simulation results help the comparison between the SPWM and the multilevel SPWM characteristics. The benefits of the proposed method are discussed in section 4. Finally the experimental results of a prototype inverter are presented in section 5.

## 2 Derivation of the topology

In this paper a generic voltage source inverter is assumed, that utilizes a demodulating second order LC filter. Since the system complexity is critical in a system that has to manage four PWM signals to produce two SPWM signals, it will be assumed an inverter that uses SPWM, produced from two separated components, one of high and one of low frequency, as described in [4]. This approach allows the addition of the two SPWM signals by adding only the high frequency components. This method minimizes the changes on the conventional SPWM system and finally it couples higher frequency signals through the coils. The block diagram of the conventional SPWM system is shown in Fig.1.

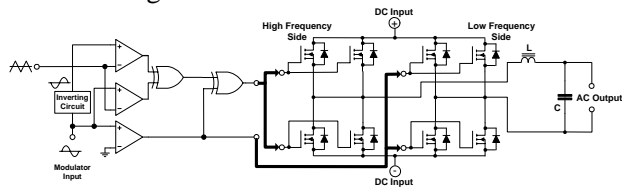


Fig. 1. Conventional SPWM Inverter.

In the conventional SPWM system, a sinewave carrier is modulated by a triangular wave whose frequency is half the carrier frequency. Each MOSFET in Fig. 1 may represent a number of parallel-connected semiconductor switches. To make the differences of the proposed system visible, the conventional SPWM system is converted into an equivalent circuit, shown in Fig. 2.

In Fig. 2, the parallel-connected semiconductor switches of the high frequency side have been

separated in two groups that have the same drive. The outputs of the two groups are coupled with two separate coils, which have been derived from coil L of the conventional SPWM system as was shown in Fig. 1. Since this separation results in an equivalent system, all electrical stresses in Fig. 2 are equal to those of Fig. 1.

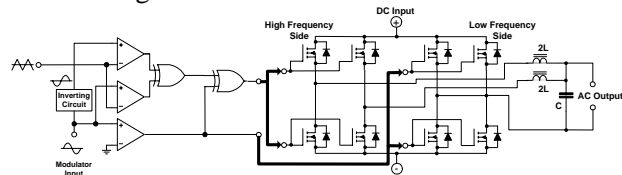


Fig. 2. Equivalent circuit of a SPWM Inverter.

The proposed system is based on the system of Fig. 2 with the difference that the two separate groups on the high frequency side have different drives. The proposed system is shown in Fig. 3.

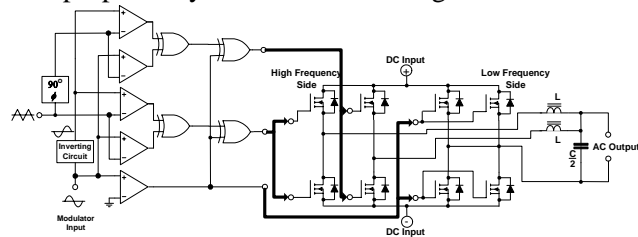


Fig. 3. The Proposed Inverter System

The proposed system has two SPWM modulators, each of which modulates the same signal on a carrier. The two resulted SPWM carriers are generated of two triangular waves with a phase shift of  $90^\circ$ . Because the carriers of the SPWM signals are chosen to have twice the frequency of the triangular wave, the  $90^\circ$  phase shift of the triangular waves results in two SPWM signals with opposite carriers ( $180^\circ$  phase shift). The summing of the opposite carriers eliminates their main components and results a modulation with double carrier frequency of the opposite carriers. The resulting system may have half the coil L and half the capacitor C of the output filter and acts exactly the same as a conventional SPWM system.

The method can be easily used generic voltage source inverters. In the case of motor drive inverters, or other inductive load inverters that use the inductive nature of the load to demodulate the current waveform, the method will produce a reactive current in the demodulating coils. This current will produce additional stress to the power components.

The benefit of the proposed system with the addition of the opposite carriers is the cancellation of the harmonics around the carrier. By removing the capacitor without adding a load, the form of the

output voltage of the system, as simulation and experimental results show, will be a more advantageous modulation type than the conventional three levels SPWM. A five (5) level (multilevel) SPWM with double carrier frequency of each SPWM component is the result of the harmonics cancellation around the carrier. The harmonic spectrum of this modulation is in the order of a three level SPWM with the half amplitude and double the frequency of each SPWM component. The Total Harmonic Distortion (THD) and the first (Eq. 1) and second (Eq. 2) order Distortion Factors are reduced significant it using this technique. All the distortion factors remain lower of those of the conventional system even with a half L and a half C output filter. The reduction of the output filter results a higher bandwidth and higher power density system.

### 3 Simulation Results

In order to verify the output waveform and the modulation harmonics profile, the Spice computer program was used. The frequency of the triangular wave was chosen to be ten times the frequency of the modulated sinewave (Normalized Carrier Frequency,  $F_{nc}=10$ ), because the low normalized carrier frequency produces clear separated pulses and easily visible waveforms. The multilevel SPWM for  $m_f=1$  are shown in Fig. 4. The harmonic spectrum of the waveforms of the SPWM component are shown in Fig. 5 (a). The harmonic spectrum of the waveforms of the Multilevel SPWM of Fig. 4 is shown in Fig. 5 (b).

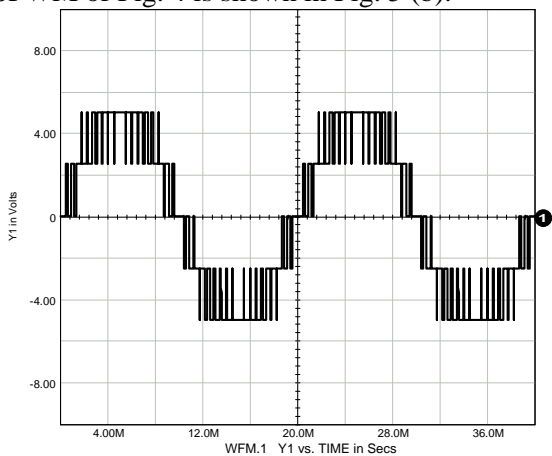
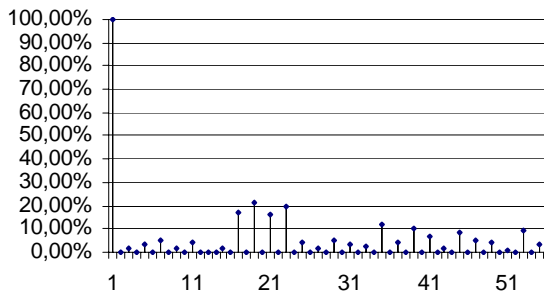


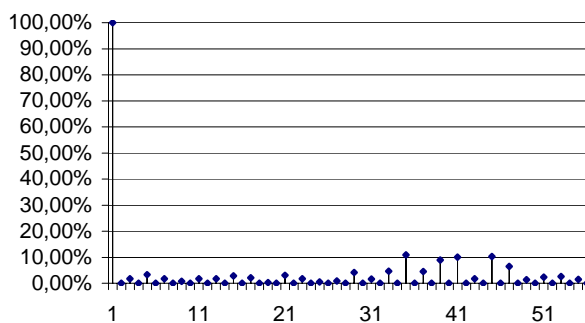
Fig. 4. The Multilevel SPWM ( $F_{nc} = 10, m_f=1$ )

The five levels SPWM has double the carrier frequency ( $4 \cdot F_{nc} = 40$ ) as shown in Fig. 5b and about half the amplitude on the main harmonics of its SPWM components (Fig. 5a). If the modulation factor ( $m_f$ ) is less than 0.5, then the five-level

SPWM is replaced from a three-level SPWM, with double the frequency and half the amplitude of the SPWM components. The modulation factor of this signal is consequently twice the modulation factor of the SPWM components.



(a)



(b)

Fig. 5. Harmonic spectrum of (a) the SPWM component and (b) the multilevel SPWM ( $F_{nc} = 10, m_f=1$ )

$m_f$ \ h	0.2	0.4	0.6	0.8	1
1	0.2	0.4	0.6	0.8	1
$4 \cdot F_{nc} \pm 1$	0.163	0.156	0.007	0.107	0.067
$4 \cdot F_{nc} \pm 3$	0.011	0.067	0.129	0.111	0.009
$4 \cdot F_{nc} \pm 5$			0.030	0.079	0.119
$4 \cdot F_{nc} \pm 7$				0.011	0.050
$8 \cdot F_{nc} \pm 1$	0.078	0.053	0.022	0.004	0.024
$8 \cdot F_{nc} \pm 3$	0.034	0.056	0.044	0.009	0.015
$8 \cdot F_{nc} \pm 5$		0.039	0.041	0.041	0.008
$8 \cdot F_{nc} \pm 7$			0.042	0.029	0.037
$8 \cdot F_{nc} \pm 9$			0.010	0.043	0.023
$8 \cdot F_{nc} \pm 11$				0.016	0.047
$8 \cdot F_{nc} \pm 13$					0.025

Table 1. The normalized Fourier coefficients of the five-level SPWM.

A computer program was developed, to be able to analyze multilevel waveforms. This program can calculate the Fourier coefficients with more accuracy. The five levels SPWM harmonic spectrum contains sideband “clusters” around the carrier harmonics ( $4 \cdot F_{nc}$ ). The calculated normalized Fourier coefficients of the five levels SPWM are listed in Table 1.

For  $m_f=1$  the dominant harmonic (d) of the five-level SPWM is  $d = 4 \cdot F_{nc} - 5$ . This is more than twice the frequency of the dominant harmonic of the three level SPWM ( $d = 2 \cdot F_{nc} - 3$ ). The normalized Fourier coefficients of the five-level SPWM dominant harmonic are about the one half of those of the three-level SPWM.

#### 4 Benefit Analysis

The proposed method gives the expected results using an asymmetrical SPWM system, with one high and one low-frequency side. This is an unbalanced system with all the switching losses on the HF side. The incremented losses will also increase the operating temperature of the power semiconductor switches, and the value of  $R_{DS(on)}$  if the switches are power MOSFETs. Higher temperature operation of power semiconductors will shorten their life significantly. This is the main disadvantage of the proposed method. If slower and cheaper semiconductors are used in the LF side and faster and better-cooled semiconductors in the HF side, and thus it is possible to reduce the problem and the total cost of the inverter.

Another disadvantage of the proposed method is the increase of the power circuit components that comes from the splitting of the output filter coil  $L$  in two coils. Firstly we assume that the coils have a value of  $2 \times L$ . The output filter coil  $L$  is usually wound around a ferromagnetic core that determines the weight and the cost of the coil. The peak energy that the coil  $L$  stores is given by:

$$E_{L_p} = \frac{L \cdot I_{L_p}^2}{2} \quad (1)$$

This energy is stored in the coil core material and determines the core mass. Each of the derived coils has value of  $2 \times L$  and operates with half output current. Thus, the stored energy in each derived coil is given by:

$$E_{2L_p} = \frac{2 \cdot L \cdot \left(\frac{I_{L_p}}{2}\right)^2}{2} \Rightarrow E_{2L_p} = \frac{L \cdot I_{L_p}^2}{4} \quad (2).$$

Each of the derived coils stores half the energy of the initial filter coil. It is concluded that the proposed method does not increase the mass of the coil material and thus the total inverter cost. On the other hand, splitting the filter coil gives a better weight distribution on the printed circuit board (PCB) and it is often the only way to make high-power ferrite core coils using the standard ferrite cores. Sharing the filter coil resistance and inductance improves the current sharing also, and thus the proposed method gives an advantage for using IGBTs in the HF Side.

The amount of the total inductance in a PWM inverter is depended on the inverter application. Constant load inverters may use only a coil for the PWM demodulation. In this case the maximum inverter output current ripple determines the minimum value of the inductance  $L$ :

$$L = \frac{V_s}{2 \cdot f \cdot I_{O_{p-p}}} \quad (3)$$

where:

- $V_s$  is the inverter supply voltage
- $f$  is the PWM carrier frequency and
- $I_{O_{p-p}}$  is the p-p current ripple

Voltage source inverters usually operate for long periods without load, or under low loading. In this case low no-load power dissipation is acquired and an LC filter is needed in order to achieve an acceptable distortion in the output waveform. The desired attenuation of the PWM determines the exact filter topology [5]. Usually a single  $L$  and a single  $C$ , LC filter is enough and it is preferred because it gives the minimum HF reactive loading. The filter cutoff frequency is properly determined to produce the desirable PWM carrier attenuation. The filter reactive current is minimized as the inductance is increased and the capacitance is reduced. This way the constant power consumption of the inverter is also minimized, but on the other hand, the inverter output internal resistance is increased due to the significant impedance of the coil  $L$ , at the low frequency (50Hz). The use of negative feedback reduces the inverter output internal resistance and is a good choice for these types of inverters.

Using the proposed method, the harmonic distortion, which is produced from the carrier sidebands at the inverter output, is reduced by 6dB because of the half carrier amplitude. The carrier

frequency doubling can further reduce the harmonic distortion by 6dB if a first order filter demodulation is assumed or by 12dB if a second order LC filter is assumed. The decrease of the inverter output distortion permits the inverter output filter to be redesigned. Even if the filter cutoff frequency is doubled, the HF component is still reduced by 6dB. The output filter cutoff frequency is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (4)$$

Doubling the output filter cutoff frequency can be achieved by reducing to one half the values of the filter coil and the filter capacitor. The reduction of the filter coil will increase proportionally the reactive HF current at the HF half bridges. This disadvantage can be overcome by the reduction of the low frequency reactive current. Thus, the coil reduction is possible to increase the stress at the power components of the HF side half bridges. However, the increment of this stress is not usually significant compared to the maximum output load stress and will not necessary affect the power semiconductors size. It must be noted that the proposed method results in a significant reduction of the HF current in the LF half bridge. The reduction of the output filter coil to the one half reduces the coil mass to the one half resulting in a higher power density system. Also it decreases almost proportionally the inverter internal resistance while maintaining the double filtering cutoff frequency under any load. This is a significant benefit for inverters that use negative feedback, the effective feedback higher frequency is doubled and the feedback gain at the output sine wave frequency (50Hz) can be also doubled. Doubling the feedback gain will in turn, reduce to one half the inverter output internal resistance. Consequently, if the inverter uses negative feedback, the proposed method could achieve reduction up to 1/4 in the inverter internal resistance.

### 5 Laboratory Implementation and Experimental Results

In order to verify the theoretical predictions and address the problems that appear in a real system, an experimental single-phase, three level phase voltage and five-level SPWM line-to-line voltage prototype inverter was constructed and tested in the laboratory. Since the system complexity is critical and there is need to minimize the high number of components needed to have a well-controlled output waveform, an equivalent of the above

modulator is used. A pair of double frequency (rectified) triangular waves is compared with the rectified sine wave to produce the SPWM components. This results a reduction of comparators and logic gates. The experimental inverter modulator block diagram is shown in Fig. 6.

The experimental design uses one-cycle control [6], in order to be immunized of input voltage variations and to have a stable open loop gain and thus to have the ability to be controlled of a high-speed feedback loop. The effect of using one-cycle control and fast negative feedback in PWM inverters reduces the output internal resistance and the output harmonic distortion significantly [4,7].

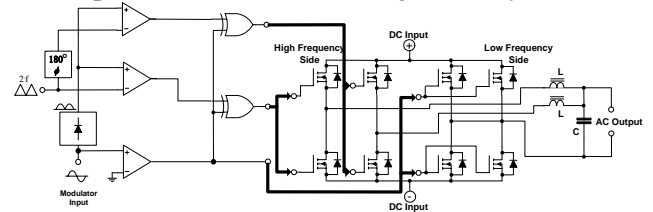


Fig. 6. The experimental inverter modulator block diagram.

The supplying inverter voltage is about 350V. The HF bridge sides use fast IGBTs. The improved current sharing of the proposed method allows their mutual contribution without oversizing them. On the other hand, IGBTs are of lower cost and higher efficiency when working in high temperature, compared to power MOSFETs. This way the HF operation losses do not affect the inverter efficiency significantly.

The minimum measured power consumption of the prototype inverter was less than 15W and the efficiency was more than 93% for resistive loads in the range from 400W to 650W. The output voltage drop from no load to 650W was negligible (less than 0.5V<sub>RMS</sub>).

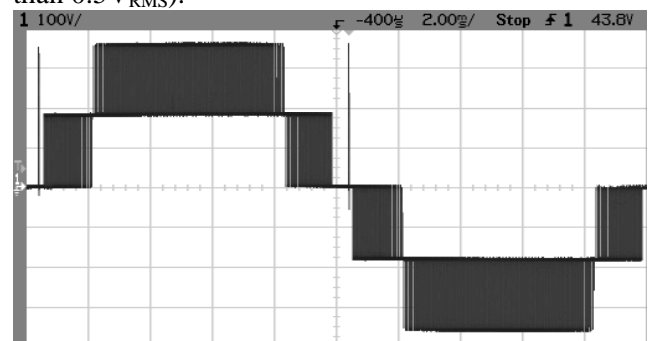


Fig.7. The five levels SPWM voltage waveform at the inverter output without filtering.

Disconnecting the capacitor of the output filter it is possible to obtain the waveform of the five levels SPWM shown in Fig. 7.

The feedback loop that is used is minimum-time (O-type) and the loop gain is 4.7 compensated through a single pole at 50Hz. The loop gain, even though low, results a low output internal resistance and a stable feedback under almost any possible type of load. The output waveform under 600W load is shown in Fig. 8. The result is very close to pure sinewave and the most distorted part is around the zero crossings. This crossover-like distortion is caused from the dead-time and the slightly different zero levels of the triangular waves and the rectified sinewave. This zero level difference is caused from the one-cycle control circuitry. The half bridge driver integrated circuits have a constant dead-time of 500nSec. The low loop gain and the limited feedback bandwidth that is used, are the reason that the feedback does not improve significantly this kind of distortion.

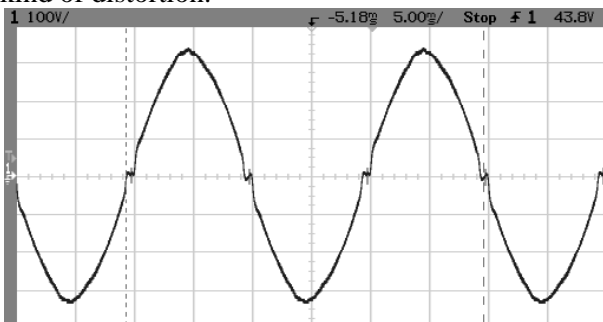


Fig. 8. The inverter output waveform with 600W load.

## 6 Conclusions

A method was developed that produces a multilevel line-to-line output high bandwidth inverter, with multiple carrier frequency and reduced carrier amplitude. The high bandwidth of this method makes it suitable for high voltage and high power waveform synthesizing. In an SPWM inverter the main components of weight and cost are the demodulating filter coil. The LC filter used in this method can be implemented with a much smaller coil. The reduction of the output filter coil is beneficial for the weight, the cost and the performance of the inverter.

When feedback is used, the multiple carrier frequency also allows higher feedback gain-bandwidth product. The prototype inverter constructed in the laboratory had high efficiency and showed excellent performance, validating the theoretical analysis.

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