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A New Quadratic Boost Converter with PFC Applications

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Abstract: - A novel quadratic boost converter capable of delivering a high output voltage is introduced. Dc-dc operation in continuous conduction mode (CCM) and discontinuous inductor current mode (DICM) are analyzed. A simple and versatile feedforward (FF) circuit is proposed in order to be used with the new converter when operated in CCM. Another application is the use of the converter as a power factor correction (PFC) circuit. At low power levels DICM operation is chosen, because of the converter natural capability of emulating a resistor at low frequency. The PFC solution at high power levels is based on CCM operation of the converter, in conjunction with the proposed feedforward circuit. Design equations, simulation results and merit parameters are presented for all the investigated topologies.

Key-Words: - converter synthesis, quadratic converters, feedforward, power factor correction, simulation.

1 Introduction

In dc-dc conversion applications that require a large range of input and/or output voltages, conventional PWM converter topologies must operate at extremely low or high duty ratios *D*. In large step-up applications the maximum attainable conversion ratio is limited by the degradation in efficiency as *D* approaches 1. This type of applications include high-voltage/low current applications such as TV CTR's, lasers, X-ray systems, ion pumps, electrostatic systems, etc. The solution of a BUCK converter followed by a push-pull multiplier has the drawback of using three active switches and therefore a complex control. Moreover, as the input current is discontinuous an input filter is invariably required. As far as conversion efficiency is concerned, it is quite clear that a single-stage converter is always a better choice than a two-stage converter [1].

Conversion range can be extended significantly if conversion ratio $M(D)$ has a quadratic dependence on duty cycle.

The novel single-stage BOOST-type quadratic converter proposed in the paper is suitable to provide a high voltage, while maintaining a continuous input current. In Section 2 CCM and DICM operation modes are analyzed. A simple but effective feedforward circuit for the new converter is proposed in Section 3. Two applications of the converter in performing PFC at low and high power levels are revealed in Section 4. The theoretical concepts are verified by simulation in Section 5, while Section 6 is devoted to conclusions.

2 The new Quadratic Boost converter

It is known [1], [3] that quadratic converters cannot be realized with less than two capacitors, two inductors and four switches, but the number of transistor switches can be reduced to one. The technique based on rotating basic switching cells [2] was employed here for deriving the new quadratic BOOST topology presented in Fig. 1. In CCM,

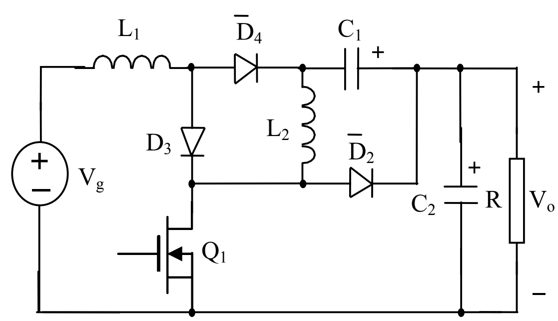

Fig. 1. The new quadratic BOOST converter topology.

during the first topological state, transistor Q_1 and diode D_3 are simultaneously on, while D_2 and D_4 are off. In the second topological state Q_1 and D_3 are off, while D_2 and D_4 conduct. This is denoted by the negation sign accompanying them. Obviously, the duty cycle *D* is related to transistor Q_1.

Writing the volt-second balance across the two inductors the static conversion ratio *M* is found:

$$M = \frac{V_O}{V_g} = \frac{1}{(1-D)^2} \tag{1}$$

thus revealing the quadratic nature of the converter.

Given the input voltage, the output voltage and the output power, the average semiconductor currents and voltage stresses are presented in Table 1. The stresses are computed in CCM, assuming that ac ripples in inductor currents and capacitor voltages are negligible. For comparison, the same stresses in the classical BOOST converter operating under the same conditions are provided in Table 2.

V_{Q1}	V_o
I_{Q1}	$P_o\left(\frac{1}{V_g}-\frac{1}{V_o}\right)$
V_{C1}	$V_o\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
V_{C2}	V_o
I_{L1}	$\frac{P_o}{V_g}$
I_{L2}	$\frac{P_o}{V_o}\sqrt{\frac{V_o}{V_g}}$
V_{D2}	V_o
I_{D2}	$\frac{P_o}{V_o}$
V_{D3}	$V_o\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
I_{D3}	$\frac{P_o}{V_g}\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
V_{D4}	$V_o\sqrt{\frac{V_g}{V_o}}$
I_{D4}	$\frac{P_o}{V_o}\sqrt{\frac{V_o}{V_g}}$

Table 1. Voltage and current stresses in the proposed quadratic BOOSTconverter.

V_Q	I_Q	V_C	I_L	V_D	I_D
V_o	$P_o\left(\frac{1}{V_g}-\frac{1}{V_o}\right)$	V_o	$\frac{P_o}{V_g}$	V_o	$\frac{P_o}{V_o}$

Table 2. Voltage and current stresses in classical BOOST converter

Comparing the results in the two tables it can be easily seen that for Q_1 and D_2 the voltage stresses are the same as the transistor and diode stresses in the classical BOOST converter, while for D_3 and D_4 the voltage stresses are lower than in the classical converter. Other converters with a BOOST type or BUCK-BOOST type characteristic are reported in [1], [2] and [3]. However, except for one converter in [2], no other converter exhibits nonpulsating input current, which is and important feature when used as a PFC circuit as will be seen in section 4.

As three passive switches are present in the converter, theoretically DICM modes can be related to any of the diodes. However, only D_2 and D_4 can induce DICM, as the current through D_3 has a positive slope during the first topological state. It can be demonstrated in a classical manner that the DICM operation induced by D_4 is quantitatively given by the condition:

$$\frac{2L_1 f_s}{R} \le D(1-D)^4 \quad (2)$$

In case of DICM operation because of D_2, the condition becomes:

$$\frac{2L_2 f_s}{R} \le D(1-D)^2 \quad (3)$$

As during its on state diode D_1 current equals i_{L1}, it results that in DICM due to D_1, the shape of the input current is the same as in the conventional BOOST converter. The input inductor current and diode D_4 current in DICM are presented in Fig. 2.

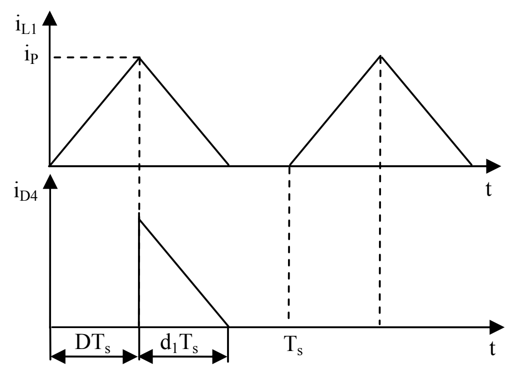

Fig. 2. Input inductor and diode D_4 current waveforms.

3 A Feedforward Circuit for CCM operation of the new converter

For switching converters feedforward compensation is effective in reducing effects of source disturbances on converter outputs and improving steady-state and dynamic responses. A converter with FF behaves at low frequencies as a linear power amplifier with constant gain independent of operating conditions.

In deriving the FF controller let us impose the average output voltage V_o to be equal to the control voltage v_m multiplied by a constant gain A:

$$V_o = A \cdot v_m \quad (4)$$

On the other side, the input and output voltages are related by the static conversion ratio given by (1).

From (1) and (4) it results immediately that:

$$v_m(1-D)^2 - \frac{v_g}{A} = 0 \tag{5}$$

For the proposed converter a leading-edge (LE) modulator is proposed [5]. Although a trailing edge modulator could also be used, this choice is more convenient because of its simplicity. As it is known, the modulator function is found from (5) if we let $D \to 1 - \frac{t}{T_s}$, resulting in:

$$v_m\left(\frac{t}{T_s}\right)^2 - \frac{v_g}{A} = 0 \tag{6}$$

It can be seen that in the modulator function (the right hand side of (6)) the term $v_m\left(\frac{t}{T_s}\right)^2$ is present.

Based on the observation that the control voltage v_m is a slow varying signal compared to the switching frequency (ractically, in open loop operation v_m is constant), the following approximation is valid:

$$v_m\left(\frac{t}{T_s}\right)^2 \cong \frac{1}{\frac{T_s}{2}}\int_0^t\left(\frac{1}{T_s}\int_0^t v_m(u)du\right) \tag{7}$$

Equation (7) clearly suggests that implementation of the term $v_m\left(\frac{t}{T_s}\right)^2$ consists of a cascade of two integrators with reset having the time constants equal to the switching period T_s and half of the switching period respectively. The practical implementation is shown in Fig. 3. Beside the two integrators, only a comparator and a flip-flop are needed. Thus the FF circuit can be easily built on an integrated circuit or with general-purpose components such as comparators, flip-flops and operational amplifiers. One can easily derive that for the architecture in Fig. 3 the output voltage is:

$$V_o = \left(1 + \frac{R_1}{R_2}\right) \cdot \frac{1}{2R_3C_3R_4C_4 f_s^2} \cdot v_m \tag{8}$$

4. Operation as a power factor correction circuit

The operation in DICM due to D_4 and the waveforms in Fig. 2 suggest the possibility to use the converter as an “automatic” or “natural” current shaper when operating in DICM. This is a simple solution at low power levels. The averaged input current, $\bar{i}_g$, can be calculated from Fig. 2 under the quasi steady state assumption [6] and constant voltage over C_1:

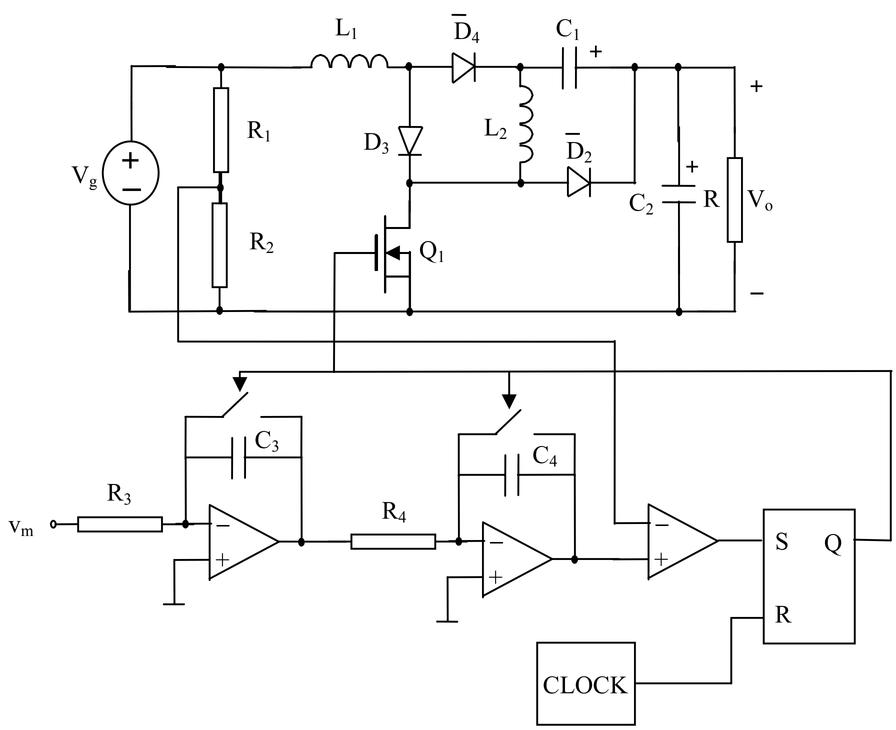

Fig. 3. The new quadratic BOOST converter and the feedforward circuit.

$$\bar{i}_g = \frac{v_g}{R_e} \cdot \frac{1}{1 - \dfrac{V_M}{V_o - V_{C_1}} |\sin \omega t|} \qquad (9)$$

where the emulated resistance is:

$$R_e = \frac{2L_1 f_s}{D^2} \qquad (10)$$

From (9) the power factor (PF) and the total harmonic distortion coefficient (THD) as a function of the ratio $(V_o - V_{C1})/V_M$ are represented in Fig. 4.

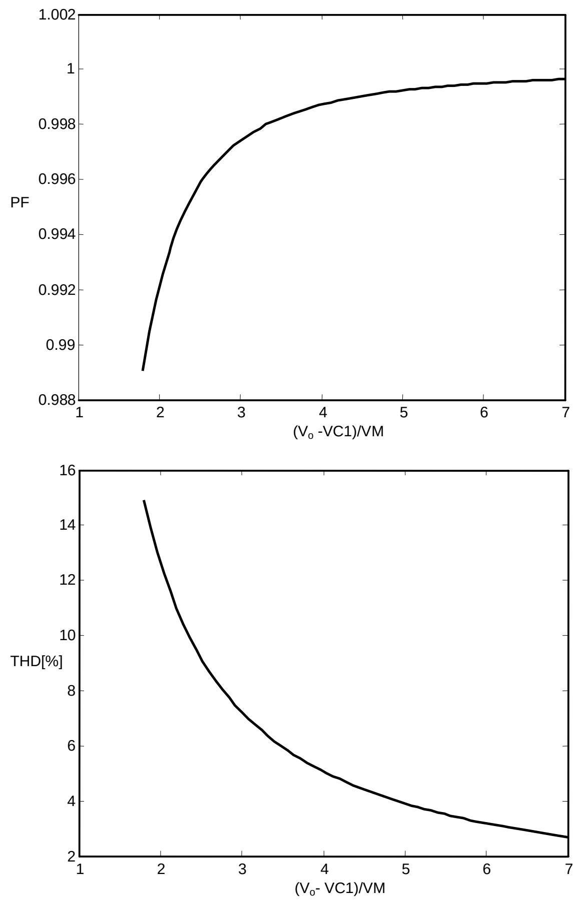

Fig. 4. Power factor and input current TDH as a function of the ratio $(V_o - V_{C1})/V_M$ in DICM.

It can be seen that good PF and THD can be obtained when $(V_o - V_{C1})/V_M > 2.5$, which in practice can be easily achieved.

At high power levels DICM operation is unacceptable because of the high current peaks. CCM operation is however possible using the proposed FF controller with only minor modifications. This can be explained taking into account that at low frequencies the averaged value of the input inductor current, $\overline{i_{L_1}}$, is proportional to the input voltage v_g because of the PFC operation:

$$\overline{i_{L_1}} = \frac{v_g}{R_e} \qquad (11)$$

As the line frequency is well below the switching frequency, the input voltage of the dc/dc converter can be approximated to be constant in a few consecutive switching periods. That is the converter operates in the quasi-steady state [8]. Hence (1) is still valid with $M \to m(t)$ and $D \to d(t)$, that is:

$$m(t) = \frac{V_o}{v_g(t)} = \frac{1}{[1 - d(t)]^2} \qquad (12)$$

From (11) and (12) it results immediately that

$$\frac{V_o}{R_e}(1 - d)^2 - \overline{i_{L_1}} = 0 \qquad (13)$$

Denoting by R_s the current transducer transresistance, (13) can be written in the form:

$$v_m (1 - d)^2 - R_s \overline{i_{L_1}} = 0 \qquad (14)$$

where the control voltage v_m is given by:

$$v_m = \frac{R_s}{R_e} V_o \qquad (15)$$

Comparing (5) with (14) it is obvious that the same controller as in Fig. 3 can be used, the only modification being the replacement of the divided input voltage with a voltage proportional to the averaged input current.

Inductor L_1 is chosen imposing CCM or DICM operation over the whole line half cycle when operated as a PFC circuit. Design equations can be derived as in [4] and they are given below.

For DICM operation:

$$L_1 \le \frac{V_M^2}{4P_o f_s}\left(1 - \sqrt{\frac{V_M}{V_o}}\right) \qquad (16)$$

For CCM operation:

$$L_1 \ge \frac{V_M^2}{4P_o f_s} \qquad (17)$$

5. Simulation results

All simulations were performed using the CASPOC package (Simulation Research) [7]. First the new quadratic BOOST converter with feedforward, similar to the architecture presented in Fig. 3, was simulated. Converter parameters were:

$$L_1 = 237\mu H;\ L_2 = 415\mu H;\ C_1 = C_2 = 10\mu F;$$
$$R = 100\Omega;\ f_s = 40kHz;$$
$$v_m = 3V;\ R_1 = 90k\Omega;\ R_2 = 10k\Omega;\ R_3 = R_4 = 2k\Omega;$$
$$C_3 = 12.5nF;\ C_4 = 6.25nF$$

The input voltage was forced to vary with a square waveshape between 8V and 14 V. The simulation results are shown in Fig. 5. It can be seen that after

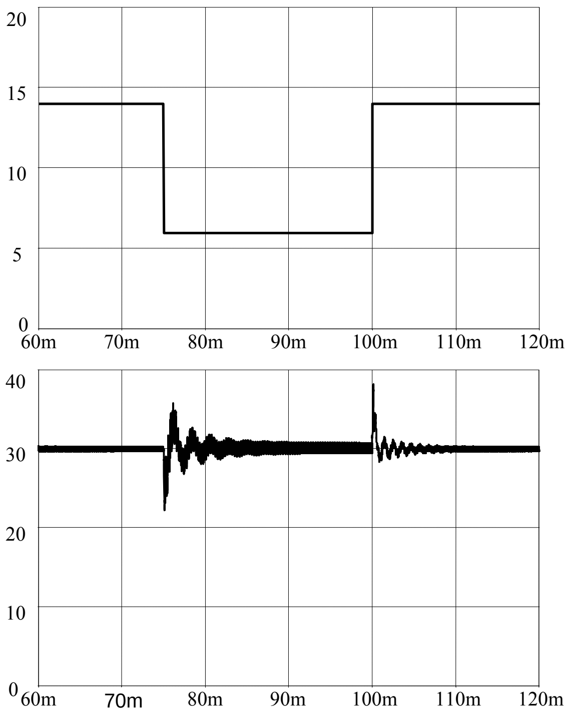

Fig. 5. Dynamic operation of the quadratic BOOST converter with FF. Input voltage (up) and output voltage (down).

short transients the output voltage tightly follows the prescribed 30V value.

Then the converter was simulated in a PFC application with DICM operation. The parameters of the PFC circuit were:

$$V_M = 70V; L_1 = 30.6\mu H; L_2 = 0.5mH; C_1 = 1\mu F;$$
$$C_2 = 470\mu F; P_o = 40W; V_o = 400V; R = 100\Omega;$$
$$f_s = 40kHz; D = 0.2;$$

After the uncontrolled bridge supplying the converter, a small high frequency filter with L_F=80µH and C_F=2µF was used, in order to suppress the high frequency components from the input current which are large in DICM. In Fig. 6 the input voltage and current waveforms are presented. The expected output voltage of 800 V was confirmed by the simulation which provided an output voltage of 806 V. It can be seen that qualitatively the input current has a closely sinusoidal shape and tightly follows the input voltage. The input current total harmonic distortion (THD) coefficient was 2.4%, while unity displacement power factor was found. An excellent total power factor of 0.998 was achieved.

In order to verify the feasibility of a PFC circuit using the new quadratic converter operated in CCM, a PFC circuit employing the same controller structure as that in Fig. 3, but using the input inductor current as the second input was simulated. The circuit parameters were the following:

$$V_M = 169.7V; L_1 = 250\mu H; L_2 = 400\mu H; C_1 = 1\mu F;$$
$$C_2 = 2200\mu F; P_o = 1000W; V_o = 400V; R = 160\Omega;$$
$$f_s = 40kHz; v_m = 2.8V$$

As the converter is CCM operated, no additional high frequency filter is needed. The simulated waveforms are shown in Fig. 7, qualitatively revealing excellent operation. The resulted average output voltage was 398V, in accordance to the theoretical considerations. The input current exhibited a THD of 9.2% and the total power factor of the system was 0.995.

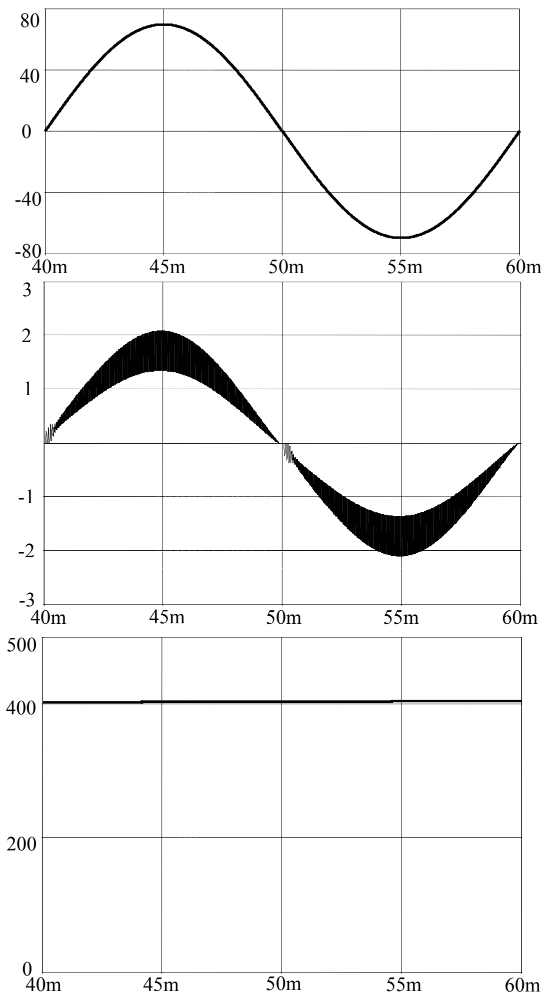

Fig. 6. PFC operation of the new converter in DICM mode. Input voltage, input current and output voltage (this up to down order).

6. Conclusion

A novel quadratic BOOST converter is proposed. Containing only a single transistor and three diodes, the converter can be easily controlled. Moreover, because the minimum off-time is much less restrictive, the converter can operate at a relatively high frequency (500 kHz). High output voltages can be obtained with the same transistor stresses as in the conventional BOOST topology. A feedforward circuit is developed to be used with the proposed converter. It consists of only two integrators, one comparator and a flip-flop and therefore it can be implemented on an integrated circuit or with general-purpose components. Compared to other quadratic converters with BOOST or BUCK-BOOST type characteristics reported, the proposed solution has the benefit of the presence of an inductor in series with the input. This is one of the reasons why the proposed converter is well suited for PFC applications. At low power levels DICM operation of the converter can be exploited because of its natural property to be an “automatic” current shaper. This solution leads to a very simple control, without a current loop. At high power levels PFC can be achieved employing CCM operation and using the proposed controller. Design equations, CCM and DICM operation conditions are provided both for dc/dc and for PFC operation in order to quickly design the required topology.

The simulation results confirmed all the theoretical predictions regarding the converter, the feedforward controller and the two PFC applications.

Thus the new converter together with the proposed controller provide simple solutions for wide range dc/dc applications and for low or high power levels power factor correctors.

Future work will focus on the development of large signal averaged models and small signal modeling and analysis of the converter.

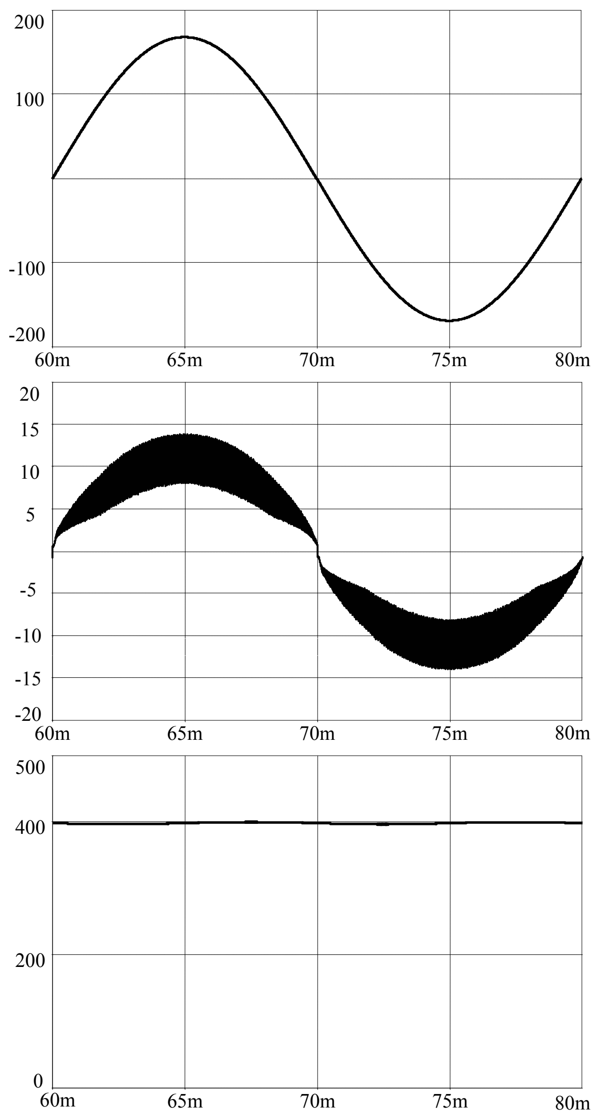

Fig. 7. PFC operation of the new converter in CCM, using the proposed integral controller. Input voltage, input current and output voltage (this up to down order).

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