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Class-AB Square Root Domain Filter

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Abstract: - This paper presents a new class AB programmable square-root domain (SRD) filter. The main advantages of the proposed circuits are low power consumption, wide input dynamic range with small standby current and potential for low-voltage operation. Simulation results confirm the validity of the proposed design technique and the high performance of the proposed circuits.

*Key-Words: S*quare-root domain, SRD filter, commanding filter, Log Domain filter

1. Introduction

One of the figures of merit of a filter is the dynamic range; this is the ratio of the largest to the smallest signal that can be applied at the input of the filter while maintaining certain specified performance. The dynamic range required in the filter varies with the application and is decided by the variation in strength of the desired signal as well as the strength of unwanted signals that are to be rejected by the filter.In conventional filter realizations, e.g. gm-C filters, the signal voltage swings are limited by the available supply voltage. Since these filters are based on linear elements, the signal current swings are also limited directly by the supply voltage. A possible solution to overcome the limited signal current swings is to employ companding. By exploiting the nonlinear concave voltage to current characteristic of the bipolar transistor or the MOS transistor, the voltage swings in a companding filter are much smaller than the current swings. Thus, larger signal swings are possible in a companding filter relative to filters based on linear elements, which is beneficial with respect to the dynamic range. Despite the local nonlinearities, companding filters can have an overall linear transfer function [1-6].Therfore, in addition to low voltage operation, the companding techniques provide the most effective use of the available current, which make it also attractive for low power operation.

An Interesting example of companding filter are the log-domain filters, which are inherently instantaneously companding [1,7,8]. Log-domain filters exploit the exponential law describing the bipolar transistor, or the MOS transistor in weak inversion, to compress the input current of the filter and also to implement multiplications of currents according to the translinear principle [9].

In CMOS technology Square-root domain filters are preferred to log-domain filters because the latter suffers from limited speed of operation and threshold voltage mismatches of the weakly inverted MOSFETs. A number of SRD-domain circuits, including integrators, oscillators, etc., were presented in the literature [10-16].

2. Principle of commanding Integrators

Fig. 1 shows a linear integrator wheres *u*, and *x y* denote the input, the output and the state variable respectively. The state variable description of this system is given by

$$dx/dt = ku \quad (1)$$

$$y=x \quad (2)$$

In [3,17,18], it is shown that the input-output relationship given above can be

obtained in another system with a transformed state variable *v*. Let the transformation be described by

$x = f(v)$ (3)

where *f* is a continuous monotonic nonlinearity. Substituting (3) into (2) and (1), using the relation $df(v)/dt = f'(v)dv/dt$ and rearranging the terms, we obtain the state equations of the system in terms of the transformed state variable *v*.

$dv/dt = k\,u / f'(v)$ (4)

$y=f(v)$ (5)

Fig. 1(b) shows the realization of this transformed system. The input u is divided by *f(v)* before being fed to the integrator. The integrator is followed by the nonlinearity *f(v)*. The input-output behavior of this system is identical to that of the integrator in Fig. 1(a). Because of the presence of the nonlinearity *f(v)* in the system, this is an externally linear, internally nonlinear integrator. An expanding nonlinearity *f(v)* has a slope *f'(v)* that increases with increasing *v*. The input (amplifier) would thus have a gain *1/f'(v)* that decreases with increasing *v*.

If *f* is an expanding function, the variation of *v* for a given variation of *x* will be less than for a linear F. Hence, with regard to the overall transfer function, the only demands made on F and F' are that both functions are integratable and that *f* is expanding. Therefore, the exact implementations of *f* and *f'* must be based on other important design aspects, such as dynamic range, bandwidth and power efficiency, all being major design aspects in a low-voltage low power environment.

The distinctive property of current mode circuits is that current is the magnitude processed, whereas voltages at the circuit nodes have only a marginal interest. In particular, they no longer need to be linearly related. This fact is exploited by the voltage companding circuits, a particular case of current-mode circuits where internal voltages are related to the currents according to a nonlinear compressing law. The internally compressed voltages relax the supply voltage requirements for a given dynamic range. Depending on the compressing law, Log–Domain [8] (logarithmic compression) or Square-Root Domain [14] (SRD or $\sqrt{x}$-domain, square-root compression) circuits, among others, are obtained. The resulting building blocks are based on the exploitation of the exponential law of bipolar (or MOS in weak inversion) transistors (Log-Domain). or the quasi-quadratic law of MOS transistors in strong inversion and saturation (SRD) leading to rather simple topologies. Such building blocks *must* be nonlinear in a large-signal sense, implementing an accurate nonlinear function for input and output swings as large as possible.[17].

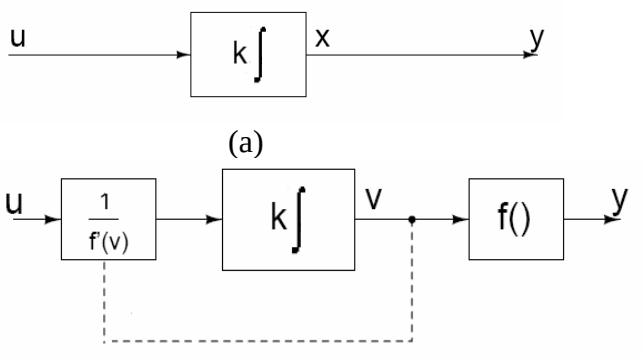


Figure 1: (a) linear integrator, (b) companding integrator

3. Square-root domain (SRD) filter

For SRD filtering The expander could be realized using a MOSFET in in strong inversion and saturation region whose I-V relationship is parabolic and is represented as:

$$i_{out} = f(v) = \frac{\beta}{2}(V_{GS} - V_t)^2 \quad (6)$$

where

$$\beta = u_n C_{ox} \frac{W}{L} \quad (7)$$

stands for transconductance parameter and V_t the threshold voltage of the device.

Fig. 2 shows the SRD low pass filter that can be obtained from the general block diagram shown in Fig. 6 when f(v) is a parabolic.

$$I_{COMP} = \frac{I_{IN}}{f'(v)} = \frac{I_{IN}}{\beta(v_{GS} - V_t)} = \frac{I_{IN}}{\sqrt{2\beta I_{out}}} \quad \textbf{(8)}$$

In the literature [12, 13, 18], three ways for implementing the current compressor in (8) are presented. In Fig. 3(a), a square-rooted version of I_{out} scaled by I_2 is applied to a current-mode multiplier/divider to generate (8). The numerator is just I_{in} , scaled by another current $I1$. Hence, the resulting nonlinear transconductor can be both linearly and nonlinearly tuned via bias currents $I1$ and $I2$, respectively. The multiplier/divider can be designed with either two squarer/divider cells [12] or with geometric-mean and squarer/divider cells [13]. Figure 3(b) shows another approach, where a squarer/divider is used to process I_{in} and I_{out} respectively, and a geometric mean cell is used to produce (8).

The nonlinear current compander in (8) can also be achieved based on the large-signal operation of class-AB linear Transconductors as shown in Fig.3 C. There are several methods to obtain the basic transconductor topology, each one using different approaches [19]. Among them, the best suited to our objectives are those based on the cancellation of nonlinear terms from a properly manipulated algebraic nonlinear V-I characteristic, so that higher-order terms cancel out yielding an ideally linear V-I dependence over a wide range. Various techniques follow this approach, e.g., the multiplier class [20] where a transconductance tunable by a voltage is obtained, and that described in [21], where Tran conductance is proportional to the square root of a current, and is therefore best suited to the former strategy. Figure 4 shows the basic idea of such a transconductor. Assuming that all transistor operate in strong inversion and saturation:

$$I_1 = \frac{\beta}{2}(v_1 - v_2 + V_x - V_{th})^2 \quad (9)$$

$$I_2 = \frac{\beta}{2}(v_2 - v_1 + V_x - V_{th})^2 \quad (10)$$

$$I_{GM} = I_1 - I_2 = 2\beta V_X (v_1 - v_2) = \sqrt{8\beta I_B}(v_1 - v_2) \quad (11)$$

Figure 5 shows the resulting first order SRD filter. This approach offers simplicity, and less power consumption than former SRD filter [22].

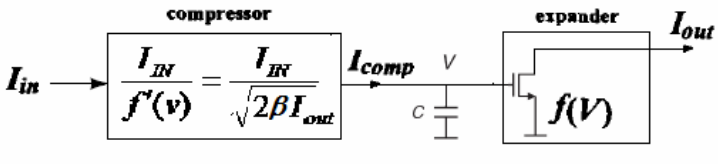
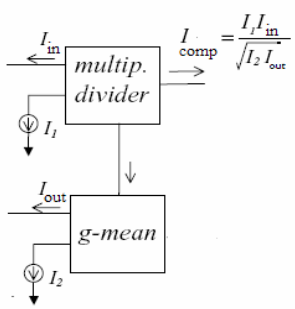
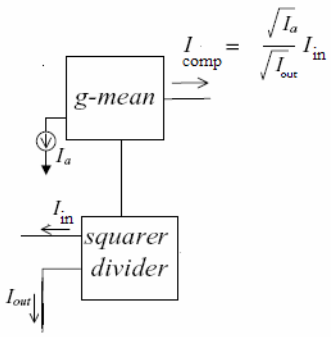


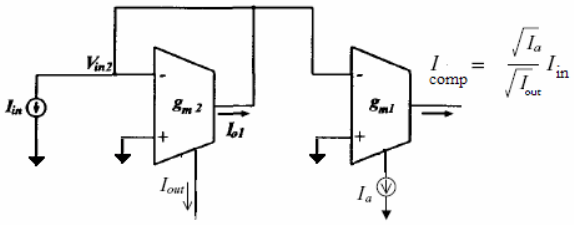
Fig. 2 SRD (a) Integrator (b) first order low pass filter



(a)



(b)



(c)

Fig.3 Nonlinear current compressor circuits

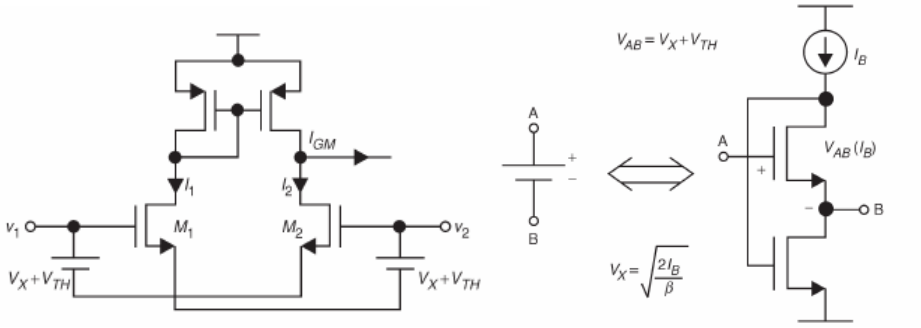


Fig. 4 Conventional class-AB linear transconductor (a) Basic principle (b) Practical implementation of floating voltage sources

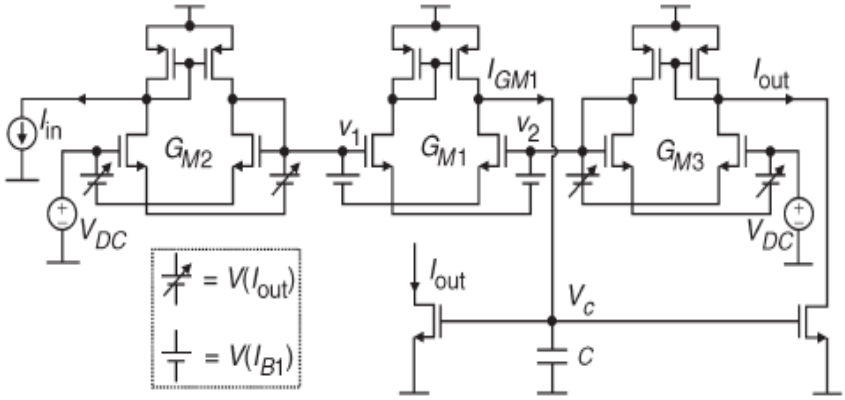


Figure 5 SRD filter circuit [22]

4. Proposed Class-AB SRD filter

Unfortunately, all of the previous SRD filter approaches use single MOSFET transistor to realize the expander *f()* which result in class A filter. Input signal currents can not be larger than input bias currents, It is well known that the power dissipation and the capacitor area is proportion to the dynamic range of class A filter. A general approach for the implementation of class-AB uses a pair of isolated Class-A filters driven by a current splitter circuit [23]. But, this technique increase the required area and the power consumption .

The circuit shown in Fig. 6 has been used before to realize a class AB buffer. It can be used here to realize the nonlinear expander. The operation of the circuit can be described as follows. If a current is withdrawn from the output terminal, the gate voltage of M1is lowered. By the action of the level shift transistors M3 and M4, the gate voltage of M2 is lowered as well. Thus, the current through M1 increases and the current through M2 decreases. Similarly, if the output terminal sinks current, the gate voltage of M1 and M2 increases; this decreases the current through M1 and increases the current through M2. Assuming all transistors are in the saturation region and M3and M4 are matched, it follows that

$$V_{GS1}+V_{GS3}+V_{GS1}=V_{GS5}+V_{GS6}+V_{GS4} \quad \textbf{(12)}$$

In standby mode no current is withdrawn from the output terminal and current I_{SB} is equal to the current following through

$$I_{O1}=I_{O2}=I_{SB} \quad \textbf{(13)}$$

The nonlinear f(v) and f′(v) will have one of this three states:

When $|I_{out}| < I_{standby}$,

$$I_{out} = f(v) = I_{o1} + I_{o2}$$
$$= \frac{\beta}{2}(v_{GSN} - V_t)^2 - \frac{\beta}{2}(v_{SGP} - V_t)^2 \quad \textbf{(14)}$$

$$f'(v) = \beta(v_{GSN} - V_t) + \beta(v_{GSP} + V_t)$$
$$= \beta(V_{GSN} + v_{gsn} - V_t) + \beta(V_{GSP} - v_{gsp} + V_t)$$
$$= \beta(v_{GSN} - V_t) + \beta(v_{GSP} + V_t)$$
$$= \beta(V_{GSN} + v_{AC} - V_t) + \beta(V_{GSP} - v_{AC} + V_t)$$
$$= \beta(V_{GSN} - V_t) + \beta(V_{GSP} + V_t)$$
$$= \sqrt{4\beta I_{SB}} = \sqrt{2\beta(I_1 + I_2)} \quad \textbf{(15)}$$

For $I_{out} > I_{standby}$, M1 is on and M2 is off

$$I_{out} = f(v) = I_{o1} = \frac{\beta}{2}(v_{SGP} - V_t)^2 \quad \textbf{(16)}$$

$$f'(v) = \beta(v_{GSP} + V_t) = \sqrt{2\beta I_{o1}} \quad \textbf{(17)}$$

For $-I_{out} < -I_{standby}$, M2 is on and M1 is off

$$I_{out} = f(v) = I_{o2} = \frac{\beta}{2}(v_{GSN} - V_t)^2 \quad \textbf{(18)}$$

$$f'(v) = \beta(v_{GSn} + V_t) = \sqrt{2\beta I_{o2}} \quad \textbf{(19)}$$

Thus f′(v) can be rewritten for the three cases as:

$$f'(v) = \sqrt{2\beta(I_{O1} + I_{O2})} \quad \textbf{(20)}$$

Fig. 7 shows the resulting circuit. Note that in Tran conductors GM2 their floating voltage sources are controlled by Iout to implement (24). Transconductor GM2 is acting as transresistors. The transconductor GM1 is acts as a V–I converter and the current I_B tunes the cutoff frequency of the filter, which is given by

$$\omega_{-3d} = \frac{\sqrt{2\beta I_B}}{C} \quad \textbf{(21)}$$

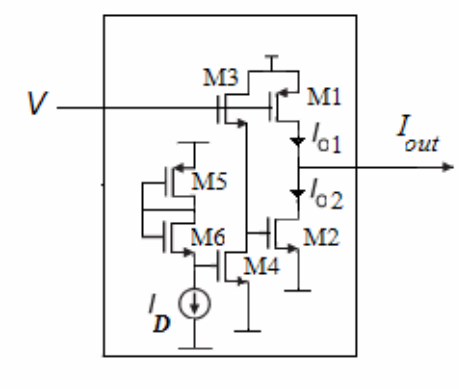


Fig. 6 Cass AB expander

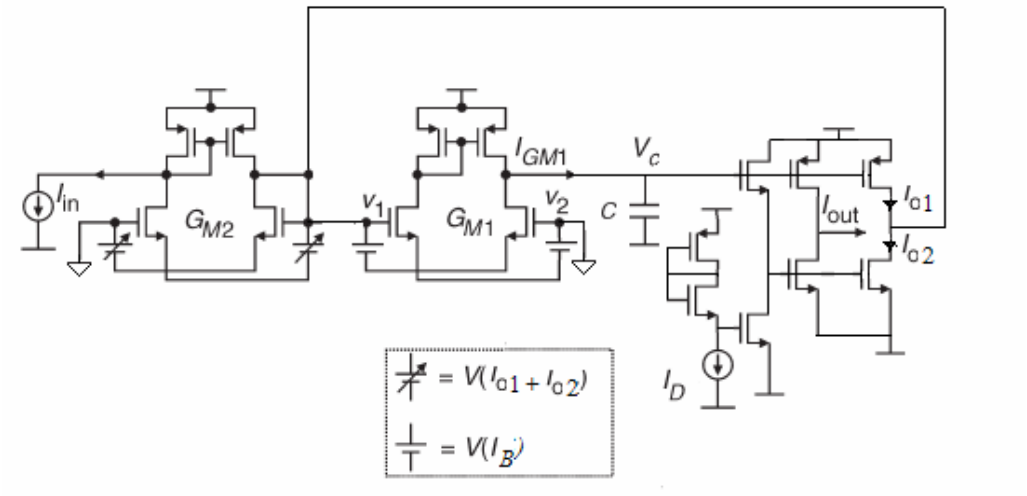


Figure 7 proposed class AB SRD filter circuit

5. Simulation Results

Simulations for proposed SRD domain low pass filter shown in Fig. 7. are carried out using 0.5um BSIM CMOS process parameters. The filter has been designed to operate from a ±1V supply voltage. Input current signal at 5kHz frequency with 50uA amplitude is applied to the filter, Fig. 8 (a) shows input and output current vs. time and Fig.8 (b) show the

compressed voltage at the capacitor. Notice that, the relation between input and output current is linear in respect of internally distorted signal. The power consumption was 167mW. Frequency response for different values of tuning current I_B shown in Fig. 9 illustrates the current tuneability of the filter. The dc gain error is small and the drift in cutoff frequency was 4% for a tuning current of 1uA.

6. Conclusions:

A novel approach to implement class AB SRD filters is presented. This approach leads to simplicity, low-voltage operation, reduced chip area and low power consumption. Simulation results from offered to validate the proposed technique. The approach is an interesting alternative to design filters with large input dynamic range and low voltage requirements. In future, this work will be extended to higher-order configurations.

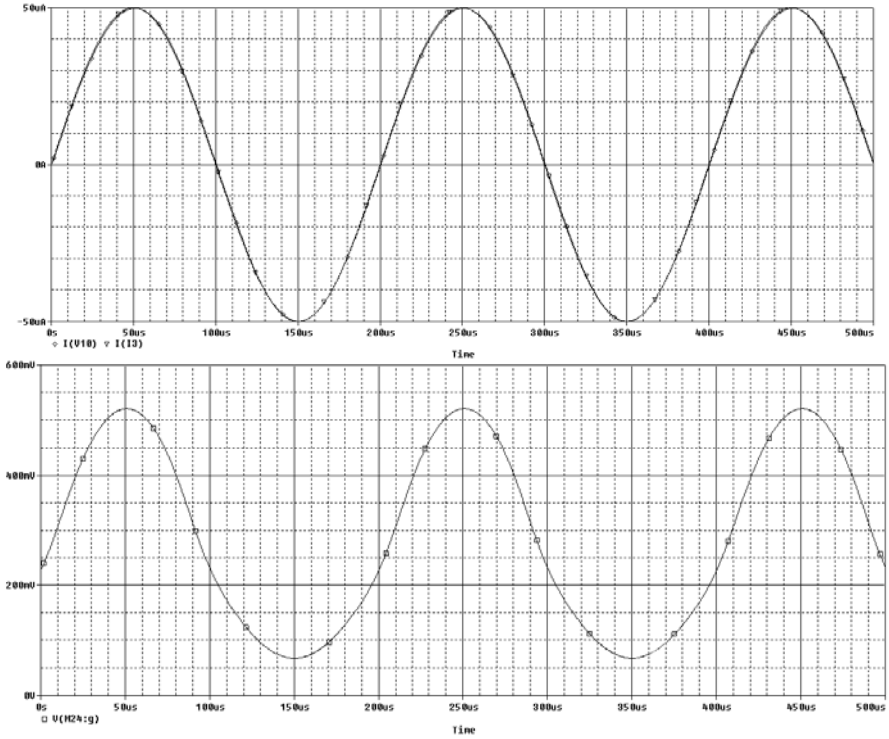


Fig. 8 Simulated time response results of class AB SRD first-order filter (a) input and output waveforms, (b) compressed internal voltage Vc

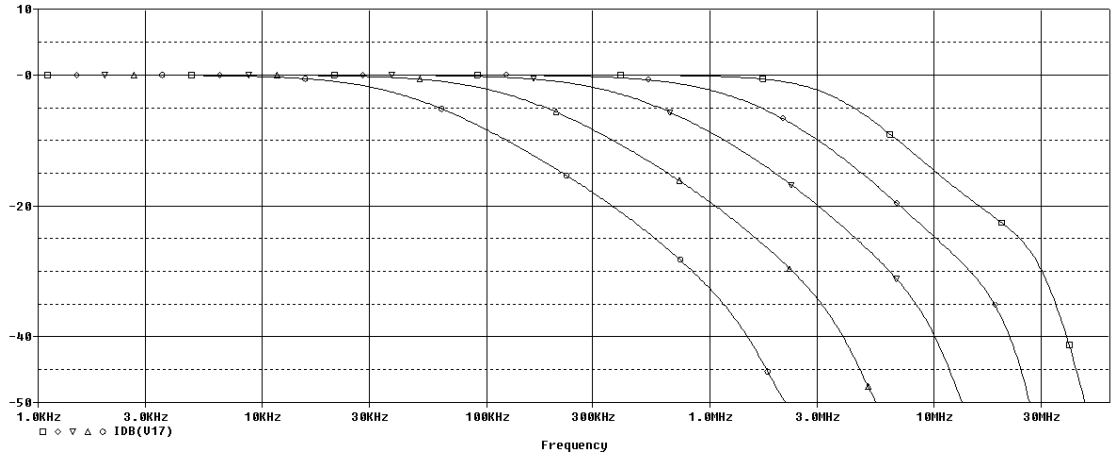


Fig. 9 Frequency responses of the proposed class AB low-pass filter with I_B equal to 100nA, 300nA, 1μA, 3μA and 10μA, respectively, and C equal to 10pF .

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