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# 1.5 V Rail-to-Rail Constant Gm CMOS Differential Amplifier

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*Abstract:* - In this paper is presented a novel constant transconductance CMOS differential amplifier. The circuit uses a modified CMOS inverter to process polarisation currents of the complementary differential amplifier in order to maintain constant transconductance over the entire common-mode input voltage range. Simulation shows error less than ±6.12 % for a single supply voltage of 1.5 V.

*Key-Words:* - low voltage, rail-to-rail differential amplifier, constant transconductance differential amplifier

## 1 Introduction

Over the last ten years supply voltages went down from 4.5-5V, the voltage levels widespread until the middle of the 90's, to 2.7-3V or 1.8-2V, with the tendency toward lower supply voltages of 0.9-1V in respond to the increasing use of battery or solar power, as was predicted in [1]. However, threshold voltages did not scale down accordingly, but remained rather high compared to the total voltage supply. This caused the need for new and different design techniques to achieve performances comparable to performances of circuits operated at higher voltages [2].

In the case of operational amplifiers, the lowering of supply voltage resulted in a reduced input common-mode range. The need for rail-to-rail operational amplifiers operated at low-voltages was evident. Rail-to-rail operational amplifiers allow input and output signals to vary from the negative to the positive supply rail, or, in case of unipolar supply, from the ground up to the supply voltage.

The design of a rail-to-rail input stage in CMOS technology is more complex than the design of a rail-to-rail output stage, which can be performed by employing class-A or class-AB output stages. The most common method of achieving rail-to-rail input stage is by using a complementary differential pair – an n-differential pair and a p-differential pair connected in parallel. The output currents from the two pairs are summed by means of current mirrors. The total transconductance of a complementary differential pair $g_{mt}$ equals the sum of the transconductances of individual differential pairs $g_{mn}$ and $g_{mp}$ [3]. When the input common mode voltage approaches positive supply rail, the n-differential pair is fully operated in saturation while the p-differential pair is off. When the input common mode approaches negative supply rail it is vice versa. In these cases the $g_{mt}$ equals the transconductance of the differential pair conducting. In the middle of the input common mode range both operational pairs conduct yielding the $g_{mt}$ equal to the sum of the respective pairs' transconductances. Operational amplifier architecture requires constant equivalent transconductance $g_{mt}=g_{mn}+g_{mp}=const.$ in order to achieve constant gain and constant unity gain frequency, which is very important when stability is concerned. Variations in transconductance of the input stage lead to variations in unity gain frequency of an amplifier, which in turn leads to suboptimal frequency compensation. Assuming channel lengths $L\geq 2\mu m$ [4], transconductance of a differential pair with MOSFETs in strong inversion is proportional to the square root of the drain current [3]. Thus, supposing the same gain factors $\beta_n$ and $\beta_p$ of the MOSFETs configuring the input differential pairs, to keep the equivalent trasconducatnce constant $g_{mt}=g_{mn}+g_{mp}=const.$ it is necessary to provide the constant sum of the square roots of the tail currents [2], [5]-[10].

In this paper is presented a novel design of the complementary differential pair with the circuit for processing its polarisation currents, based on a modified inverter, so that the sum of their square roots is constant. In addition to the low single supply voltage of 1.5 V and a small error of transconductance variation of ±6.12 %. Also, this design avoids a deviation from mathematical model, due to subthreshold operation of the respective MOSFETs,

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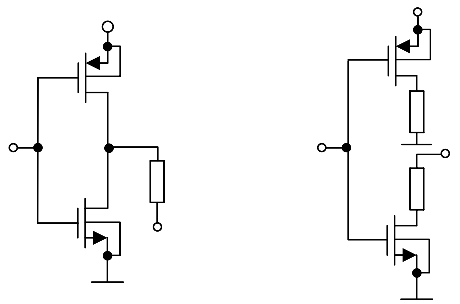

a) b)

Figure 1. *Modified CMOS inverter a), and its equivalent circuit b).*

as present in [5], [10].

## 2 Modified inverter

The circuit of the modified inverter is shown in Fig. 1. Unlike the classical CMOS inverter [10], this circuit has the resistor $R$ at its output. The gain factors $\beta_{p1}$ and $\beta_{n2}$ of the p-channel MOSFET $M_1$ and the n-channel MOSFET $M_2$, respectively, are made equal $\beta_{n2}=\beta_{p1}=\beta$ by proper design of the respective aspect ratios, that is to say, the ratio $(W/L)_p/(W/L)_n$ equals the ratio of the electron mobility to the hole mobility $\mu_n/\mu_p$. Simple square law Shockley model of a MOSFET [2] will be presumed in the following analysis. When the input voltage $V_{IN}$ is swept from the ground to the positive supply voltage $V_{DD}$, the modified inverter goes through seven operating regions which are as follows.

### 2.1 Region A

For the input voltage $V_{IN}$ in the range: $0<V_{IN}<V_{tn2}$, where $V_{tn2}$ is the threshold voltage of the n-channel MOSFET $M_2$, p-channel MOSFET $M_1$ is in the ohmic region, while n-channel $M_2$ is cut off. If the gain factor $\beta_{p1}$ of the MOSFET $M_1$ and the resistance $R$ are chosen so that $\beta_{p1}R>>1$ V$^{-1}$, the drain current $I_{D1}$ of the MOSFET $M_1$ can be approximated as

$$I_{D1}=\frac{V_{DD}}{2R}. \tag{1}$$

Since the drain current $I_{D2}$ of the MOSFET $M_2$ is $I_{D2}$=0 A, the sum of the square roots of the two currents in this operating region is

$$\sqrt{I_{D1}}+\sqrt{I_{D2}}=\sqrt{\frac{V_{DD}}{2R}}. \tag{2}$$

### 2.2 Region B

For the input voltage $V_{IN}$ in the range: $V_{tn2}<V_{IN}<V_{tn2}+4V_T$, where $V_T$ is the thermal voltage [3], p-channel MOSFET $M_1$ is in the ohmic region, whereas n-channel MOSFET $M_2$ is in the weak inversion. The drain current $I_{D2}$ of the MOSFET $M_2$ is much smaller than the drain current $I_{D1}$ of the MOSFET $M_1$, therefore, relation (2) is valid in this region, too.

### 2.3 Region C

For the input voltage $V_{IN}$ in the range: $V_{tn2}+4V_T<V_{IN}<(V_{tp1}+V_{np})/[1+\beta R(V_{DD}+V_{tp1}-V_{tn2})]$, where $V_{tp1}$ is the threshold voltage of the p-channel MOSFET $M_1$, and $V_{np}$ is given by:

$$V_{np}=\frac{1}{2}\beta R\left[\left(V_{DD}+V_{tp1}\right)^2-V_{tn2}^2\right]. \tag{3}$$

P-channel MOSFET $M_1$ is in the ohmic region, while n-channel MOSFET $M_2$ is in the saturation region. Assuming $\beta_{p1}R^2=\beta_{n2}R^2=\beta R^2>>1$ A$^{-1}$, one can obtain the value of the sum of the square roots of the currents in this region:

$$\sqrt{I_{D1}}+\sqrt{I_{D2}}=\sqrt{\frac{\beta}{2}}\left(V_{IN}-V_{tn2}\right)\left(1+\sqrt{1+k_p}\right), \tag{4}$$

where

$$k_p=\frac{2\left(V_{IN}-V_{tp1}-\frac{1}{2}V_{DD}\right)}{\beta R\left(V_{IN}-V_{tn2}\right)^2}. \tag{5}$$

### 2.4 Region D

For the input voltage $V_{IN}$ in the range: $(V_{tp1}+V_{np})/[1+\beta R(V_{DD}+V_{tp1}-V_{tn2})]<V_{IN}<(V_{tn2}+V_{np})/[1+\beta R(V_{DD}+V_{tp1}-V_{tn2})]$, both MOSFETs $M_1$ and $M_2$ are in the saturation. The value of the sum of the square roots of the MOSFETs $M_1$ and $M_2$ currents in this region is:

$$\sqrt{I_{D1}}+\sqrt{I_{D2}}=\sqrt{\frac{\beta}{2}}\left(V_{DD}-V_{tn2}+V_{tp1}\right). \tag{6}$$

The relation (6) gives the relationship between the supply voltage and threshold voltages of n- and p-channel MOSFETs: $V_{DD}>V_{tn2}-V_{tp1}$. The output voltage in this region can be found to be

$$V_{OUT}=-\beta RV_{IN}\left(V_{DD}+V_{tp1}-V_{tn2}\right)+V_{np}. \tag{7}$$

Using (3) and (7), the value of the input voltage $V_{IN}$ for which the drain currents $I_{D1}$ and $I_{D2}$ of the MOSFETs $M_1$ and $M_2$ are equal ($V_{OUT}$=0) is

$$V_{IN}=\frac{V_{DD}+V_{tp1}+V_{tn2}}{2}. \tag{8}$$

The quiescent current $I_0$ is now:

$$I_0 = I_{D1} = I_{D2} = \frac{1}{8}\beta\left(V_{DD} + V_{tp1} - V_{tn2}\right)^2 . \qquad (9)$$

From relations (6) and (9) follows:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = 2\sqrt{I_0} . \qquad (10)$$

### 2.5 Region E

For the input voltage $V_{IN}$ in the range: $(V_{tn2}+V_{np})/[1+\beta R(V_{DD}+V_{tp1}-V_{tn2})] < V_{IN} < V_{DD}+V_{tp1}-4V_T$, p-channel MOSFET $M_1$ is in the saturation region, while n-channel MOSFET $M_2$ is in the ohmic region. Similarly to the region *C*, the sum of square roots of the currents is given by:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{\frac{\beta}{2}}\left(V_{DD} + V_{tp1} - V_{IN}\right)\left(1 + \sqrt{1 + k_n}\right), \qquad (11)$$

where

$$k_n = \frac{2\left(V_{tn2} - V_{IN} + \frac{1}{2}V_{DD}\right)}{\beta R\left(V_{DD} + V_{tp1} - V_{IN}\right)^2} . \qquad (12)$$

### 2.6 Region F

For the input voltage $V_{IN}$ in the range: $V_{DD}+V_{tp1}-4V_T < V_{IN} < V_{DD}+V_{tp1}$, p-channel MOSFET $M_1$ is in the weak inversion, whereas n-channel MOSFET $M_2$ is in the ohmic region. The drain current $I_{D1}$ of the MOSFET $M_1$ is much smaller than the drain current $I_{D2}$ of the MOSFET $M_2$, therefore, relation (2) denoting the sum of the square roots of drain currents of MOSFETs in regions *A* and *G* is valid in this region, too.

### 2.7 Region G

For the input voltage $V_{IN}$ in the range: $V_{DD}+V_{tp1}<V_{IN}<V_{DD}$, p-channel MOSFET $M_1$ is cut off, whereas n-channel MOSFET $M_2$ is in the ohmic region. Similarly to region *A*, if the gain factor $\beta_{n2}$ of the MOSFET $M_2$ and the resistance *R* are chosen so that $\beta_{n2}R>>1$ $V^{-1}$, the drain current $I_{D2}$ of the MOSFET $M_2$ can be approximated as

$$I_{D2} = \frac{V_{DD}}{2R} . \qquad (13)$$

Since the drain current $I_{D1}$ of the MOSFET $M_1$ is $I_{D1}=0$ A the sum of square roots of the two currents in this operating region is given by (2).

### 2.7 Summary of the modified CMOS inverter operation

Examining the equations (2), (6), and (10) it is clear that if their right sides are equal, the sum of square roots of currents $I_1$ and $I_2$ is constant in the regions *A*, *B*, *D*, *F*, and *G*:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{\frac{V_{DD}}{2R}} = \sqrt{\frac{\beta}{2}}\left(V_{DD} - V_{tn2} + V_{tp1}\right) = 2\sqrt{I_0} \qquad (14)$$

The equation (14) states that the square root of the currents of p-channel MOSFET $M_1$ in the regions *A* and *B*, and n-channel MOSFET $M_2$ in the regions *F* and *G*, when they are in the ohmic region, must be twice the square root of the quiescent current. This condition precisely sets apart this modified CMOS inverter from inverter used as a class-AB output stage. Upon rearranging, the equation (14) gives the condition that must be satisfied:

$$\frac{V_{DD}}{\left(V_{DD} - V_{tn2} + V_{tp1}\right)^2} = \beta R . \qquad (15)$$

Furthermore, as indicated throughout descriptions of regions, it must be satisfied $\beta R>>1$ $V^{-1}$and $\beta_{p1}R^2=\beta_{n2}R^2=\beta R^2>>1$ $A^{-1}$. In order to obtain large enough $\beta R$ factor, it is desirable to have a single supply $V_{DD}$ slightly larger than the sum of absolute values of the threshold voltages $V_{DD}> V_{tn2}-V_{tp1}$.

As for the regions *C* and *E*, it is evident that they introduce a deviation from the level of the sum of square roots set by relation (14). However, by appropriate setting of the supply voltage $V_{DD}$ as well as $\beta R$ parameter, the deviations in the regions *C* and *E* can be made small enough.

## 3 Complete circuit schematics

As discussed in Introduction, in order to have constant transconductance $g_{mt}$=const. of the complementary differential pair, the following relation must be satisfied

$$\sqrt{I_{Bn}} + \sqrt{I_{Bp}} = const. , \qquad (16)$$

where $I_{Bn}$ and $I_{Bp}$ are the polarization currents of n-channel and p-channel differential pairs working in parallel, respectively. Comparing relations (14) and (16), it can be concluded that the constant transconductance $g_{mt}$=const. can be achieved by matching the polarization currents $I_{Bn}$ and $I_{Bp}$ of the differential pairs working in parallel to the drain currents $I_{D2}$ and $I_{D1}$ of the MOSFETs configuring modified CMOS inverter shown in Fig.1a), i.e. $I_{Bn}=I_{D2}$ and $I_{Bp}=I_{D1}$. In order to simplify mirroring of the currents $I_{D2}$ and $I_{D1}$ to the currents $I_{Bn}$ and $I_{Bp}$, respectively, the circuit shown in Fig. 1b) is used for

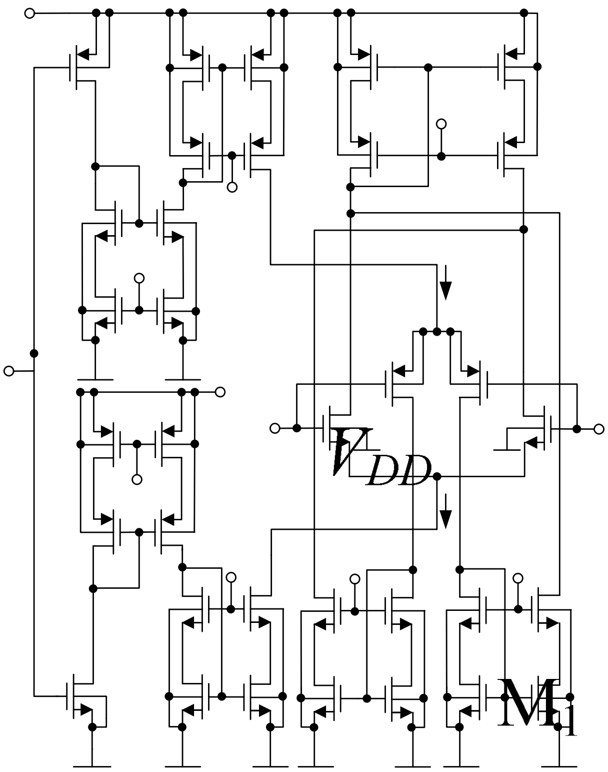

Fig. 2. *Complete circuit schematics of the modified inverter-based rail-to-rail CMOS differential amplifier with constant transconductance*

this purpose. The circuits shown in Figs. 1a) and 1b) are equivalent in terms of the MOSFETs' $M_1$ and $M_2$ currents. When the MOSFET M1 (M2) is in the ohmic region, MOSFET M2 (M1) is cut-off, the current through the M1 (M2) is given by (1); when MOSFET M1 (M2) is in the saturation region the current through it, neglecting the channel-modulation effect, is dependent on the gate-source voltage solely.

The complete schematic of the modified inverter-based rail-to-rail CMOS differential amplifier with constant transconductance is shown in Fig. 2. The input of the modified inverter is connected either to $V_{in}^+$ or to $V_{in}^-$. In active mode of the complementary differential amplifier (with a negative feedback), the equality $V_{in}^+=V_{in}^-=V_{CM}$ holds, where $V_{CM}$ is common mode voltage. When complementary differential amplifier works as a comparator (without negative feedback), the inequality $V_{in}^+ \neq V_{in}^-$ holds. In that case, depending on the value of the input voltage of the modified CMOS inverter $V_{in}^+$ ($V_{in}^-$), at least one of the differential amplifiers configuring complementary differential pair works in saturation mode, and comparator function is performed. The resistors 2R in Fig. 2b) are designed as the input resistance of the structure consisting of MOSFETs $M_5$,$M_6$,voltage reference $V_{B1}$, MOSFETs $M_3$ and $M_4$ for p-channel MOSFET $M_1$, and for n-channel MOSFET $M_2$ as the input resistance of the structure consisting of MOSFETs $M_{13}$,$M_{14}$,voltage reference $V_{B3}$, MOSFETs $M_{11}$ and $M_{12}$. When MOSFET $M_1$ is in the ohmic region the current through it is defined by the current source consisting of MOSFETs $M_5$,$M_6$ and voltage reference $V_{B1}$, the parameters of which must be chosen so that it is satisfied:

$$\frac{1}{2}\beta_{n5}\left(V_{B1}-V_{tn5}\right)=\frac{V_{DD}}{2R} \tag{17}$$

The MOSFETs M3 and M4 present active load. As the common- mode voltage increases, MOSFET $M_1$ enters saturation mode, while MOSFETs $M_5$ and $M_6$ go into ohmic region, thus presenting voltage controlled resistors by the voltage $V_{B1}$. In this way, these resistors present source resistors for the current mirror consisting of $M_3$ and $M_4$, and the whole structure acts as a source-degenerated current mirror.

The similar analysis holds for the n-channel MOSFET $M_2$, where the relation between parameters of MOSFETs M13, M14, and voltage reference $V_{B3}$ is given by:

$$\frac{1}{2}\beta_{n13}\left(V_{B3}-V_{tn13}\right)=\frac{V_{DD}}{2R} \tag{18}$$

The wide-swing current mirrors $M_7$-$M_{10}$ and $M_{15}$-$M_{18}$ are used for reversing directions of the currents $I_{Bn}=I_{D2}$ and $I_{Bp}=I_{D1}$. The N-channel and p-channel differential pairs working in parallel are made by the MOSFETs $M_{19}$-$M_{20}$ and $M_{21}$-$M_{22}$, respectively. Wide-swing current mirrors [11] $M_{23}$-$M_{26}$, $M_{27}$-$M_{30}$, and $M_{31}$-$M_{34}$ are used for summing of differential pairs' current.

## 4 Simulation results

The operation of the modified inverter-based rail-to-rail CMOS differential amplifier with constant transconductance shown in Fig. 2 has been simulated using PSPICE (Orcad Family Release 9.2) with a level 7 MOS transistor model for AMIS ABN n-well CMOS process with 1.6 µm feature size obtained by MOSIS. The typical value of the threshold voltages are $V_{tn}$=0.53 V and $V_{tp}$=-0.84 V. The resistor R= 20 kΩ for the supply voltage $V_{DD}$=1.5 V have been used. Simulation results of the sum of the square roots of the polarization currents for the modified inverter-based rail-to-rail CMOS differential amplifier with constant transconductance for the voltage supply of

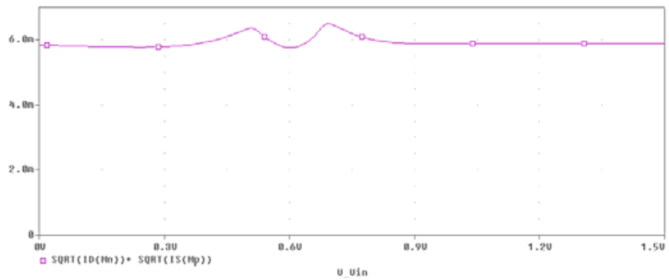


Fig. 3. *Simulation result of the sum of square roots of the polarization currents for the modified inverter-based rail-to-rail CMOS differential amplifier with constant transconductance* $V_{DD}=1.5$ *V.*

1.5 V is shown in Fig. 3. Relative error is determined related to the optimal line calculated as arithmetic mean of the maximum and the minimum of the sum of square roots of the polarization currents $I_{D16}$ and $I_{S8}$.

## 5 Conclusion

A new type of the processing circuit for constant sum of the square roots of polarization currents of the complementary differential pair is presented in the paper. This processing circuit is based on the modified CMOS inverter. Assuming known ratio of the electrons and holes mobility, a rail-to-rail differential amplifier is obtained, suitable for low supply voltage applications. Simulation results show transconductance variation error less than 6.12 % for the supply voltage of 1.5 V.

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