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Parametric fault model for RTD based Threshold Logic Gates

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Abstract: - One of major implementations of Linear Threshold Gate (LTG) is via resonant tunneling diodes (RTD). The functionality of this threshold logic gate greatly depends on the parameters of the RTD and parametric faults impact its functionality. A suitable fault model for Combinational Threshold Logic gates is presented. A methodology is also developed to generate test patterns that detect these parametric faults.

Key-Words: - Threshold logic, Linear threshold gate, Resonant Tunneling Diode, RTD parameters, MOBILE, parametric fault.

1 Introduction

Gates implemented with Threshold gates offer the capability of realizing complex Boolean functions using a smaller number of logic gates or fewer logic stages. A gate that implements threshold logic is called a Linear Threshold logic gate (LTG). It is a multiple terminal device that calculates a weighted sum of inputs [1] which is compared with a Threshold value to determine the logic value of the gate. It can be implemented using a Resistor-transistor element, a Magnetic core element or using a MOBILE element. The latter is the most popular implementation. A MOBILE [4, 5] is a pseudo-dynamic, clocked logic circuit consisting of a FET that is monolithically integrated with a resonant tunneling diode (RTD) [6, 9]. In contrast to dynamic circuits where the logic state is represented by the electrical charge on a capacitor, MOBILE circuits are in a static, self stabilizing state due to the inherent bistability of the devices. Consequently, the threshold logic gates are more robust against charge leakage and pre-charging is unnecessary [6, 4, 11].

Since the late 1950's threshold logic has been proposed as an alternate to conventional logic. Extensive research has been done in field of synthesis using threshold logic gates.

Recently defects in threshold logic gates associated primarily with interconnect issues and shorts across the RTDs have been modeled using the stuck-at fault model and also an ATPG has been proposed [2]. However, the functionality of the LTG greatly depends on parameters of its principle element, RTD. Hence parametric faults play a vital role in their functionality. A suitable fault model for Combinational Threshold Logic gates is needed and is proposed in this paper.

The proposed parametric fault model is based on the basic parameters of RTD, Area and Peak Current Density. These parameters of an RTD in a threshold logic gate determine the weight of a particular input. Its manufactured area may be different from the designed one. This leads to variation of weights of the threshold gate. Hence the function of Threshold Logic gate alters. This paper proposes a suitable fault model to detect such defects.

The remainder of this paper is organized as follows. Section 2 presents basic concepts that are required to understand the ideas presented in this paper. Section 3 presents the parametric fault model for threshold logic gates and also a methodology to test the faults. The experimental results are discussed in Section 4. The paper is concluded in Section 5.

2 Preliminaries

An *n*-input LTG is a logic gate where each weight w_i is associated with each input variable x_i and the output y of the gate is logic 1 only if weighted sum of its inputs exceeds or equals the value of a threshold, w_0 [1].

$$y = 1 \text{ when } \sum_{i=1}^{n} w_i x_i \geq w_0 \text{ and } 0 \quad \text{otherwise}$$

A typical threshold gate implemented using a MOBILE is shown in Figure 1. Figure 1 shows two serially connected RTDs and four RTD-HFET devices (the RTD and HFET are connected in

parallel) with two positive weighted inputs (x_1, x_2) and two negative weighted inputs (x_3, x_4) [10].

The concept of threshold function and thus the operation of a Threshold Gate can be explained with an example. Consider a LTG with ($w1$, $w2$, $w3$, $w4$; w_0) = (1, 0.5, -0.5, -2; 1.5). For input vector 0001, the output y of the gate will be 0 since

$$1*0 + 0.5*0 + -0.5*0 + -2*1 < 1.5$$

For input 1011 y will be 0, but with vector 1100 the output will be 1.

2.1 Weight of an RTD

The weight w_i of a certain RTD is realized as the ratio of the RTD peak current denoted by I_P^i over I_P^{min}, the peak current of an RTD designed with minimum dimensions [6] . Namely,

$$I_P^i = w_i . I_P^{min}$$

Since RTD is a vertical device, its current depends on its area. Hence the weight of an input RTD-HFET can be implemented by linearly scaling its area A_{RTD}^i with respect to the area of a minimum sized RTD, A_{RTD}^{min}. Hence the weight of any RTD-HFET gate of MOBILE is the ratio of its area A_{RTD} over a minimum area, A_{RTD}^{min}.

The threshold w_0 of the gate is determined by the areas of Load and Driver RTDs. It is the net difference in weights of the driver and load RTDs.

$$w_0 = w_D - w_L \qquad (1)$$

2.2 MOBILE Operation

Let V_{GS}^i be gate to source voltage of HFET of a certain RTD-HFET gate and if I_P^i be the peak current through that RTD. Then $I_P^i . V_{GS}^i$ will be the current from the RTD-HFET gate. This current $I_P^i . V_{GS}^i$ or $w_i I_p^{min} V_{GS}^i$ is added to the LOAD-DRIVER network if the gate to source voltage, V_{GSk} of an input x_i exceeds the threshold voltage of the HFET, i.e. if logic 1 is applied at x_i.

The internal weighted sum W of a LTG is then given by the total input current, ΔI at the output node. This current can be determined by Kirchhoff's current law. In Figure-1

$$\begin{aligned}\Delta I &= I1 + I2 - I3 - I4 \\ &= I_P^1 . V_{GS}^1 + I_P^2 . V_{GS}^2 - I_P^3 . V_{GS}^3 - I_P^4 . V_{GS}^4 \\ &= w_1 I_p^{min} . V_{GS}^1 + w_2 I_p^{min} . V_{GS}^2 - w_3 I_p^{min} . V_{GS}^3 - w_4 I_p^{min} . V_{GS}^4\end{aligned}$$

Hence the weight of a RTD determines the amount of current added to the network and the input x_i determines whether the current is added to network or not.

As the size of RTD shrinks, the peak current fluctuates due to the RTD area variation caused by the increasing impact of lithography and etching on lateral dimensions. It is been experimentally verified that the RTD I-V characteristics depends on the vertical device dimensions (epitaxial layer stack) with a high sensitivity in the sub-nanometer range and on lateral device dimensions (lithography, etching) in the nanometer range [13].

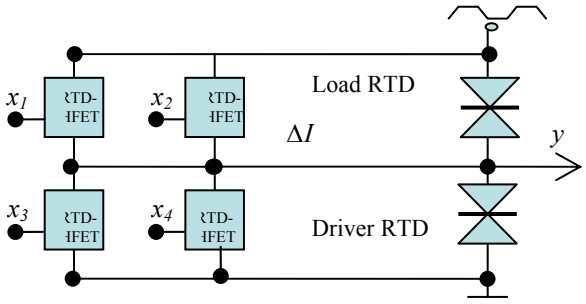

Figure 1. MOBILE implementation of threshold gate

2.3 Parameters of RTD

The basic parameters of a RTD are the Peak Voltage V_P, the Peak Current Density j_P and the side length L_{RTD}.

Since the RTD is a vertical device, the current is proportional to the device area and therefore

$$I_P = j_P A_{RTD}$$

Hence the logic output is greatly depends on the j_P and A_{RTD}. In the above example if w_1 is 0.5 instead of expected 1.0, the input vector results into $y = 0$ instead of the correct value of 1.

Many factors may result in fluctuations in values of these parameters. It is been experimentally proved that Doping Concentration N_D, well thickness d_B and barrier thickness d_W have great impact on the peak current density, j_P in case of a double-barrier resonant tunneling diode. A double-barrier resonant tunneling diode is composed of a low-bandgap quantum well with thickness d_W sandwiched between to wide bandgap electronic barriers with the thickness d_B. With the presence of impurities, there might be generation of unwanted electrons or holes in conduction band or valence band. This might disturb the balance of the band gap influencing the functionality of the RTD as whole. In case of a AlAs/In(Ga)As RTD, the sensitivity of peak-current density on the barrier thickness is found to be $\Delta j_P / \Delta N_D = 32 \times 10^{-18}$ KA cm [13].

Changes in well thickness and barrier thickness also have major impact on the peak current density. In both cases, increase in the value results in decrease of the peak current density, j_P. The sensitivity of j_P

with respect to d_W is found to be $\Delta j_P/\Delta d_W$ = -14 KA cm^{-2}/nm with d_B = 2.2nm and with respect to d_B is $\Delta j_P/\Delta d_B$ = -38 KAcm^{-2}/nm with d_W = 4.8nm [13].

The area of RTD also fluctuates because of variations in device parameters. A_{RTD} is directly dependent on L_{RTD}, the length of the side of vertical opening in the disc lattice through which electrons flows. Namely,

$$A_{RTD}{}^{min} = L^2{}_{RTD}$$

There may be discrepancies in the diode due to poor overgrowth during fabrication or temperature changes. During fabrication process there might be a accumulation of dust particles on these sides altering the side length L_{RTD} and hence the A_{RTD}. It is been shown that these dust particles have a major impact on the I-V characteristics of an RTD even when the side length is in range of 80μm [14]. The change in current density or variation in area of RTD has also an effect on the flow of current which is the weight of the RTD.

3 The Fault Model and rationale

Section-2 showed that a change in the parameters of an RTD may change drastically the functionality of the threshold gate. Because of such physical defects there will be variation in the values of the weights, w_i and the threshold, w_0. The threshold w_0 is also a weight value determined by two RTDs as in (1). Such variations can be greater than or lesser than the expected value. The defect at a weight may take different ranges of values. Parametric fault model helps in dividing these ranges of values into groups (sub-ranges) and helps to identify suitable pattern set for each group. This classification facilitates the manufacturer to efficiently test for faults at RTD for suspected range of values.

For each weight these range of faulty values may range greater than the expected value (***GE-fault***) and lesser than the expected value fault (***LE-fault)***.

Let us consider a 3-input NAND gate with (w_1, w_2, w_3; w_0) = (-1, -0.7, -0.3; -1.8). The input-output relationship of a trivial NAND gate is depicted in Table 1.

A CMOS gate consists of several transistors whereas a threshold gate implemented with MOBILE consists of several RTDs. An existing fault model for the CMOS gates of a circuit assumes that *only one transistor* can be faulty in the whole circuit (not only the CMOS gate) and either on or off. There are two faults per transistor but only one transistor is faulty in the whole circuit. Likewise, we propose a fault model where *only one RTD* in the whole circuit (not only in the whole circuit) can be faulty. Furthermore, for each RTD we have two types of faults, the GE fault and the LE fault.

Table 1. Implementation of NAND (-1, -0.7, -0.3; -1.8)

x_1	x_2	x_3	y	*Inequality*
0	0	0	1	$0 \geq w_0$
0	0	1	1	$w_3 \geq w_0$
0	1	0	1	$w_2 \geq w_0$
0	1	1	1	$w_2 + w_3 \geq w_0$
1	0	0	1	$w_1 \geq w_0$,
1	0	1	1	$w_1 + w_3 \geq w_0$
1	1	0	1	$w_1 + w_2 \geq w_0$,
1	1	1	0	$w_1 + w_2 + w_3 < w_0$

The threshold value w_0 is the difference of the Driver (w_D) and the Load (w_L) RTDs weights (see also Equation (1)). Divergence in these weights affects the w_0 value, but for fault modeling purposes these two RTDs must be treated together and a single GE-fault or LE-fault is assigned to the (Driver-Load) RTD pair of any MOBILE. This is true because in a typical MOBILE implementation only the w_D-w_L difference is specified. If w_D and w_L were given separately in the specifications of the gate implementation, then the two RTDs each would have treated separately. In our MOBILE 3-input NAND gate example we have 4 LE-faults and 4 GE-faults since the weights are w_i, $0 \leq i \leq 3$.

We use the notation LEw_i to denote a LE-fault associated with a defect at w_i. Similarly we use the term GEw_i to denote a GE-fault at w_i.

3.1 Parametric fault at single RTD

Let us consider the case of modeling of parametric fault at a single RTD without loss of generality**.** Consider the example of Table 1 and assume that the w_1 has a physical defect.

3.1.1 *GE-fault* at w_1

The application of pattern 111 would result in a faulty output if

$$w_1 \geq w_0 - (w_2 + w_3)$$
$$\geq -1.8 - (-0.7 + -0.3)$$
$$\Rightarrow w_1 \geq -0.8$$

If $w_1 > -0.8$ then the application of input pattern 111 will be able to activate the G*E* w_1. We also note that there is a region [-1..-0.8] where a GE-fault is inherently redundant from the MOBILE's specification. This is called the inherently redundant (IR) region for the GEw_1.

3.1.2 *LE-fault* at w_1

From the Table 1 it can be observed that the patterns that would activate the LEw_1 are 100, 101, 110, and 111.

Pattern 100 will be able activate the fault if $w_1 < w_0$. Since the output y will be 0. Hence the pattern 100 will be detect the fault at w_1 when $w_1 < -1.8$. Likewise, pattern 101 will detect the LEw_1 when $w_1 < -1.5$ and pattern 110 will detect LEw_1 when $w_1 < -1.1$. The tolerable region in this case is [-1.1..-1.0]. The above discussion is illustrated in Figure 2(a).

Pattern 110 detects any defect that is modeled as a LEw_1 fault. Pattern 101 detects subset of defects but may be useful if pattern 110 can not be observed at the input of this MOBILE or when its error can not propagate to any output of the circuit that the MOBILE belongs. If this the case then the IR region or the tolerable region of w_1 expands to [-1.5..-1].

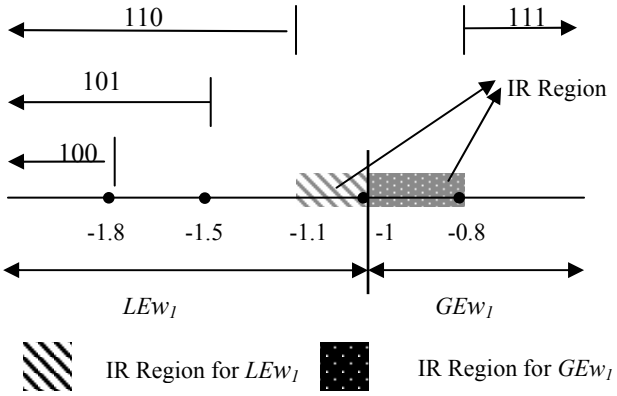

Figure 2 (a). Pattern detectability characteristics for LE-fault and GE-fault at w_1

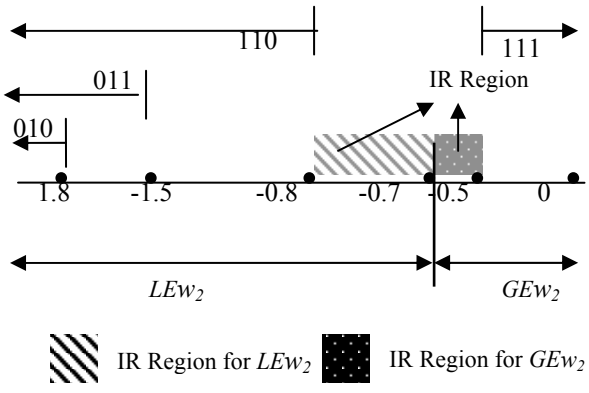

Figure 2 (b). Pattern detectability characteristics for LE-fault and GE-fault at w_2

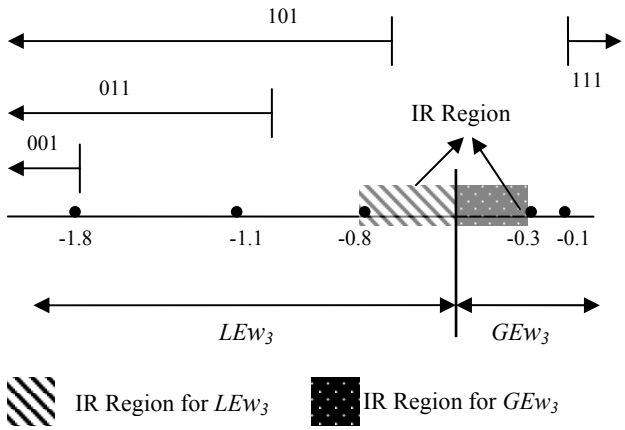

Figure2 (c). Pattern detectability characteristics for LE-fault and GE-fault at w_3

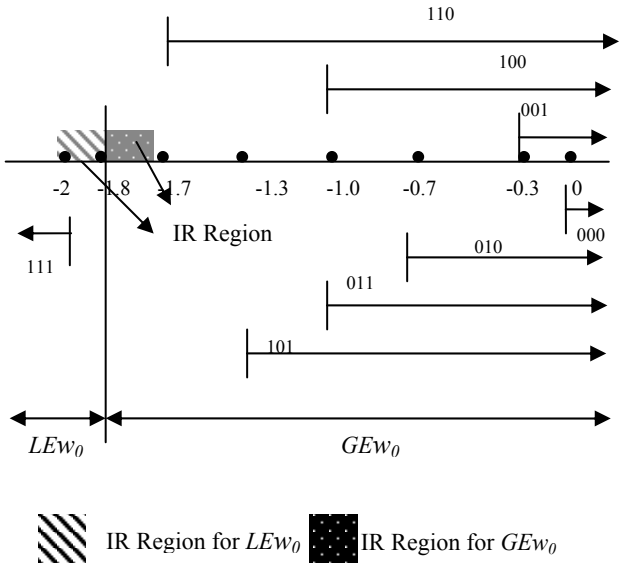

Figure 2 (d). Pattern detectability characteristics for LE-fault and GE-fault at w_0

If pattern 110 can be obtained and its error can be propagated to a circuit output then we say that the MOBILE is said to be ***1-Testable.*** If *LE* w_1 is not ***1-testable***, we still have chance of detecting the *LE* w_1 by considering the pattern 101. If pattern 101 is obtainable at input of the MOBILE and its effect can be propagated to the output of the circuit, then the fault is said to be ***2-Testable***. Finally, if pattern 101 is not activated or propagated then the pattern 100 will be used to detect ***3-Testability*** of LEw_1. If this pattern is also inapplicable then the fault is redundant.

In a way similar to Figure 2(a) for the case of LEw_1 and GEw_1, Figure 2(b) gives the pattern detectability characteristics for faults LEw_2 and GEw_2. Likewise, Figure 2(c) and Figure 2(d)

illustrate characteristics for w_3 and w_0, respectively. In Figure 2(d) notice that ***2-testability*** can be exercised with either 101 or 100. In general more than one pattern can detect the *i-testability* of a LEw_i or GEw_i for some RTD w_i.

We should target to detect faults of the MOBILE so that they are ***1-testable***. If a certain fault (LE or GE) at w_i is not ***1-testable***, then we must select a pattern for ***2-testability.*** In this case the RTD has an increased redundant region due to the circuit characteristics. Higher values of *i-testability* will only be considered if necessary.

If the parameter deviations of some w_i can not justify testing for a large value of i then we label the RTD as redundant. More specifically, if in the previous NAND example w_1 cannot be less than -1.8 then there is no need to test for ***3-testability***.

All possible faults of the NAND gate are tabulated in Table-2. Here only patterns which can detect the faults up to ***3-testabiltiy*** are considered for each case.

The parametric fault at input x_1 effects w_1 associated with x_1 whereas the stuck-at fault at x_1 effects whether x_1 is connected to network or not. Consider a NAND implemented with threshold logic with input and threshold (w_1, w_2, w_3; w_0) = (-1, -0.7, -0.3; -1.8). With stuck-at 0 fault at x_1 the functionality of changes (0, -0.7, -0.3; -1.8) and the pattern set for detecting this fault is {111}. And for SA0 fault at x_1 is {011}. Hence total pattern set to detect faults at x_1 is {111,011}. Consider parametric fault at x_1 resulting in w_1 associated with x_1 to be -1.3 instead of -1.0 : (-0.5, -0.7, -0.3; -1.8) resulting LE fault at x_1. The primary pattern needed to detect this parametric fault from previous discussion is 110. And also primary pattern to detect GE fault at x_1 when w_1=-0.5 is 111. Hence the pattern set needed to detect parametric fault at x_1 is {110, 111}. It is obvious that pattern set for stuck at fault is different from parametric fault.

4 Experimental Results

The test pattern generation methodology is implemented on ISCAS'85 benchmarks and all possible LE-faults and GE-faults are examined. An Automatic Test Pattern Generation (ATPG) tool has been implemented to determine which of these faults are *1-testable* or *2-testable*. All the faults which are higher order testable are considered to be redundant. The assumption is that such discrepancies in the parameters will not result due to manufacturing defects. In this section the term redundancy corresponds to untestability of an RTD fault due to topology of the circuit. It is different from the inherent redundancy of a weight at LTG level.

Each Boolean gate in the benchmarks is considered to be implemented with threshold logic having equal weights. For example a 3-input NAND is considered to be implemented with (-1.0, -1.0, -1.0; -2.5).The experimental results are listed in Table 3.

It can be observed from Table 3 that the total number of detected *1-testable* faults is greater than detected *2-testable*. This is probably the case because often there is more than one pattern for *1-testable* faults. This observation is true only for the equal weight implementation we examined.

5 Conclusion

The importance of parametric faults in the threshold logic gates is discussed. A suitable fault model is proposed for this kind of manufacturing defects. A test pattern generation methodology has been developed for the proposed fault model.

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Table 2. Faults of NAND (-1, -0.7, -0.3; -1.8)

Parametric Fault at	*LE Fault*			*GE Fault*		
	1-Testability	*2-Testability*	*3-Testability*	*1-Testability*	*2-Testability*	*3-Testabilty*
w_1	110	101	100	111	NA	NA
w_2	110	011	010	111	NA	NA
w_3	101	011	001	111	NA	NA
w_0	111	NA	NA	110	101	011/100

Table 3. List of tested faults on ISCAS'85 Benchmarks

ISCAS'85 Benchmarks	*LE Faults*		*GE Faults*		Redundant Faults
	1-Testable	*2-Testable*	*1-Testable*	*2-Testable*	
c17	12	0	12	0	0
c880	461	83	502	143	0
c1355	892	130	866	154	6
c1908	1026	177	1049	231	72
c3540	1895	271	2093	335	70
c5315	3370	368	3029	397	26
c7552	4297	763	4246	611	205