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Test Scheduling Optimization For Globally Asynchronous Locally Synchronous System-On-Chip Using Genetic Algorithm

P. SAKTHIVEL
Ramanujan Computing Centre
Anna University
Chennai – 600 025
INDIA

P. NARAYANASAMY
Department of Computer Science and Engineering
Anna University
Chennai – 600 025
INDIA

Abstract: - Test Methodologies for Globally Asynchronous Locally Synchronous (GALS) System On a Chip (SOC) are a subject of growing research interest since they appear to offer benefits in low power applications and promise greater design modularity. Pre-designed cores and reusable modules are popularly used in the design of large and complex Systems. As the size and complexity of System increase, the test effort, including test development effort, test data volume, and test application time, has also significantly increased. Available techniques for testing of core-based systems on a chip do not provide a systematic means for compact test solutions. A test solution for a complex system requires good optimization of Test Scheduling and Test Access Mechanism (TAM). In this paper, we provide a Test Scheduling Optimization for Globally Asynchronous Locally Synchronous System-On-Chip Using Genetic Algorithm that gives compact test scheduling.

Key-Words: - Systems on a Chip (SOC), Asynchronous Circuits, Core-Based Systems, Test Scheduling, Test Access Mechanism, Reusable Modules, Very Large Scale Integration (VLSI), Genetic Algorithm.

1 Introduction

Very Large Scale Integrated (VLSI) circuits designed using modern Computer Aided Design (CAD) tools are becoming faster and larger, incorporating millions of smaller transistors on a chip [1]. VLSI designs can be divided into two major classes: Synchronous and Asynchronous circuits. Synchronous circuits use global clock signals that are distributed throughout their sub-circuits to ensure correct timing and to synchronize their data processing mechanisms [14, 15]. Asynchronous circuits contain no global clocks. Their operation is controlled by locally generated signals [13]. Asynchronous circuits [11] have many potential advantages over their synchronous equivalents including lower latency, low power consumption, and lower electromagnetic interference [11].

However, their acceptance into industry has been slow, which may be due to a number of reasons. System On a Chip technology is the packaging of all the necessary electronic circuits and parts for a "System" on a single integrated circuit generally known as a "Microchip"[5]. System On a Chip technology is used in small, increasingly complex consumer electronic devices. Some such devices have more processing power and memory than a typical computer. The design of asynchronous circuits has been attracting more interest recently, as clock distribution on a large die becomes increasingly difficult. The ITRS road-map [11] predicts that, as a solution to the clock distribution problem, Globally Asynchronous Locally Synchronous system will become mainstream in the near future. In a GALS system, a number of synchronous islands of logic communicate asynchronously using a suitable interconnect. Unfortunately, the testability of asynchronous systems is considered one of their major drawbacks.

Testing SOC becomes an increasing challenge [5] as these devices become more complex. An SOC design is typically built block by block. Efficient testing is also best done by block by block. Recently, pre-designed cores are also used in the SOCs [6]. Testing individual circuits, individual blocks and individual cores have established technologies. But, available techniques for testing of core-based systems on a chip do not provide a systematic means for synthesizing low overhead test architectures and compact test solutions [7]. Embedded cores such as processors, custom application specific integrated circuits, and memories are being used increasingly to provide SOC solutions to complex integrated circuit design problems [8]. The advance in design methodologies

and semiconductor process technologies has led to the development of systems with excessive functionality implemented on a single chip [7].

In a core based design approach, a set of cores, that is predefined and pre-verified design modules, is integrated into a system using user defined logic and interconnections. In this way, complex systems can be efficiently developed [9]. However, the complexity in the system leads to high-test data volumes and design and optimization of test solution are must for any test. Therefore consider the following independent problems [7]:

- How to design an infrastructure for the transportation of test data in the system, a test access mechanism.
- How to design a test schedule to minimize test time, considering test conflicts and power constraints.

The testable units in an SOC design are the cores, the User Defined Logic (UDL) and the interconnections. The cores are usually delivered with predefined test methods and test sets, while the test sets for UDL and interconnections are to be generated prior to test scheduling and TAM Design. The workflow when developing an SOC test solution can mainly be divided into two consecutive parts: an early design space exploration followed by an extensive optimization for the final solution.

In this paper, we propose a new technique using Genetic Algorithm for optimizing the test scheduling for Globally Asynchronous Locally Synchronous System On Chip with the objective to minimize the test application time. The aim with our approach is to reduce the gap between the design space exploration and the extensive optimization that is to produce a high quality solution in respect to test time and test access mechanism at a relatively low computational cost.

The rest of the paper is organized as follows. Various issues related to SOC testing and Test Scheduling Techniques are discussed in Section 2. Genetic Algorithm based framework for Test scheduling is presented in Section 3. In section 4, the experimental results for ITC-02 Benchmark SOC circuit p34392 are presented. Finally, section 5 gives conclusion to the paper.

2 SOC Testing and Test Scheduling Techniques

The test-application time when testing a system can be minimized by scheduling the execution of the test sets as concurrently as possible [1]. The basic idea in test scheduling is to determine when each test set should be executed, and the main objective is to minimize the test application time.

The scheduling techniques can be classified by the following scheme [2]:

- No partitioned testing
- Partitioned testing with run to completion, and
- Partitioned testing.

2.1 Testing System On a Chip

Integration of a complex system, that until recently consisted of multiple Integrated Circuits, onto a single Integrated Circuits, is known as System On a Chip [3]. The shrinking of silicon technology leads to increase in number of transistors on a chip. This increases the number of faults and test vectors that in turn leads to the serious increase in test time. Test time reduction is one of the research challenge [4] in the SOC design paradigm.

The most important issues in the System On a Chip Testing are as follows [5]:

- Controlling the whole process of SOC Testing.
- Testing the User Defined Logic and Interconnections.
- Testing cores with different functionalities coming from different vendors.
- Accessing cores from the system's primary inputs and primary outputs.

2.2 Test Access Mechanism

The test access mechanism (TAM) takes care of chip test pattern transport. It can be used to transport test stimuli from the test pattern source to the core under test and to transport test responses from the core under test to the test pattern sink. The TAM is by definition implemented on chip [6].

The following are the four problems structured in order of increasing complexity [2].

- P_W: Design a wrapper for a given core, such that the core testing time is minimized, and the TAM width required for the core is minimized.
- P_{AW}: Determine (i) an assignment of cores to TAMs of given widths, and (ii) a wrapper design for each core such that SOC testing time is minimized.
- P_{PAW}: Determine (i) a partition of the total TAM width among the given number of

TAMs, (ii) an assignment of cores to TAMs of given widths, and (iii) a wrapper design for each core such that SOC testing time is minimized.

- P_{NPAW}: Detremine (i) the number of TAMs for the SOC, (ii) a partition of the total TAM width among the given number of TAMS, (iii) an assignment of cores to TAMs of given widths, and (iv) a wrapper design for each core such that SOC testing time is minimized.

The above problems are all NP – Hard problems. Therefore, efficient heuristics and other techniques are needed for large problem instances [7]. In this work, we are presenting Genetic Algorithm based approach [8] to effectively solve the problems namely P_{AW} and P_{PAW}.

3 Genetic Algorithm Based Framework for Test Scheduling

In this section the Genetic Algorithm (GA) that is used for generating test sequences for System On a Chip is described [1,2,3,4,9]. First, the basic idea of the method is given. Then we present the representation of test conditions and the objective function and provide some insight into the parameter settings of the Genetic Algorithm [10]. Genetic algorithms can be used to solve effectively the search and optimization problems. GAs consists of population of solutions called chromosomes. Here the chromosomes are an encoding of the solution to a given problem. The algorithm proceeds in steps called generations. During each generation, a new population of individuals is created from the old, by applying genetic operators. Given old generation, new generation is built from it, according to the following operation given in section 3.1, 3.2 and 3.3 [11].

3.1 Selection

This operator selects the individuals from the old generation. The individual with a better performance possess higher chance of getting selected.

3.2 Crossover

This operator generates two new chromosomes from the couple of selected chromosomes. A random point on the chromosome also known as cross-site is selected. Portions of individuals in a couple are exchanged between themselves to form new chromosomes as follows [12]:

for I = 1 to number of entries in the chromosome

Child (I) = Parent1 (I) if I <= cross-site
= Parent2 (I) if I > cross-site

Child2 (I) = Parent2 (I) if I <= cross-site
= Parent1 (I) if I > cross-site

3.3 Mutation

This operator chooses a random chromosome and modifies it to form the new chromosome.

3.4 Overview of our Method

The different steps of our method is given as follows [1]:

1. Generate the initial population of chromosomes, randomly.
2. Sort the initial population in ascending order of the cost.
3. While there is no improvement in cost function
   Do
   Select first 20% chromosome as best class.
   Generate 40% chromosomes using crossover operator.
   Generate 40% chromosomes using mutation operator
   Sort this generation in ascending order of the cost.
4. End of genetic algorithm.

4 Experimental Results

Our experiments were conducted for the ITC-02 SOC benchmark circuit p34392 [3]. The p34392 SOC benchmark circuit consists of 20 modules, of which 15 are combinational and 5 are sequential circuits. It has 3 levels, 2057 input and outputs, 20948 scan flip-flops and 66349 test patterns.

The Table - 1 gives the result for SOC p34392 with two partitions. W is the width of TAM. w1 and w2 are size of the partition 1 and partition 2. The processor time and test time given under the Heuristics are taken from [2]. The processor time and test time given under Genetic Algorithm is the combination of the results of our

experiment and [1]. For two partitions of total TAM width, the maximum processor time taken is 1.34 seconds and minimum processor time taken is 0.82 seconds.

Table – 1: Results for SOC p34392 with two partitions

W	w1 + w2	(Processor Time(*Seconds*))/ Test Time(*Cycles*)	
		Heuristics	Genetic Algorithm
16	8 + 8	(1)/ 1080940	(1.34)/ 1080900
24	15 + 9	(1)/ 928782	(1.25)/ 928562
32	21 + 11	(1)/ 750490	(1.10)/ 749850
40	24 + 16	(1)/ 721566	(0.97)/ 721450
48	31 + 17	(1)/ 709262	(0.85)/ 708550
56	38 + 18	(1)/ 704659	(0.82)/ 704650
64	18 + 46	(1)/ 700939	(0.88)/ 700800

5 Conclusion

The experimental results are given for only one Benchmark circuit SOC p34392 with two partitions. The result gives good approximation compare to Heuristics within a few generations with acceptable processor times. This establishes the suitability of this problem to be solved by Genetic Algorithm. We can apply this technique to all the other SOCs given in [3] having more number of cores with many scan chains and even more number of TAM widths.

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About the Authors

P. Sakthivel received the Bachelor of Engineering Degree in Computer Science and Engineering from Sathyabama Engineering College, University of Madras, Chennai, India in 1992 and Master of Computer Science and Engineering Degree from Jadavpur University, Kolkata, India in 1994. He is currently Lecturer in Ramanujan Computing Centre, Anna University, Chennai, India and working towards the PhD Degree in the Department of Computer Science and Engineering, Anna University, Chennai, India. His research interests include VLSI Design and Testing and Computer Aided Design of VLSI Circuits.

P. Narayanasamy received the Bachelor of Engineering Degree in Electrical and Electronics Engineering from Coimbatore Institute of Technology, University of Madras, Coimbatore, India in 1980, Master of Engineering Degree in Electrical and Electronics Engineering from Anna University, Chennai, India in 1982 and PhD Degree in the area of Computer Applications in Electrical Engineering from the Faculty of Electrical Engineering, Anna University, India in 1989. He is currently Professor and Head of the Department of Computer Science and Engineering, Anna University, Chennai, India. His research interests include VLSI Design and Testing, Computer Communication Networks, Wireless and Mobile Computing. He has guided many students for PhD and MS Programmes. He has published many technical and research papers in the National and International Conferences and Journals. He has also served as the Secretary for the Tamilnadu Engineering Admissions during the year 2002 – 2005.

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