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A Wideband Low-Power Cascade ∑Δ Modulator Based on Considerations of the Integrator Settling Behavior

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Abstract: - This paper presents a study of the effect of settling error due to finite gain-bandwidth product (GBW) and slew-rate (SR) of opamps in SC ΣΔ A/D modulators. Based on the theoretical point of view, a new architecture for cascade multibit ΣΔ A/D modulators is proposed to achieve better performances at low oversampling ratio. The performance improvement is analyzed and compared with traditional cascade architectures. Simulation results show that the proposed Sigma-Delta modulator relaxes the circuit requirement on the GBW of opamps up to twice the sampling frequency. At the same time, the requirement on slew rate is significantly low, so that it can be automatically satisfied for an adequate settle during its settling phase. Therefore, the proposed architecture is suitable for wideband and low-power applications. Moreover, it is shown that the proposed architecture is also immune to other non-idealities, such as finite DC-gain, capacitor mismatching and non-linear DC-gain.

Key-Words: - Analog integrated circuits, high-speed high-resolution analog–to-digital converters, and sigma–delta modulator

1 Introduction

High-speed high-resolution analog-to-digital converters (ADCs) are one of the key devices in measurement equipment and communication systems. Therefore, many different ADCs based on various kinds of ADC topologies have been developed. Among them, Sigma-Delta ADCs have been frequently applied to realize high resolution under the consideration of low cost and power consumption.

For high-speed applications, integrator defective settling is the main bottleneck in the present wideband SC Sigma-Delta modulator designs. Many low oversampling high-resolution modulators use MASH structures [2]–[4], where 1-bit quantizer is commonly used in the first stage, to avoid the performance degradation due to the non-linearity of DAC. However, these structures need a high opamp GBW to relieve the impact on the settling error. With the development of the efficient dynamic element matching (DEM) techniques [6]-[8], multibit quantization has been recently used in SC single-loop Sigma-Delta modulators to realize high-resolution at low OSR. Although, the required opamp GBW can be relaxed by using multibit quantizers, it is practically difficult to be obtained, since high-order single-loop modulators are formed by cascading multiple integrators in the forward path, and therefore, the dc gain of the forward path is very high. As a result, the signal, which is sensed by quantizer, is almost independent of the input signal. Therefore the input levels of integrators are still high [8]. Another problem associated with settling error of all of the aforementioned structures is the appearance of harmonic distortion due to the gain dependence of the integrator on its input, when opamp dynamic operation is in partial slewing.

In this paper, the effect of settling error thermal noise on the performance of SC Sigma-Delta modulators will be discussed, and an efficient interdependency between finite *GBW* and *SR* of opamps will be described for estimating the minimum demand on the GBW of opamps. Following it, a new cascade Sigma-Delta modulator architecture is presented, which combines the merits of cascaded Sigma-Delta Modulator structure, low distortion structure [9], and multibit quantization. This ADC development relaxes the GBW of opamps as low as twice the sampling frequency f_S, much lower than that in other Sigma-Delta modulator implementations [3]-[5]. Another advantage of the proposed modulator is that it is insensitive to circuit non-idealities. Section 2 contains a general analysis of the settling behavior in the SC integrators. Section 3 describes the newly-proposed architecture. Section 4 presents the simulation results for the validation of performance improvements. The conclusion is followed in Sections 5.

2 Analysis of Settling Behavior

2.1 SC integrator simplified model

The settling error is caused by *GBW* and *SR* of amplifiers in SC Sigma-Delta modulators [1] [2]. The simplified model of a SC integrator is shown in Fig.1, which consists of two pairs of input samplers, a sampling capacitor C_S, an integration capacitor C_I and a single-pole amplifier. The amplifier is modeled by the transconductance g_m, with biasing current I_{BIAS} , C_{GS} and C_L standing for a parasitic capacitor associated with the summation node of the amplifier input and a capacitive load, which includes parasitics at the amplifier's output node and the parasitic associated with the bottom plate of the integration capacitor C_I, respectively.

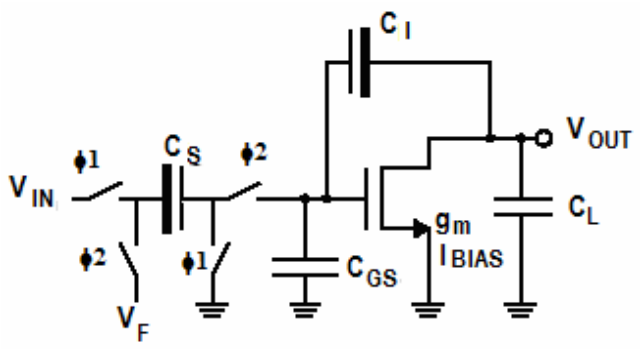

Fig. 1 Simplified CMOS integrator schematic

In this case, the equivalent closed-loop capacitance at the integrator output depends on the equivalent open-loop capacitance ($C_{cl,ol}$) and the dc feedback factor (*f*) during the integration phase, and it is given by [11]:

$$C_{eq,cl} = \frac{C_{eq,ol}}{f} = C_S + C_{GS} + \frac{(C_S + C_{GS} + C_I)C_L}{C_I} \tag{1}$$

Therefore, the close-loop time constant and slew rate are obtained, respectively [2]:

$$\tau = \frac{C_{eq,cl}}{g_m} \tag{2}$$

$$SR = \frac{I_{BIAS}}{C_{eq,cl}} \tag{3}$$

Furthermore, the relationship between the slew rate and the time constant has been derived using the simple square-law model of the MOS transistors [2]:

$$SR * \tau = \frac{I_{BIAS}}{g_m} = \frac{V_{GS} - V_{th}}{2} = \frac{V_{eff}}{2} \tag{4}$$

Where V_{GS} is the quiescent gate-to-source voltage of the input transistor, V_{th} is its threshold voltage, and V_{eff} is the overdrive voltage. Reforming (4) by introducing gain-bandwidth product GBW, a more design-oriented constant is obtained:

$$\frac{SR}{GBW} = \pi V_{eff} \tag{5}$$

It indicates that both design parameters SR and GBW are directly proportional to I_{BIAS}, and therefore, the ratio is quite constant in opamps, which depends directly on the overdrive voltage.

2.2 Settling Behavior of the SC integrator

With respect to the settling error, two separate cases have been considered [5]:

1. In the case of

$$SR \geq \left| \frac{C_S}{C_I} \frac{v_s}{\tau} \right| \tag{7}$$

there is no slew-rate limitation, and the integrator output will be linearly settled.

2. In the case of

$$SR < \left| \frac{C_S}{C_I} \frac{v_s}{\tau} \right| \tag{8}$$

and

$$t_0 = \frac{C_S}{C_I} \frac{|v_s|}{SR} - \tau < \frac{1}{2 f_s} \tag{9}$$

the op-amp is first in slewing within t_0, and therefore, the integrator output shows a partially SR limited *nonlinear settling*. Imposing (4) in (7) and reforming, we get the linearly-settling condition:

$$V_{eff} \geq 2 \frac{C_S}{C_I} |v_s| \tag{10}$$

Similarly, imposing (4) in (8) and (9), the partially SR limited nonlinear settling condition with $GB_{norm}=GBW/f_s$ is:

$$2 \frac{C_S}{C_I} \frac{|v_s|}{1 + \pi GB_{norm}} < V_{eff} < 2 \frac{C_S}{C_I} |v_S| \tag{11}$$

The linear settling error can be approximated as:

$$\varepsilon_{st} \cong \exp\left(-\frac{T_S}{2\tau} \right) = \exp\left(-\pi GB_{norm} \right) \tag{12}$$

whereas the nonlinear settling error can be approximately evaluated as:

$$\begin{aligned} \varepsilon_{st} &\cong \frac{SR * \tau}{\frac{C_S}{C_I} v_S} * \exp\left(-T_S / 2\tau - 1 + \frac{C_S}{C_I} \frac{|v_s|}{SR\tau} \right) \\ &\cong \frac{V_{eff}}{2 \frac{C_S}{C_I} v_s} * \exp\left(-\frac{\pi GBW}{f_S} - 1 + 2 \frac{C_S}{C_I} \frac{|v_s|}{V_{eff}} \right) \\ &= \frac{V_{eff}}{2 v_{norm}} * \exp\left(-\pi GB_{norm} - 1 + 2 \frac{|v_{notm}|}{V_{eff}} \right) \end{aligned} \tag{13}$$

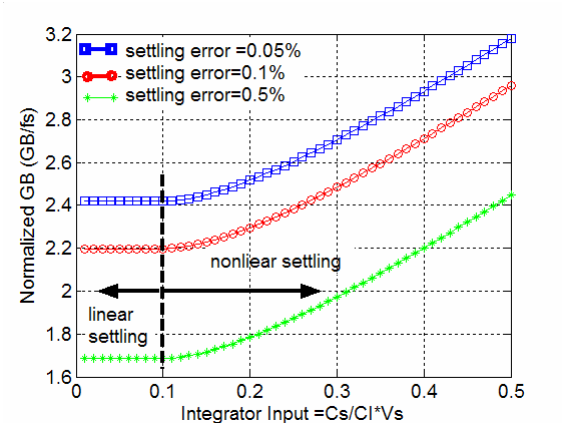

Fig. 2 The relationship between the demanded normalized GB and the relative integrator input level for a given settling error

Fig. 2 illustrates the corresponding relationship between the normalized GB and the integrator's relative input level. The output response of the integrator is assumed to be settled to a given error of 0.05%, 0.1% and 0.5%, respectively, and V_{eff}=200mV. It is shown that the low input level of the integrator is the key to reduce the required normalized gain-bandwidth GB. Note that most of the other existing Sigma-Delta modulators have a great occurrence that the input levels of the integrators are relatively large, so that eq. (10) is not satisfied. Therefore, they operate mostly in the non-linear settling region. Consequently, a relatively large opamp gain-bandwidth is required, and harmonics is produced. Additionally, the opamp normalized gain-bandwidth GB can also be reduced by using a certain topology, which is insensitive to the settling error.

3 Proposed ΣΔ Modulator

With respect to saving power and maximizing the conversion rate, the most essential issue in the design of ADC's is to reduce the normalized GB as much as possible, whereas the resolution of the converter is not deteriorated. It means, when the signal bandwidth is fixed, f_s is also fixed, and the reduced requirement on the opamp GBW results in a smaller I_{BIAS}, and thus smaller power consumption; on the other hand, when the opamp GBW is fixed due to technology limitation, a higher f_s can be used, resulting in extended signal bandwidth.

Based on the analysis on the settling behavior of SC integrators, a new alternative approach to realize wideband and wide-dynamic-range ADC is proposed, in which the low-distortion multi-bit Sigma-Delta modulator concept [9] is introduced into cascaded sigma delta modulators. The proposed generic architecture is shown in Fig.3, where g_{N1}, g_{N2}, g_{N3} are the interstage scaling factors in the *n*th stage. With the consideration of physically achievable output swings, in combination of behavior simulation and statistical optimization, we obtain;

g_{i1}=1 g_{i2}=1 g_{i1}=0.5 i=2….N-1
g_{N1}=1 g_{N2}=0.5 g_{N3}=1

H(z) in the blocks denotes the integration function:

$$H(z)=\frac{z^{-1}}{1-z^{-1}} \qquad (14)$$

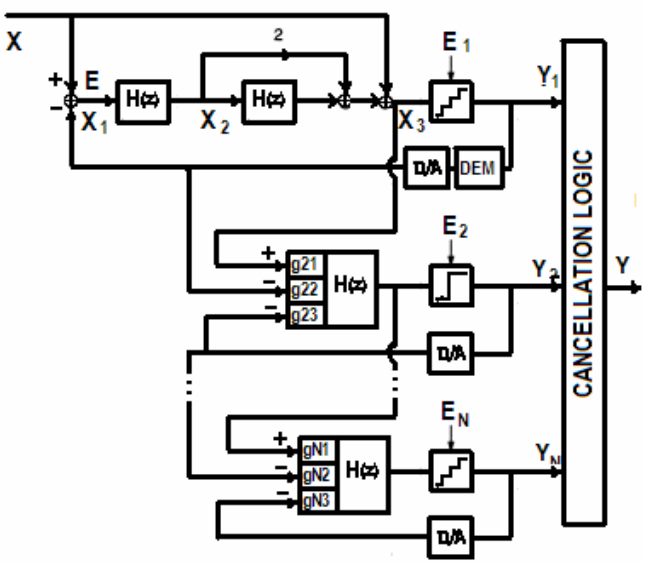

Fig. 3. The proposed N-stage cascade Sigma-Delta modulator

Ideally, the quantization error in all stages except the last one of the cascade structure can be completely cancelled in the digital domain. Therefore, the output signal can be expressed as the combination of the delayed input signal and the $(N+1)^{th}$-order noise-shaped quantization noise (N is the number of cascaded stages), that is:

$$Y = X * z^{-(N-1)} + E_N (1 - z^{-1})^{N+1} \qquad (15)$$

where E_N indicates the last-stage quantization error. Note that the proposed interstage scaling factors do not degrade the dynamic range as other cascade structures.

The key advantage over other high-order cascades is that the individual input level of the integrators is considerably lower, even with high feedforward gain C_S/C_I=1 in the two integrators of first stage, as only low-level quantization noise *E* is introduced in the integrator loops. To illustrate this, Fig. 4 shows the histogram of the integrator inputs (X_1 and X_2) and quantizer input (X_3) for an input signal with amplitude of -3 *dBFS*.

Fig.5 presents the performance improvement with respect to the settling error by comparing the SNDR, signal-to-(noise+distortion) ratio, vs. the normalized GB

and OSR of a 2-1-1-1(4b) cascade [4] with the one described in this paper with N=4 and 4-bit quantizers in the first and third stage, respectively. The results of behavioral simulations are obtained by assuming that the slew rate of opamps always follows the relationship of (5), where V_{eff}=200 mV. It is shown that the needed gain-bandwidth-product in Hz of the proposed one is only 2 fs, whereas that of the traditional 2-1-1-1 cascade is over 4 fs [3] [5], in order to avoid the impact of the settling error. Note that there is a systematic loss of 1 bit, or 6 dB SNDR in the traditional cascade architectures due to the smaller amplifying factor in comparison with an ideal $(N+1)^{th}$-order Sigma-Delta modulator. This loss is avoided in the proposed architecture, since the proposed integrator gains are optimized to obtain the ideal $(N+1)^{th}$-order noise shaping function.

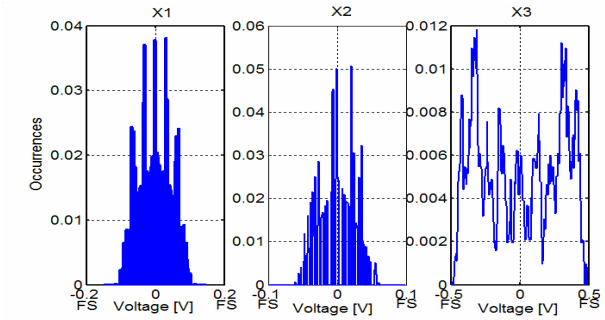

Fig. 4 First stage histogram of the integrator inputs and quantizer input relative to the FS voltage.

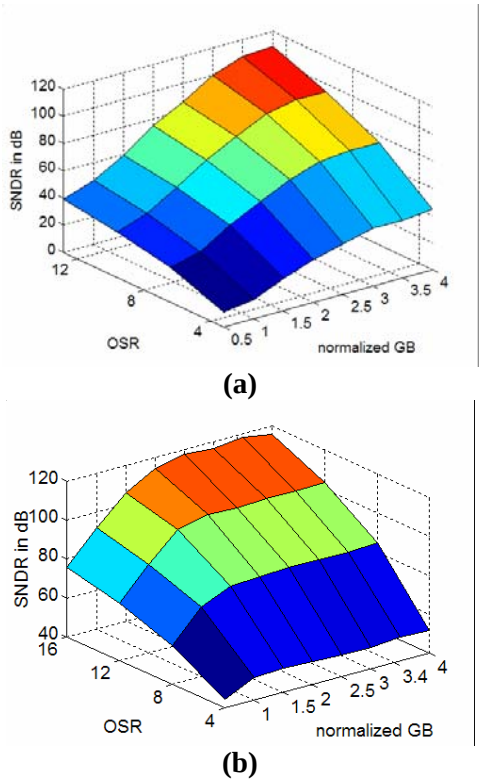

Fig.5 SNDR vs normalized GB and OSR of (a) the 2-1-1-1 cascade [4] , and (b) the proposed one in this paper with N=4.

Returning to the proposed 4-b quantizer in the first stage, note that the quantization noise is low, so that the quantization noise leakage is significantly low. The new modulator architecture dramatically relaxes the requirements of high precision analog stages especially that of opamps with high dc-gain, which is more difficult to obtain as IC technologies advance [10].

Finally, the proposed architecture is insensitive to the nonlinearity of opamps by inserting the additional feed-forward path from the modulator input directly to the quantizer input in the first stage, where the loop filter processes only shaped quantization noise. Since, ideally, no input signal is processed by the loop-filter integrators; therefore, no harmonic distortion is generated [9].

4 Simulation Results

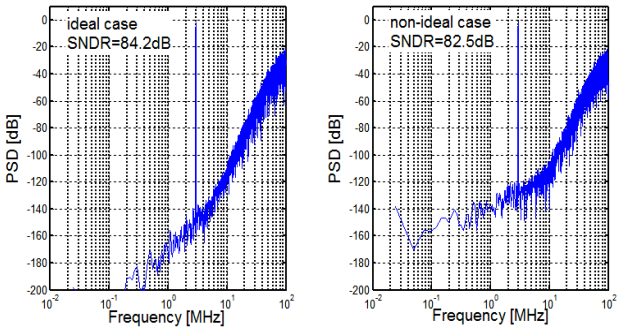

Fig. 6 The output spectra of the proposed 2(4b)-1-1-1(4b) (a) with ideal case, (b) with circuit non-idealities

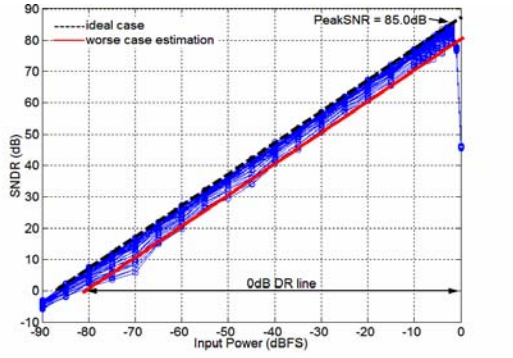

Fig. 7 The SNDR against input level in the proposed Sigma-Delta modulator with Monte Carlo analysis.

The proposed architecture has been validated by behavior simulation of a 2(4b)-1-1-1(4b) modulator in MATLAB®. The modulator was designed with a sampling rate of 200 MHz, a fixed OSR of 8, yielding a signal bandwidth of 12.5 MHz. The input is a 3 MHz sine-wave signal with amplitude of -3 dBFS. The 4 bit

quantizers are used for the first- and last stage modulators, and the single-bit quantizers are used for other modulators. The scaling loop gains are set as mentioned before. The finite opamp dc gain, unity-gain frequency, and capacitor mismatching in the integrators of the first stage are set to 55 dB, 400 MHz (SR≈260 V/μs) and 0.1%, respectively.

The output spectra of the ideal case and the aforementioned non-ideal case are shown in Fig. 6. The achievable SNDR is 84.2 dB and 82.5 dB, respectively. Fig. 7 illustrates the SNDR against the input level for the proposed modulator with Monte Carlo analysis of 30 times, where not only the process variation of capacitors are considered as the worst case σ_C=0.5%, but also the design parameter variation of finite opamp dc gain and GBW frequency are assumed as large as 20% deviated from their nominal values, respectively. It is shown that the achievable peak SNDR and DR of the proposed modulator are not sensitive to circuit non-idealities, and even with the assumed large parameter variations the performance degradation is only about 6 dB.

Table 1 presents the predicted performance summary of the proposed 2(4b)-1-1-1-(4b) Sigma-Delta modulator.

Sampling frequency	**200**	**MHz**
Digital output rate (M=8)	**25**	**MS/s**
DR(ideal case)	**85**	**dB**
Peak SNDR(nonideal case)	**82.5**	**dB**
Peak SNDR(worse case)	**79.2**	**dB**
DR (ideal case)	**87.8**	**dB**
DR (worse case)	**81.5**	**dB**
Estimated Power Consumption (1.8Vsupply)	**120-150**	**mW**

Table 1 performance summary

5 Conclusion

An architecture of the wideband and high-DR cascade high-order Sigma-Delta modulator is proposed. It uses the low-distortion second-order Sigma-Delta modulator as the first stage of a cascade Sigma-Delta modulator, therefore both integrators in the first stage process only low power quantization noise. Consequently, the requirement on the opamp gain-bandwidth-product of the proposed Sigma-Delta modulator is significantly relaxed by 2 *fs*, which is lower than *4* f_S in other traditional Sigma-Delta modulator implementations. On the other hand, using a multibit quantizer in the first stage reduces the sensitivity to non-idealities of circuits, such as finite dc-gain of opamps and capacitor mismatching. Hence, the proposed architecture is a suitable candidate for wideband, high-resolution and low-power applications.

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