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Carbon Nanotube Field Effect Transistors with improved Characteristics

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Abstract: - Using Schrodinger-Poisson formalism, a carbon nanotube field effect transistor (CNTFET) is studied. To improve the saturation range in the output characteristics, new transistor structures are proposed. These structures are simulated and compared with the conventional structure. It is shown that proposed structures have better output characteristics.

Key-Words: - Carbon nanotube, FET, Simulation, Schrodinger equation, CNT.

1 Introduction

A CNT is a sheet of graphite rulled-up as a tube, with a diameter typically in the nanometer range, which can be from less than one nanometer, up to several nanometers. CNTs are one dimensional (1-D) devices in which electron transport is quasi ballistic. Moreover, mobility of CNTs is considerably larger than silicon and can be as large as 10^5 $cm^2/V.S$ [1]. These properties have emerged CNTs as candidate for nanometer (10nm) electronic technology [2-5].

CNTs can be semiconducting or metallic according to the chiral vector [6]. Single wall semiconducting CNTs, with few nanometers in diameter can be used as channels for field effect transistors (FETs).

In this paper a zig-zag CNT field effect transistor (CNTFET) with Schottkey barrier contacts is simulated and its characteristics are evaluated. Then, novel structures are proposed which have superior characteristics, specially, for digital applications. Section 2 deals with modeling of a conventional CNTFET structure. In section 3 new structures are proposed and their I-V is discussed. Main conclusions are summarized in section 4.

2 CNT modeling

We consider a (16,0) nanotube with radius R_t=0.6nm, bandgap E_g=0.62ev, dielectric constant ε_t=1, and the tube length L_t=20nm. Due to the azimuthal symmetry of the tube, the simulation domain is two dimensional (2-D). The gate insulator has ε_{ins}=25 and thickness R_g=2.5nm. Drain and source metals make Schottkey contact to the channel with Φ_b=0.3ev. Figure 1 shows the CNTFET structure.

To derive I-V characteristics of the transistor, the 1-D Schrodinger equation is solved consistently with the Poisson's equation. Poisson's equation with azimuthal symmetry is:

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho}\frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\varepsilon} \qquad (1)$$

In this equation ρ is the tube radial direction, z is the channel direction, Q is the charge density on the tube surface and is derived from Schrodinger equation. Poisson's equation is solved using finite difference method. The charge density is zero everywhere except at the tube surface:

$$Q = \frac{q(p-n)}{2\pi}\frac{\delta(\rho - R_t)}{\rho} \qquad (2)$$

Where n and p are electron and hole densities respectively and are derived from the Schrodinger equation. In the carbon nanotube, the electron transport is almost ballistic therefore, the Schrodinger equation is solved to compute the charge density and the transmission probability:

$$\frac{\partial^2 \Psi}{\partial z^2} = -\frac{2m}{\hbar^2}(E-U)\Psi \qquad (3)$$

Where E is the electron or hole energy, U is the potential energy, which is –qV for the electron and $qV+E_g$ for the hole. The Schrodinger equation is solved using centeral difference discretization method.

Upon computing the transmission probability TC, the drain-source current is derived from [7]:

$$I^{n,p} = \frac{4q}{\hbar}\int dE\left[f_S^{n,p}(E) - f_D^{n,p}(E)\right]TC^{n,p}(E) \quad (4)$$

Where the superscripts n and p stand for electron and hole respectively. For a conventional CNTFET depicted in Fig.1, drain current (Id) versus drain-source voltage (Vds) for various gate-source voltages (Vgs) is shown in Fig. 2. For Vds up to 0.6V, output characteristics is similar to conventional FET transistors. But for larger voltages, the drain current is suddenly increased. This is due to the hole injection from the drain to the source. As this figure shows, the saturation region in the output characteristics is about 0.6V, which is small for typical applications. Figure 3 shows the electron potential energy for the gate voltage Vgs=0.4V and three values of drain voltages. For Vds=0.2V electrons surmount (or tunnel) through the source and drain Schottkey barriers and this makes the drain current. With increasing the drain voltage, the potential on the drain side decreases and the electron current increases. At a special Vds, the drain barrier vanishes. If the Schottkey barrier equals $E_g/2$, at Vds=Vgs the drain barrier vanishes. In Fig. 3 this happens for Vds=0.4V. For larger Vds, hole injection is increased. At Vds=2Vgs Hole and electron current would be equal. Beyond Vds=2Vgs, hole current will increase exponentially, as is known for a Schottkey diode.

3 Novel transistor structures

In the conventional CNTFETs, for low Vgs, exponentially increasing of the drain current takes place at low drain voltages (tens of 1V). This limits usage of the transistor for most applications, specially for digital circuits. To overcome this problem, one must prevent the drain Schottkey diode from entering on state, and consequently increase the saturation range in the output characteristics. In this section, novel structures are proposed in order to increase the saturation range.

3.1 Double dielectric

For the transistor of Fig. 1, if an insulator with higher dielectric is used, the gate control on the channel increases and vice-verse. Keeping this in mind, the transistor in Fig. 4 is proposed, in which, gate length is divided into two equal sections. In this transistor, the gate dielectric at the drain side is selected from a material with lower dielectric constant. Therefore, the gate control on the drain side of the channel is decreased. Figure 5 shows Id-Vds for this transistor. The dielectric constant at the drain side is assumed 5, whereas at the source side the dielectric constant is assumed 25. As Fig. 5 shows, the saturation range of the transistor is slightly increased.

3.2 Double metal gate

In this structure, as the previous one, the gate length is divided into two parts, with uniform dielectric, but with different gate metals. The gate metal on the drain side is selected with lower work function. Fig. 6 shows Id-Vds for a transistor with gate metal of 0.2V lower work function. This figure shows that the current saturation portion is almost 0.2V wider than the conventional transistor.

3.3 Partially gate metallization

In this structure the gate metal on the drain side is not deposited. With this, gate affects the channel near the source, and has no effect on the channel near the drain. Figure 7 depicts the Id-Vds characteristics of the transistor. It is obvious from this figure that the saturation range of this transistor is wider than two former structures. Moreover this structure is easier to fabricate.

4 Conclusion

A CNTFET is simulated based on Schrodinger-Poisson formalism. This evaluation showed that the saturation range in the output characteristics is small. Three different structures are proposed to increase this range. These structures are evaluated and it is shown that proposed transistors have wider

FET saturation range. This makes them suitable for digital applications.

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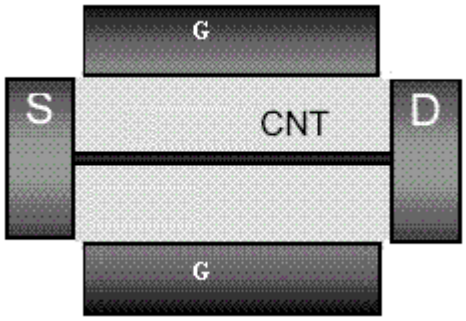

Fig. 1 CNTFET structure

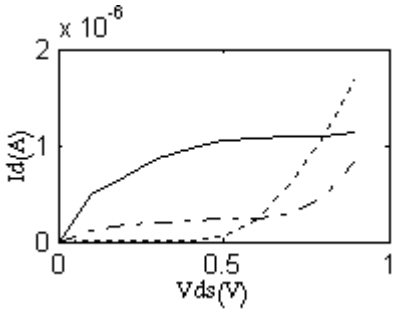

Fig.2 Id-Vds for Vgs=0.2V (dot), 0.4V (dash-dot) and 0.6V (solid)

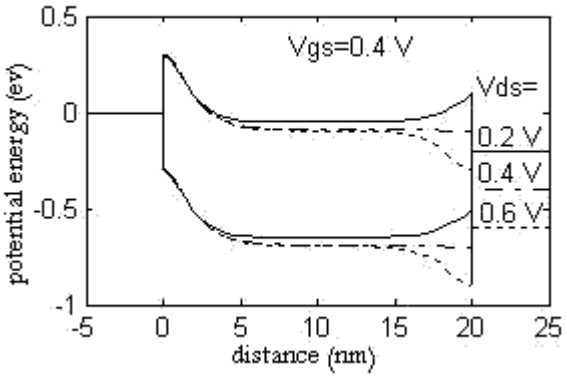

Fig. 3 potential energy for Vgs=0.2V and Vds=0.2V (solid), 0.4V (dash-dot) and 0.6V (dot)

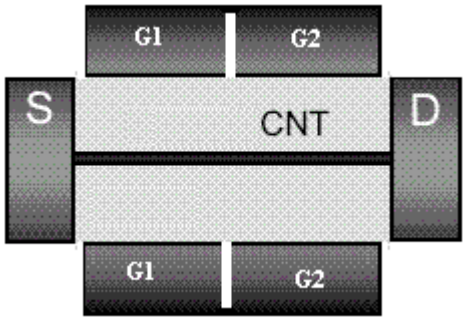

Fig. 4 CNTFET with split gate

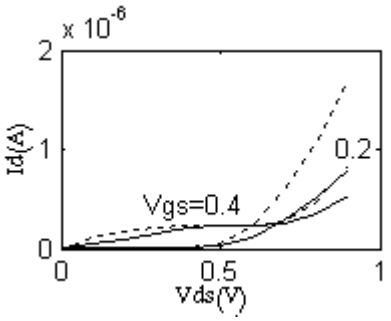

Fig. 5 Id-Vds for transistor proposed In section 4-1 (solid) and conventional transistor (dot)

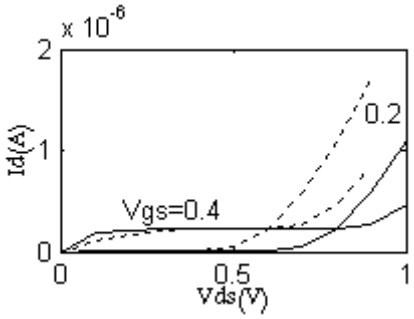

Fig. 6 Id-Vds for transistor proposed in section 4-2 (solid) and conventional transistor (dot)

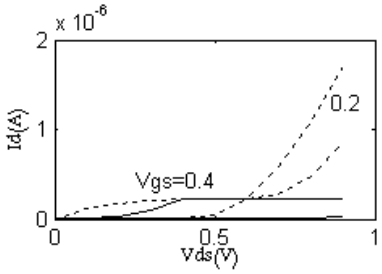

Fig. 7 Id-Vds for transistor proposed in section 4-3 (solid) and conventional transistor (dot)