Proceedings of the 5th WSEAS Int. Conf. on Instrumentation, Measurement, Circuits and Systems, Hangzhou, China, April 16-18, 2006 (pp170-174)

High Speed and Large Capacity Solid state recorder for Radar video signal

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Abstract: Purpose: Developing solid state recorder for video signal of active and passive radar homing seeker. Methods: The recorder has been realized by using 12-Bit, 105 MSPS A/D Converter, FPGA as main control logic chip, FLASH memory as storage medium. Results: The recorder has successfully been used in ground trial and radar seeker. The sample precision of the recorder can achieve 0.1%, while the capacity 6GByte, sampling rate 60M. Conclusion: The trial on radar seeker shows that the recorder can perform with high sampling precision and steady performance.

Key-words: Radar video signal, High speed data acquisition, Solid state recorder, FPGA, FLASH memory, A/D converter

1 Introduction

Along with the quick development of science and technology, radar homing equipment plays more and more important role in army-civilian field [1]. Either guidance of aircraft and airship docking, or vehicles monitoring, precision recognition to the goal is needed [2] [3]. In order to improve the precise recognition capability, other than advanced initial information safeguard system and ensuring at first and second section of the flight, homing technology at the final section should be adopted [4]. To the maneuvering target, homing guidance proves to be especially important, while to the fixed target, when the aiming error is relative big, radar seek equipment is also necessary for accurate guidance [5]. So, developing high quality radar homing equipment is meaningful on remarkably improving recognition capability of selected target [6] [7].

The recorder in this paper is designed for active and passive radar homing detection. Three groups of I and Q video signals are sample at the same time by using high speed A/D converter. Peak value of each channel is the total sampling rate is 60MSPS, that is to say, peak value of total sampling rate is 360MSPS. In the recorder, 12-Bit A/D converter which can provides sample precision of 0.1% is used. Total data storage capacity can reach 6GByte. Using USB2.0 interface, we can read video data from record and transform to selected data format.

2 Holistic Design of the Recorder

The recorder is made up of USB control card, acquisition control card, three acquisition and storage cards, power card and back plane, the block diagram of which is shown in Fig1.

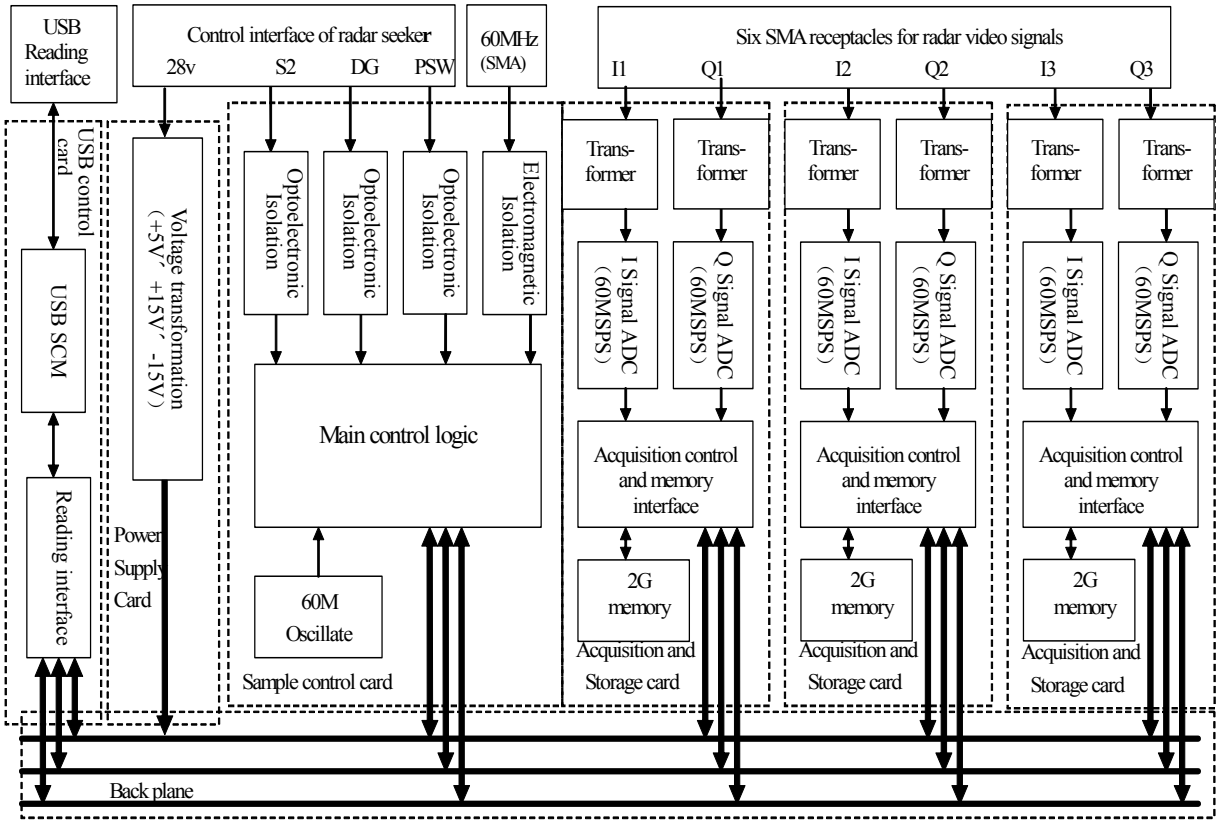

Fig.1 Block diagram of the solid state recorder

3 groups of I, Q signals and the 60MHz clock signal are connected to the recorder using 7 SMA receptacles, while control signals of the radar seeker and power sources are provided to the recorder through a digital interface. All signals connected to the recorder are isolated to each other

After isolated by DC-DC, +28V from the digital interface provides power for each unit of the whole recording system.

The five function modes of the recorder are: acquisition and recording, data holding, data erasing, data reading and self-checking. Operations of acquisition control and data storage are completed by logic unit which uses FPGA as main chip.

2.1 Time sequence of acquisition

When the recorder is fixed on radar seeker, it starts to sample while the power-on signal (S2) changes for high level.

During each period of trigger signal (DG), the recorder samples 3 groups of I and Q video signals after XμS delay from DG's trailing edge until rising edge comes. Sampling rate for each channel is 60MSPS and effective bit of the A/d acquisition is 12-bit.

The delay time is defined by delay control signal (PWS). When PWS is at low level, the delay is X1μs, while when PWS turns into high level, the delay is X1μs.

2.2 The control of acquisition signal format in date recording

Taking the width error trigger signal (DG) into consideration, if DG pulse is used to control acquisition, the length of data flow collected during each period is not the same. This will bring difficulty in resuming the original data. So, frame synchronization marks and timing marks are added at the end of every group of data. The format of the marks is shown in Table1.

Table 1 The Structure of Marks

Number	Definition
1	Time（The lowest byte）
2	Time
3	Time
4	Time
5	Time
6	Time（The highest byte）
7	000H
8	000H
9	0FFH
10	0FFH

As indicated in the table above, the first six bytes of the mark are timing mark, while the rest bytes are frame synchronization mark. The time of each LSB is 16.667nS（1/60MHZ）, so the longest recording time is 4691249s. 12-bit data acquired by A/D converter is storage as two byte with the highest four bits being 0000.

2.3 Data Reading of the recorder

The computer on ground read the data of recorder by the reading interface. The computer and sample equipment is interconnected by USB2.0; the reading speed is quicker than 10MByte/s. Data flow is read through back plane bus from acquisition and storage cards one by one in the process of reading. Data is read by inverted order, that is to say, data stored latest is read first, while data stored first is read last. In order to improve the speed of reading, there is an index area in FLASH memory marked the initial address. Only the useful data is read while the data of vacant area can be identified automatically when reading.

3 Key technologies

3.1 Circulatory read-write technology to FLASH memories [8] [9]

The 128Mbyte FLASH memory is selected as storage medium. Because buffer of FLASH memory is 2kByte and the maximum writing speed is 20MByte/s, we can calculate that the time for writing buffer is more than 100μs, while time for programming data in the buffer is between 200μs and 700μs. If we make a FLASH array composed of 8 pieces 128MByte memories, the buffer of it will reach 16kByte. If the writing speed is continuously 20MByte/s, time for writing 7 pieces of them is about 700μs which is more than the longest time for programming. From the calculation above, we can know that, after writing to the buffers of the 8 pieces FLASH memories in turn, the programming operation of the first has completed. Then we can carry out writing operation to the buffer to the first FLASH memory, again and again, until the whole memory is full.

3.2 The realization of A/D acquisition and data buffering

Using 12 bit, 60MSPS A/D converter, the acquisition module of recording system can create 60M 12-bit data per second, while the maximum writing speed for large capability memory is 20MByte/s. So, high speed data transmission and storage become the bottleneck of solid state recorder design. In this paper, technologies based on high speed FIFO and paging memory is adopted to solve the problems. The block diagram of acquisition card can be described as Fig2.

After isolated by transformer, I and Q signals are acquired by AD9432 (sampling rate is 60MSPS). Then the 12-bit data flow which is expanded to16-bit by setting 0000 to highest four bits is written into 16-bit high speed FIFO for buffering. At last, data are transferred from FIFO to FLASH memories at the speed of 10MWord/s. Data are stored into FLASH memories by means of low byte first and high byte last.

The process of acquisition and storage is controlled by FPGA logical unit which not only can provide high speed for the whole system, but can be maintained easily.

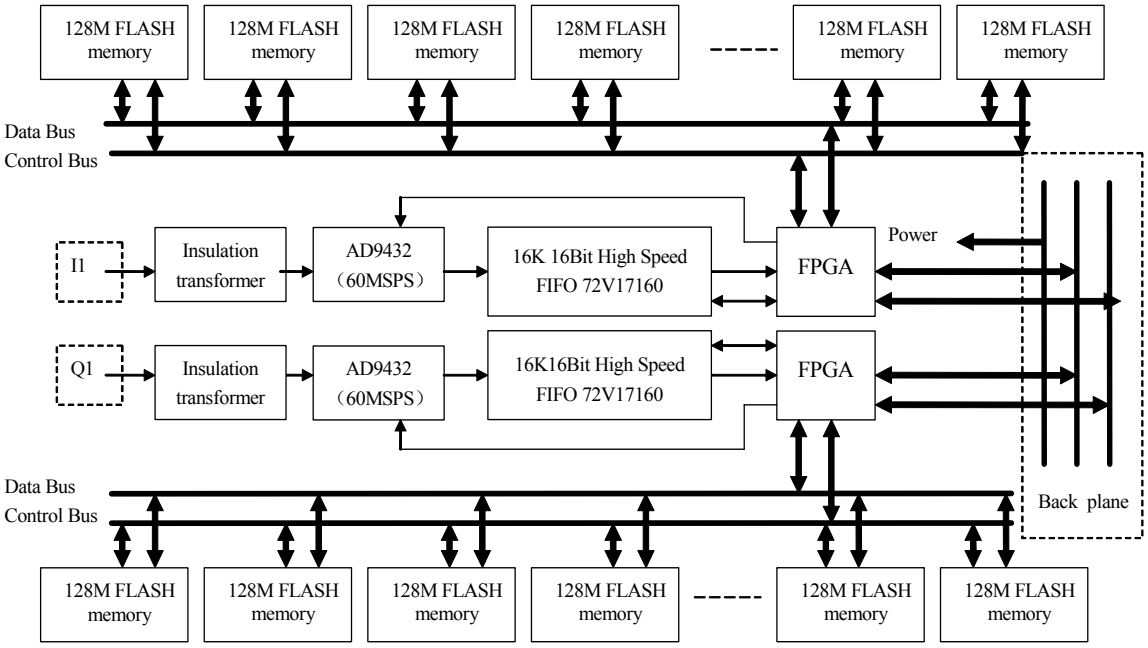

Fig.2 Block diagram of the acquisition and storage card

3.3 The Control of Phase error

In the system, 6 channel I and Q signals are required to be synchronous and the delay time among channels can't exceed 0.55ns. To solve the problem, measures as follows are taken: the same clock signal is used for the collection of 3 pairs of I and Q signals; in order to obtain an intact ground, 4 layers PCB circuit is adopted; wiring between back plane and A/D converter for each pair of I and Q signals is symmetrical to make the transmission time match each other; A/D converter and logic devices with the same performance is selected to assure that there are the delay when signal pass the devices; the wire splice between the back plane and acquisition card is adjusted slightly to achieve accurate match.

By taking measures above, Phase error between channels of the system will be controlled into acceptable scope.

3.4 The realization of high speed, high accuracy and high reliability

Start and stop operation for acquisition has the character of unplanned and intermittent, so the delay for A/D acquisition can't be too long. Traditional method for start and stop acquisition using electronic switch for channel switching will bring big delay on time sequence, which then will affect the precision of the acquisition. So, on each acquisition card, two A/D converters are used for acquisition I and Q signals separately. By doing this, a lot of problems brought by switching analog channels are avoided.

In addition, each channel acquisition and storage separately can lighten the pressure of data flow, making the system achieve total sampling rate of 360MSPS.

Acquisition control, data storage and reading operation are completed by FPGA. The logic in the FPGA is realized by hardware description language, which makes the functional mode of the recorder be clear and maintainable. Synchronized logic is adopted in internal module circuits to avoid race and hazard and improve the reliable of the system [10].

Moreover, all the signals between the recorder and radar are isolated by transformer or photocoupler, and the power is isolated by DC-DC. Measures of isolation improve the anti- interference ability of the system. Impedance matching is used at

the input interface to eliminate echo. Low ripple power is adopted in the system to avoid interference.

4. Conclusion

The recorder proves to be stable and reliable after environmental stress test, system ground association test and flight test. If the technology of data compression is adopted in the recorder, the performance storage capacity and recording time change for the better.

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