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Effect of Finite Amplifier Gain, Bandwidth, and Non-Idealities of Switches in Switched Capacitor Ladder Circuits

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Abstract: In this paper, a realization of stray-insensitive third order ladder filter using switched capacitor (SC) circuits has been presented. MATLAB has been used to analyze the ladder filter to determine the errors in their transfer functions due to the finite gain and finite bandwidth of the op-amp. The z-domain transfer function of the ladder filter is expanded using Continued Fraction Expansion. Each row of the expansion is a transfer function of leaky inverting or non-inverting integrator. Higher order circuits are realized by connecting the switched capacitor blocks of amplifier and integrator in ladder form. The implementation of this higher order circuit is done using Or CAD Pspice. The frequency response of the SC amplifier and integrator is obtained in z-domain analytically, considering the effect of finite gain and finite bandwidth. The relative magnitude and phase errors obtained by comparing the frequency responses of the ideal and actual filter transfer function are plotted using MATLAB. The ladder filter is also simulated on MATLAB and a comparison of results with OrCAD Pspice is also presented.

Key-Words: Switched capacitor circuits, ladder filter, finite amplifier gain and bandwidth.

1. Introduction

Switched capacitor circuits are intricate systems containing many components and multiple feedback loops, and are realized normally in a fully integrated form. They have inherent advantages of CMOS compatibility, programmability, good voltage linearity, flexibility, better accuracy and stability and ease of fabrication. As a result of the integrated realization, many unavoidable parasitic effects occur in the circuit. If these non-ideal effects are not considered carefully, then there is a sufficient loss in performance of the circuit when fabricated. These parasitic effects include non-ideal effects in the switches and capacitors, non-ideal op-amp effects like finite gain and bandwidth effect, settling behaviour and non-zero output resistance.

The influence of op-amp non-idealities and switch on-resistance on the performance of switched capacitor circuits has been investigated in [1-5] and their combined influence has been analyzed in [6-7].

In this paper, the effect of non-ideal switches, clock feedthrough and effect of finite gain and bandwidth on a stray insensitive third order ladder filter have been considered. The errors in transfer function due to finite op-amp gain and bandwidth of SC amplifier and integrator are derived. These errors in the magnitude and phase of the transfer function are plotted in MATLAB. These errors are useful in designing filter circuits on chip. The third order ladder filter is also simulated in Or CAD Pspice and the results compared with those obtained using MATLAB.

The paper is organized as follows: Section 2 discusses the effect of non-zero on-resistance and clock feedthrough on switches. In Section 3, the errors in transfer functions of the basic switched capacitor integrator and amplifier blocks due to finite gain and bandwidth of op-amp are derived. Section 4 explains the Continued Fraction Expansion technique used to realize the switched capacitor stray insensitive third order ladder filter. Section 5 presents the MATLAB simulation results of the errors in magnitude and phase, and the Or CAD Pspice simulation results of the third order ladder filter taking into account the effect of the non-idealities discussed in the paper.

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2. Effect of non-zero on-resistance and clock feedthrough of switches

2.1 Non-zero on resistance

The off-resistance of the MOSFET switch is high so that they can be considered as open circuited. "On" resistance R_{on} depends on the actual dimensions of the switch. The value of the on-resistance for a MOSFET (Fig 1) in an IC is of the order of 2 to 10 KΩ [9].

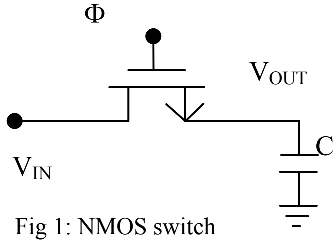

Fig 1: NMOS switch

The instantaneous value of the clock signal on the gates of the MOSFETs used as switches is usually the supply voltage (V_{DD} or V_{SS}) of the circuit. Thus, for $[v_{GS} - V_T] \rangle |v_{DS}|$ the device is "on", it is in the non-saturated region and behaves as a linear resistor of value

$$R_{on} = \frac{1}{2k(v_{GS} - V_T)} \tag{1}$$

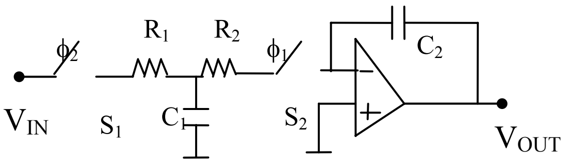

Fig 2: Switched capacitor integrator

A simple Switched Capacitor integrator is considered (Fig 2). In the ideal case, when $R_1=R_2=0$, the transfer function is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-C_1/C_2}{z-1} \tag{2}$$

Assuming that the switch resistances $R_1=R_2=R$ are linear, the new transfer function is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-(1-e^{-T/2RC_1})^2\, C_1/C_2}{z-1} \tag{3}$$

Comparing the above two equations, it is observed that the on-resistances reduce the effective value of the capacitance ratio C_1/C_2 . The relative error is

$$\varepsilon = 1-(1-e^{-T/2RC_1})^2 \cong 2e^{-T/2RC_1} \tag{4}$$

Thus $RC_1 \leq T/20$ (5)

will minimize the effect of non-zero on resistance.

2.2 Effect of Clock feedthrough

In addition to the channel current I_D, there are capacitive currents associated with the transient response of the MOSFET [8]. Of the several stray capacitances present, the two gate capacitances C_{gd} and C_{gs} are of importance in switching applications. These capacitances are responsible for clock feedthrough noise of voltage comparable to the signal. To compensate for the clock feedthrough effect complementary type transistors called transmission gates are used (Fig 3). The clock feedthrough is eliminated since at least one of the two devices will always conduct whenever ϕ is high regardless of the signal level v_{in}. The maximum on-resistance of CMOS switch is 16kΩ.

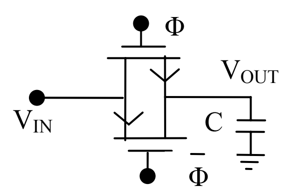

Fig 3: CMOS Transmission gate

3. Effect Of Finite Op-Amp Gain And Bandwidth

3.1 Effect Of Finite DC Gain

The effect of the finite dc gain A_0 is derived for the switched capacitor integrator of Fig 4. In phase Φ_1, the capacitor C gets charged to the input voltage V_{IN}. In the next phase Φ_2, the charge on C is distributed on capacitors α and β. The output is also obtained in phase Φ_2. The expressions are as follows:

In phase Φ_1 (Fig 5a)

$$v^o_{C1}(n-1) = v^o_{in}(n-1) \tag{6}$$

$$v^o_{\beta C2}(n-1) = v^o_{out}(n-1) - \frac{v^o_{out}(n-1)}{A_o} \tag{7}$$

$$v^e_{out}(n-1/2) = \left(\frac{C_1}{(1+\beta)C_2}\right) v^o_{in}(n-1) + \left(1+\frac{C_1}{(1+\beta)C_2}\right)\frac{v^e_{out}(n-1/2)}{A_o} + v^o_{\beta C2}(n-1)\left(\frac{\beta}{1+\beta}\right) \tag{8}$$

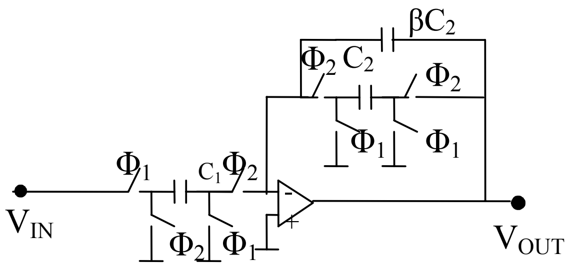

Fig 4: Switched capacitor integrator used as building block of the third order ladder filter

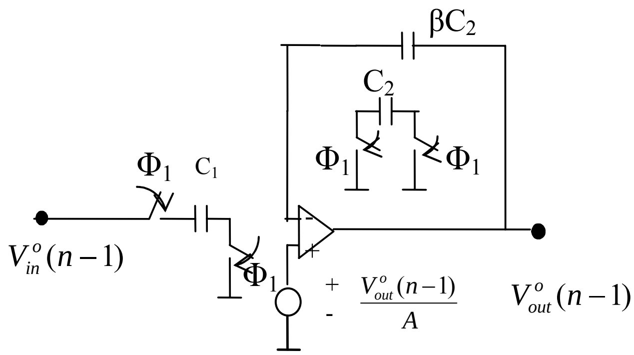

Fig 5a: Switched capacitor integrator in phase Φ_1

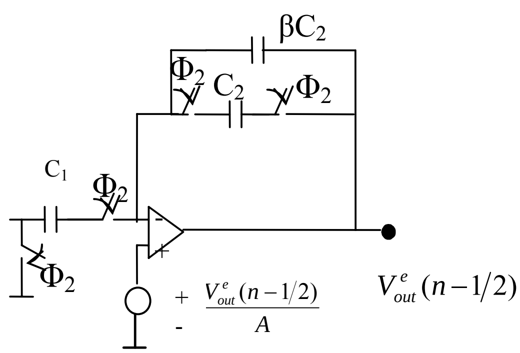

Fig 5b: Switched capacitor integrator in phase Φ_2

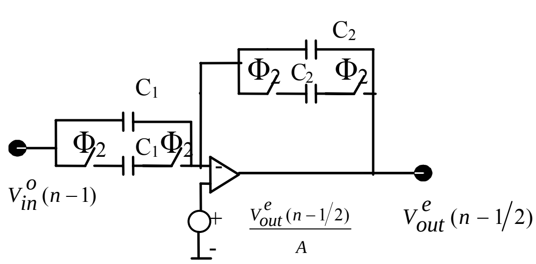

Fig 6: Switched capacitor amplifier

In phase Φ_2 (Fig 5b)

$$v_{out}^{o}(n) = \left(\frac{C_1}{(1+\beta)C_2}\right) v_{in}^{o}(n-1) + \left[1 + \frac{C_1}{(1+\beta)C_2}\frac{v_{out}^{o}(n)}{A_o} + \left(\frac{\beta}{1+\beta}\right)\left(v_{out}^{o}(n-1) - \frac{v_{out}^{o}(n-1)}{A_o}\right)\right] \tag{9}$$

Taking z-transforms of eqn. (8) and (9),

$$H^{oo}(z) = \frac{H_I(z)}{\left[1 + \dfrac{z^{-1}\beta C_2 - C_1}{C_2 A_o(1+\beta(1-z^{-1}))}\right]} \tag{10}$$

where $H_I(z) = \dfrac{C_1 z^{-1}}{C_2(1+\beta(1-z^{-1}))}$ is the ideal transfer function with $A_o \to \infty$

Substituting $z \approx \exp(j\omega T)$ and $e^{-j\omega T} = \cos\omega T - j\sin\omega T$ in $H^{oo}(z)$ frequency response of the integrator of Fig 4 with finite-gain op-amp is

$$H^{oo}(e^{j\omega T}) = \frac{H_I(e^{j\omega T})}{\left[1 + \left(\dfrac{\beta C_2\cos\omega T + \beta^2 C_2\cos\omega T + \beta C_1\cos\omega T - C_1 - \beta^2 C_2 - \beta C_1}{C_2 A_o(1+2\beta^2(1-\cos\omega T)+2\beta(1-\cos\omega T))}\right) - j\left(\dfrac{\beta C_2\sin\omega T + \beta^2 C_2\sin\omega T - \beta C_1\sin\omega T}{C_2 A_o(1+2\beta^2(1-\cos\omega T)+2\beta(1-\cos\omega T))}\right)\right]} \tag{11}$$

The actual frequency response can be written in the form

$$H^{oo}(e^{j\omega T}) = \frac{H_I(e^{j\omega T})}{[1+m(\omega) - j\theta(\omega)]} \tag{12}$$

where

$$m(\omega) = -\left(\frac{\beta C_2\cos\omega T + \beta^2 C_2\cos\omega T + \beta C_1\cos\omega T - C_1 - \beta^2 C_2 - \beta C_1}{C_2 A_o(1+2\beta^2(1-\cos\omega T)+2\beta(1-\cos\omega T))}\right)$$

and

$$\theta(\omega) = \frac{(\beta C_2\sin\omega T + \beta^2 C_2\sin\omega T - \beta C_1\sin\omega T)}{C_2 A_o(1+2\beta^2(1-\cos\omega T)+2\beta(1-\cos\omega T))}$$

for $\omega T \langle\langle 1$

Here, $m(\omega)$ and $\theta(\omega)$ are the relative errors in magnitude and phase.

Similarly, it can be derived that the actual frequency response of the Switched Capacitor amplifier (Fig 6) is

$$H^{oo}(e^{j\omega T}) = \frac{H_I(e^{j\omega T})}{[1+m(\omega) - j\theta(\omega)]} \tag{13}$$

where $m(\omega) = -(1 + C_1/C_2)1/A$ and $\theta(\omega) = 0$

3.2 Effect Of Finite Op-Amp Bandwidth

The effect of finite bandwidth on the switched capacitor integrator is studied. Assuming that the op-amp response $A_v(s)$ has widely separated poles and there is only one dominant pole s_1 which affects the frequency response, then

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)} \approx \frac{-\omega_0}{s - s_1} \approx \frac{-1}{1/A_0 + s/\omega_0} \qquad (14)$$

Here A_0 is the dc gain, and ω_0 is the unity-gain bandwidth of the op-amp. V_{out} is the output and V_{in} is the input voltage of the amplifier. The actual frequency response is

$$H^{oo}(\omega) = \frac{-C_1/C_2 e^{-j\omega T/2}}{2j\sin\omega T/2}\left[\begin{array}{l} 1 + e^{-k_1}\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\cos\omega T - e^{-k_1} - \\ je^{-k_1}\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\sin\omega T \end{array}\right] \qquad (15)$$

$$H^{oo}(\omega) = H_I(\omega)\left[\begin{array}{l} 1 + e^{-k_1}\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\cos\omega T - e^{-k_1} - \\ je^{-k_1}\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\sin\omega T \end{array}\right] \qquad (16)$$

from eqn. (16), we obtain

$$m(\omega) = e^{-k_1}\left[\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\cos\omega T - 1\right]$$

and $\theta(\omega) = -e^{-k_1}\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\sin\omega T$

where $k_1 = \pi\left(\frac{C_{eq}}{C_1 + C_{eq}}\right)\frac{f_0}{f_c}$ and $C_{eq} = (1+\beta)C_2$

For the switched capacitor amplifier the actual frequency response is

$$H_a(\omega) = -(C_1/C_2)(1 - e^{-k_1}) \qquad (17)$$

The error functions are

$m(\omega) = -e^{-k_1}$ and $\theta(\omega) = 0$

Using Mason Gain's Formula, the combined error in magnitude and phase for the third order ladder filter is obtained.

4. Continued Fraction Expansion Technique

The transfer function of the third-order ladder filter used to determine the errors due to non-ideal effects

$$G(z) = \frac{1657z^3 - 2603z^2 + 1048z - 62.78}{49z^3 - 49z^2 + 7z + 1} \qquad (18)$$

This transfer function can be expanded into several mixed Cauer forms. One of the expansions is

$$G_1(z) = -A_0 + \cfrac{1}{g_1(z) - \cfrac{1}{g_2(z) - \cfrac{1}{g_3(z)}}}$$

$$G(z) = -62.78 * G_1(z) \qquad (19)$$

where

$A_0 = 0.538$; $g_1(z) = 3.25z - 0.464$;

$g_2(z) = 3.76z - 1.6236$; $g_3(z) = 3.23z - 1.381$

In eqn. (19), the constant A_0 can be realized using a SC amplifier / attenuator, and $1/g_i(z)$; i = 1,2,3 are transfer functions of integrator of the form:

$$+\left[\frac{1}{B_p z - A_p - G_{m,p+1}(z)}\right] \qquad (20)$$

The SC realization [9-10] of the ladder filter is shown in Fig 7. The symbols ϕ_1 and ϕ_2 represent non-overlapping clocks.

In order to account for the on-resistance of switch, CMOS transmission gates (Fig 7) have been used as switches. To compensate the effect of clock feedthrough the size of MOSFETs used is small (l = 2μ and w =5μ). Folded cascade op-amp has been used to compensate for non-ideal effects of op-amp.

The circuits are implemented using Or CAD Pspice 9.1. Level - 3 MOSFETS have been used for implementing transmission gates. The clock frequency chosen is 10 kHz.

5. Results

In this paper, a Switched Capacitor realization of third order ladder filter has been implemented using Or CAD Pspice. The errors in magnitude and phase due to the non-idealities of switches and finite op-amp gain and bandwidth have been determined for the third order ladder filter and analyzed using MATLAB. Fig 8 shows the Pspice simulation results of the ladder filter and compares it with plot of s-domain equivalent of the third order filter transfer function. This is the transfer function of a half differentiator $s^{1/2}$. The magnitude plot increases with increase in frequency and the phase is 45°. It is observed that both the plots match with each other in magnitude and phase.

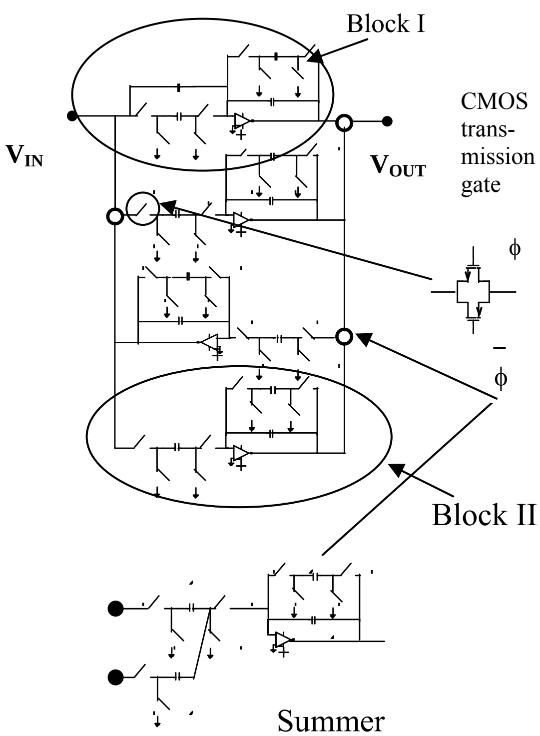

Fig 7: Switched capacitor realization of third order ladder filter

(a)

(b)

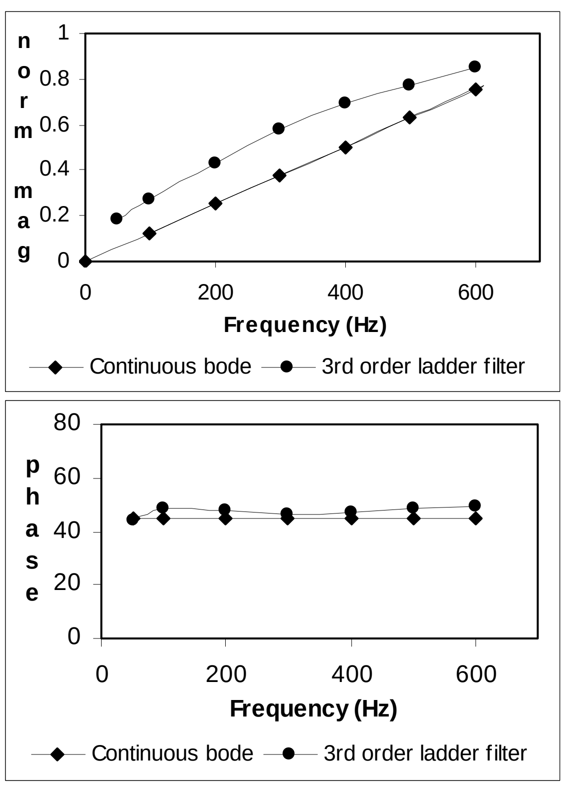

Fig 8: OrCAD Pspice results of third order ladder filter a) magnitude b) phase

Figs 9 a-d show the MATLAB results for the errors in magnitude and phase errors of the third order ladder filter determined analytically. It is observed that there is a reduction in amplitude due to finite op-amp gain (Fig 9 a, c). The finite op-amp bandwidth has the effect of reducing the phase which can be observed from the phase plot of Fig 9d. This difference is also tabulated in Table 1.

From the plots of Fig 8, it can be inferred that the SC implementation of the third order ladder filter is a good choice.

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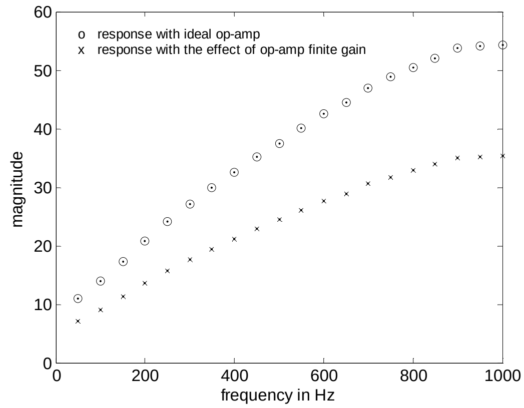
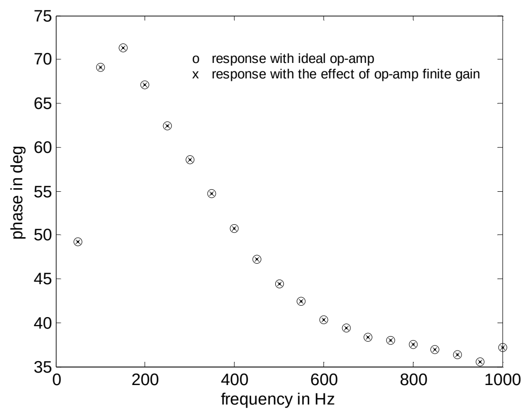
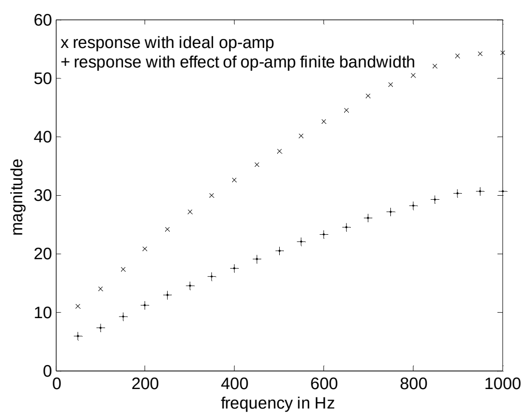


(a)

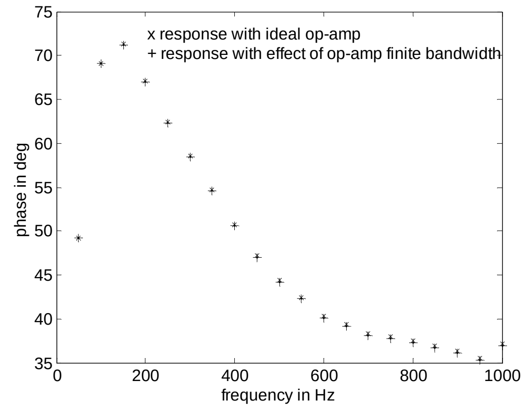


(b)



(c)

Fig 9: a-d MATLAB simulation results showing the error in magnitude and phase taking into account the effect of finite gain and bandwidth of op-amp (a, b) Effect of finite op-amp gain; (c, d) Effect of finite op-amp bandwidth



(d)

TABLE I

Effect of finite op-amp bandwidth on response of the third order ladder filter

FREQUENCY	BANDWIDTH	
	INFINITE	FINITE
50	49.202454	49.17657
100	69.100425	69.05098
150	71.301318	71.230383
200	67.093774	67.003197
250	62.392468	67.003197
300	58.599865	58.474816
350	54.694906	54.554743
400	50.771439	50.617442
450	47.188192	47.021574
500	44.379056	44.200991
550	42.467946	42.279587
600	40.33579	40.138289
650	39.382436	39.176953
700	38.284106	38.07182
750	37.926334	37.708447
800	37.466964	37.2447
850	36.881281	36.655883
900	36.393609	36.166339
950	35.547893	35.320019
1000	37.164797	36.937588