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Analysis of the Substrate Noise Effects for DC-DC Converter Integration in a 0.13µm RF CMOS Technology

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Abstract: - Substrate noise effects caused by the integration of a DC-DC converter into a 0.13 µm CMOS technology integrated circuit are investigated in this paper. Simulations performed using the Substrate Noise Analyst tool show strong impact of switching and power supply noise on a sensitive analog block. The dependence of substrate noise coupling on physical separation distance, floorplanning and introduction of guarding structures has been investigated. Simulation results highlight great efficiency of p+ guard rings closer to and surrounding sensitive nodes. Modelling of guarding structures in sub-micron technologies is mandatory to prevent noise coupling during the design stage.

Key-Words: Substrate noise coupling, substrate characterization, DC-DC converter, isolation strategies, guardring.

1 Introduction

An increasing amount of system-on-chip (SOC) has been worked out, as a result of the development of high-performance low-cost CMOS technologies. A drawback of the single-chip integration is the parasitic coupling through the shared silicon substrate that could cause important degradation of analog and RF circuits performance. The noise generation problem in both epi-type and lightly-doped-substrates as well as the propagation problem in epi-type substrates have been extensively investigated [1]-[3]. Less insight exists for noise propagation in lightly-doped-substrates. In this situation, substrate cannot be modelled as an equipotential node but has to be regarded as a three-dimensional RC-mesh, resulting in a more complicated approach and investigation. The impact of substrate noise on the analog performance is being still investigated and several experimental researches have been proposed for different ICs, designed in CMOS technology with a lightly-doped-substrate [4]-[7]. Experimental results show that lightly doped wafers are about three times less noisy than heavily doped ones and, thus, they are more advisable for mixed-signal IC manufacturing [8], [9].

A typical approach to reduce substrate noise effects is to increase noise isolation. Assuming to discriminate among sensitive blocks which require strict specifications in terms of impacting noise, changes in the floorplanning and/or introduction of specific structures surrounding sensitive node can be made to improve noise isolation.

The complexity in optimizing noise isolation depends on different technological options such as grounding, guard rings, process technology, package, shielding, decoupling.

In lightly-doped-substrates, current flowing through the substrate between two medium size contacts is mostly two dimensional with a small portion of the current flowing vertically. In this case, the separation distance and the relative positions in the floorplanning between noisy and sensitive blocks have a strong influence on noise coupling reduction. It is a common practice to place noisy and sensitive blocks as far as possible and to keep them separate using different grounding and supplies (different analog and digital voltage supplies, split ground plane, RF ground reference). Besides using these tricks, p+ diffusion guard rings surrounding the blocks (totally or partially) provide an effective isolation assuming that they are connected to a quiet supply. Better isolation is provided if guard rings are placed closer to sensitive than noisy blocks and their efficiency depends on

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noise frequency, package inductance and guard ring width [10].

This paper proposes a preliminary investigation on the substrate noise coupling effects deriving from the integration of a DC-DC converter into a Bluetooth transceiver chip. The DC-DC converter core is supposed to be one of the most noisy blocks of the IC, due to a strong switching activity and to the direct connection to the battery supply. A current mirror has been used as sensitive analog block and guarding structures have been inserted to investigate their efficiency in isolating sensitive nodes.

Among overall isolation strategies, process technology and guard ring effects related to a DC-DC converter integration will be analysed in this paper.

2. DC-DC Converter

In Fig.1 the topology of a DC-DC converter is shown. Its core is considered to be the only noise injector within the DC-DC block, while the Pulse Width Modulation (PWM) control ring is supposed not introducing additional noise into the substrate. The DC-DC converter has a standard buck-conversion topology, composed of a DRIFTMOS inverter whose output is externally connected to an LC filter [11].

Dimensions of DRIFTMOS transistors used in the core inverter design are reported below:

PDRIFT: $81\times\frac{W}{L}=\frac{100}{0.7}$ µm

NDRIFT: $25\times\frac{W}{L}=\frac{100}{0.7}$ µm.

The transistor channel length is the minimum allowed by the 0.13µm CMOS technology for DRIFTMOS devices.

The PDRIFTMOS source and bulk contacts are directly connected to a voltage battery ranging from 2.7 V to 4.8 V. In these simulations, a value of 3.6 V has been chosen as operating voltage for VPLUS. A bond- wire model has been included in the simulations. The NDRIFTMOS source and bulk, and the PDRIFTMOS substrate contacts are directly connected to the same ground reference and, also in this case, a bond-wire model has been included in the simulations.

Fig. 2 shows DRIFTMOS cross-section. Transistor contacts are highlighted: in the case of PDRIFTMOS, there is a further p+ contact surrounding the entire device used as substrate contact. Due to its large extension, it represents a possible channel for noise injection since it results to be directly connected to GND. Moreover, in both PDRIFT and NDRIFT transistors, n-wells sidewall capacitance can be neglected due to the presence of vertical EPI layers. Nevertheless, the bottom well size is strongly involved into noise capacitive coupling effects.

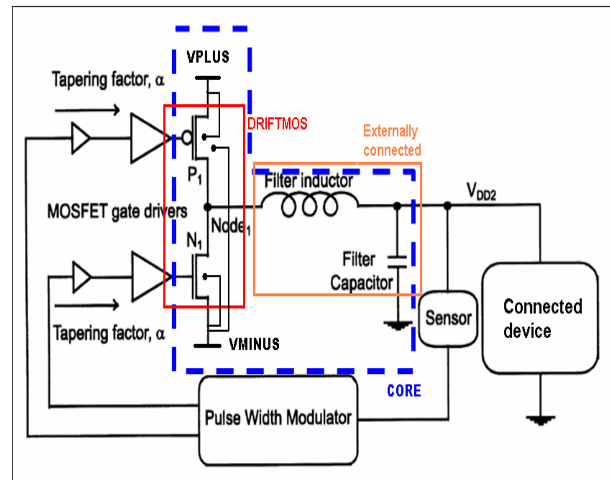

Fig. 1. DC-DC converter topology.

DRIFTMOS transistors are characterized by an higher V_{DS} value with respect to the standard transistors. This property makes DRIFTMOS suitable for application in regulator topologies, but could generate hot carriers in the conduction channel, giving rise to impact ionization effects and Hot Carrier Injection (HCI) into the substrate. HCI effects increase with scaling in transistor dimensions [12]. Nevertheless, in the DC-DC converter application, DRIFTMOS transistors operate as switches only (ON/OFF states) excluding the possibility of generating too high electric fields through the channel during both ON and OFF state.

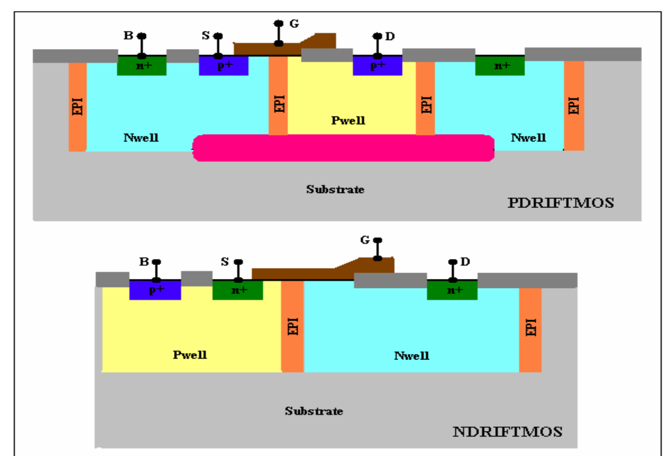

Fig. 2. DRFTMOS cross-sections.

Main causes of noise injection in the substrate are supposed to be the switching noise, due to DC-DC activity itself, and noise from power supply.
The switching noise is mostly related to DC-DC operating frequency, fixed at 2.2 MHz. Harmonic components of this frequency could have negative impact on sensitive RF outputs, as they introduce side-band spurs in the output signal spectrum. Noise from power supply depends mostly on DC-DC converter topology, as substrate is connected directly to contaminated supplies (such as battery voltage and ground) through bulks and substrate contacts.

3. Simulations and results

Calibre Substrate Noise Analyst (CalibreSNA) tool has been used for noise simulations. The first step of these simulations is the circuit layout in which noisy and sensitive nodes have been already discriminated. All the technological parameters and the doping profile are included while no backside connection is considered. Starting from the layout, a netlist describing the parasitic values extracted through SNA have been obtained for each case and imported in ELDO simulator to simulate the transient and the AC behaviour of the DC-DC converter core.
The analog block, composed of a 0.13 µm CMOS current mirror, and in particular the standard NMOS bulk contact is the one Sensitive Node (SN), while the NDRIFTMOS bulk contact is assumed to be the Noise Source (NS) referring node.
Four different topological and layout configurations have been considered for the simulations, differing each other as regards the distance d between the NS and the SN, their reciprocal position and the presence of a guard ring. The four configurations are the following, as illustrated in fig.3:

1. d = 100 µm
2. d = 1mm
3. the SN position varies along a 100µm circle centred on the noisy inverter
4. introduction of a guard ring (p+ diffusion, two side contact wide, with a dedicated ground) surrounding the sensitive NMOS.

The four cases described above will be indicated as *Substrate1*, *Substrate2*, *Substrate3*, and *Substrate4*, respectively.

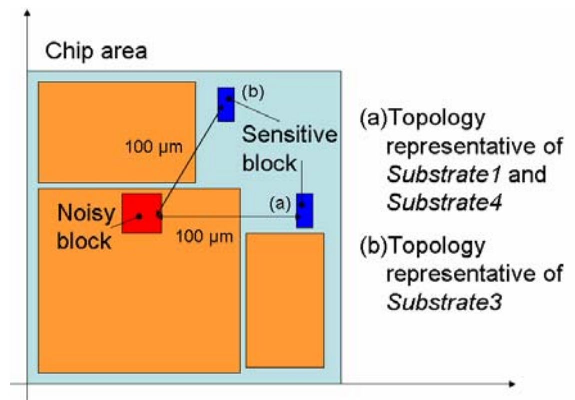

Fig. 3: Schematic of different configurations investigated.

Fig.4 shows *Substrate1* layout. The inverter is on the left side and is composed of only two transistors having the minimum size allowed. Fig.5 shows the sensitive block layout in the case of *Substrate4*, in which the p+ diffusion guard ring surrounding the NMOS is evident.

According to the theoretical assumptions, transient simulation results show a negative-going voltage transient in the substrate that implies a positive spike in the sensitive output voltage, considering the high-to-low transition at the noisy inverter output. Waveforms referred to *Substrate2* and *Substrate4* show the smallest spike amplitude and the lowest signal value, respectively. This confirms that the distance and p+ guard ring are effective factors to improve isolation. The spike amplitude is dependent on the rise and the fall time, too.

AC simulations have provided more interesting results. VPLUS (PDRIFTMOS bulk contact), VMINUS (NDRIFTMOS bulk contact/PDRIFTMOS substrate contact) and OUT contacts were considered as independent noise sources. Simulations have been performed considering an AC voltage component equal to 1 V applied to one node per simulation in every layout case. Fig.6 shows the obtained results: the curve marked with a triangle represents *Substrate1*, the curve marked with a circle represents *Substrate2*, the curve marked with a square represents *Substrate3* and the curve marked with a diamond represents *Substrate4*.

Noise contribute from OUT corresponding to *Substrate3* is equal to -57 dB @ 2.4 GHz. Noise contribute from VPLUS corresponding to *Substrate3* is -48 dB @ 2.4 GHz. Both of them are less significant than noise contribute injected from VMINUS node in *Substrate3* (-19 dB of attenuation @ 2.4 GHz).

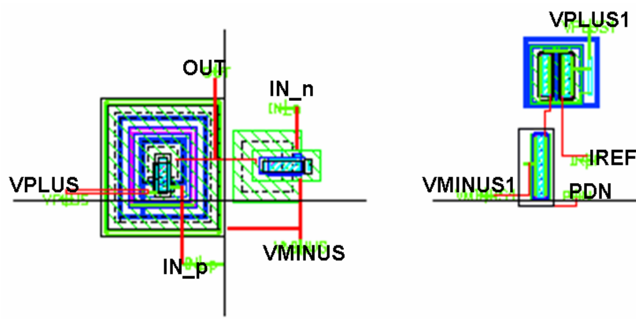

Fig. 4. *Substrate1* layout (not in scale).

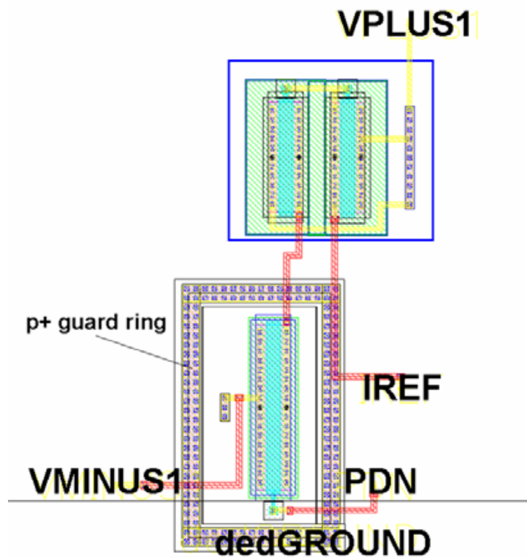

Fig. 5. Sensitive block layout in *Substrate4*.

Noise contribute from VMINUS is dominant with respect to other noise sources. Two causes mostly can explain this result. VMINUS represents the ground reference for PDRIFTMOS substrate contact which has the largest extension, as shown by the layout; therefore it represents an important noise injector. Moreover, VMINUS is also the ground reference for NDRIFTMOS bulk contact and, as shown by experimental results, noise injection coming from NMOS devices is higher than that from PMOS. From floorplanning design it is evident that diagonal position of sensitive node (at an equivalent distance of 100 μm) gives worse results than simple linear position between noisy/sensitive bulk contacts. Better results are provided by a longer distance and by the introduction of a p+ guard ring. In fact, with respect to all noise sources, in *Substrate4*, an isolation improvement up to 28dB @ 2.4 GHz is obtained with respect to *Substrate1*. Peaks in the frequency response (mostly referred to VMINUS noise source) are due to the capacitive coupling from the p+ diffusion substrate contact and to the bond-wire connection.

Beyond a certain frequency value, this effect becomes dominant even in presence of a guarding structure (*Substrate4*). p+ diffusion guard ring width is no more sufficient to isolate the sensitive block and a peak in the sensitive drain waveform appears.

SNA provides the surface noise distribution only as guideline for guard ring effectiveness. Fig. 7 illustrates SNA results related to different cases. The isolation improvement deriving from the introduction of the guard ring results from the legend reported in the figure.

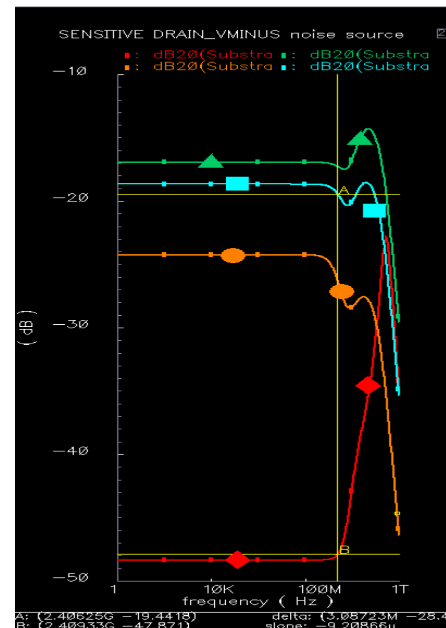

Fig. 6. Sensitive drain AC response corresponding to VMINUS source nodes.

4. Conclusions

The substrate analysis for a DC- DC converter integration in a RF CMOS IC has been developed in this paper. Different topologies of the DC-DC converter core have been designed using DRIFTMOS transistors in 0.13 μm CMOS technology. Noise injection/coupling effects through the lightly-doped-substrate have been investigated to provide guidelines in improving sensitive analog/RF circuits isolation. The obtained results show the effectiveness of the introduction of guarding structures such as p+ diffusion guard rings surrounding sensitive block. The strong impact of separation distance between noisy

and sensitive blocks and their relative position in the floorplanning have been also illustrated.

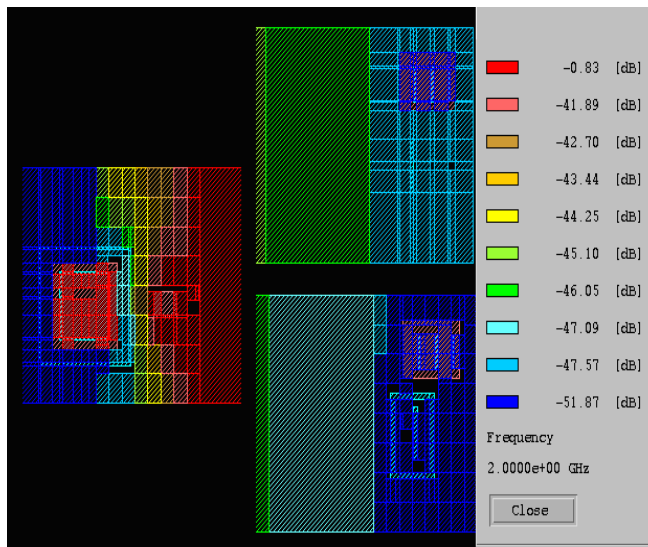

Fig. 7. SNA surface noise distribution: on the left side, a detail of the noisy block is shown; on the right side, two details from *Substrate1* and *Substrate4* of the sensitive block.

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